# Full accounting for verifiable outsourcing

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Justin Thaler[△], Michael Walfish[◦], and Thomas Wies[◦]

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[◦]New York University
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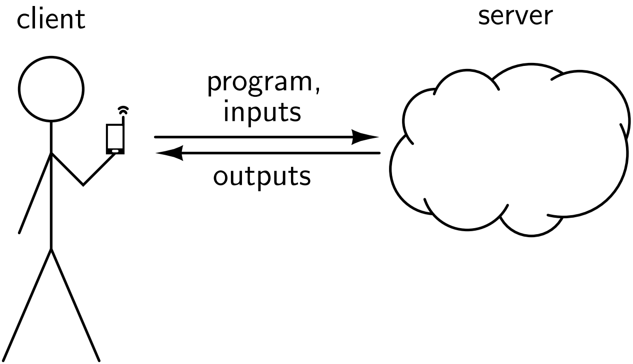
[‡]Northeastern University
[△]Georgetown University

November 2nd, 2017

# Probabilistic proofs enable outsourcing



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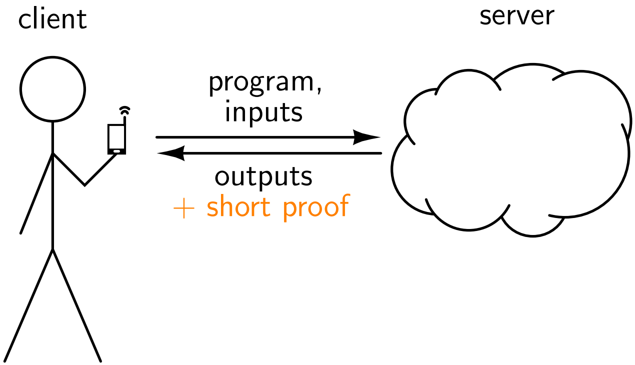
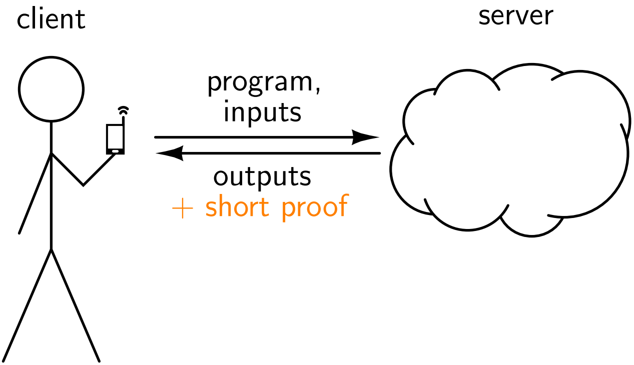



Approach: Server's response includes short proof of correctness.

[Babai85, GMR85, BCC86, BFLS91, FGLSS91, ALMSS92, AS92, Kilian92, LFKN92, Shamir92, Micali00, BG02, BS05, GOS06, BGHSV06, IKO07, GKR08, KR09, GGP10, Groth10, GLR11, Lipmaa11, BCCT12, GGPR13, BCCT13, Thaler13, KRR14, . . . ]

# Probabilistic proofs enable outsourcing

SBW11
CMT12
SMBW12
TRMP12
SVPBBW12
SBVBPW13
VSBW13
PGHR13
BCGTV13
BFRSBW13
BFR13
DFKP13
BCTV14a
BCTV14b




BCGGMTV14
FL14
KPPSST14
FTP14
WSRHBW15
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CFHKNPZ15
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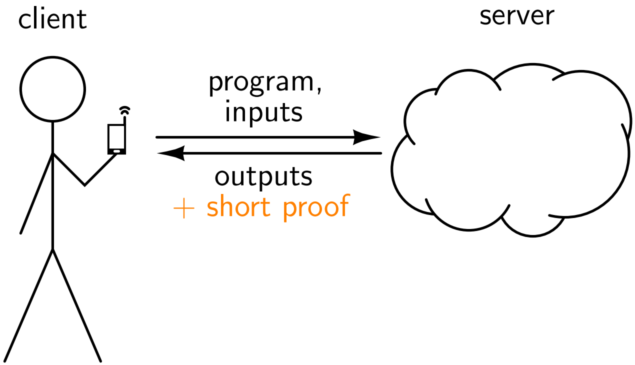


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**Goal:** outsourcing should be less expensive than just executing the computation

# Do systems achieve this goal?

Verifier ($\mathcal{V}$): can easily check proof (asymptotically)

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Prover: assume $\mathcal{P}$ is $>10^8\times$ cheaper than $\mathcal{V}$

# Our contribution

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- an asymptotically $\mathcal{P}$-optimal proof protocol that improves on prior work [Thaler, CRYPTO13]
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# Roadmap

1. Verifiable ASICs
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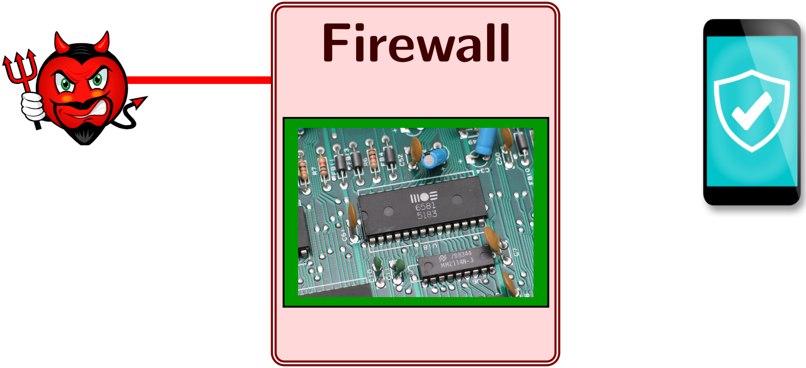
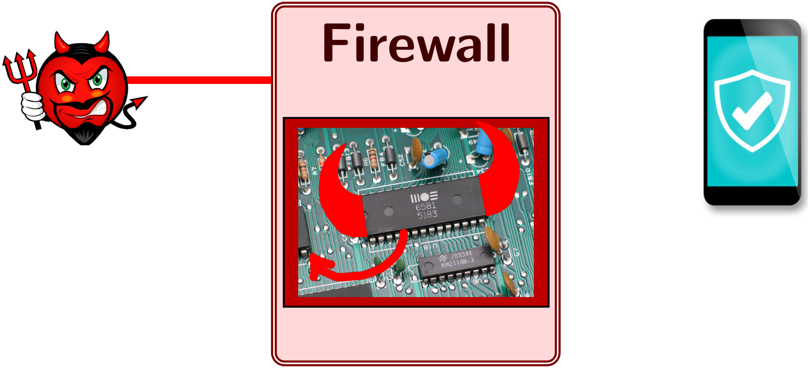
## How can we build trustworthy hardware?




e.g., a custom chip for network packet processing whose manufacture we outsource to a third party

# Untrusted manufacturers can craft hardware Trojans

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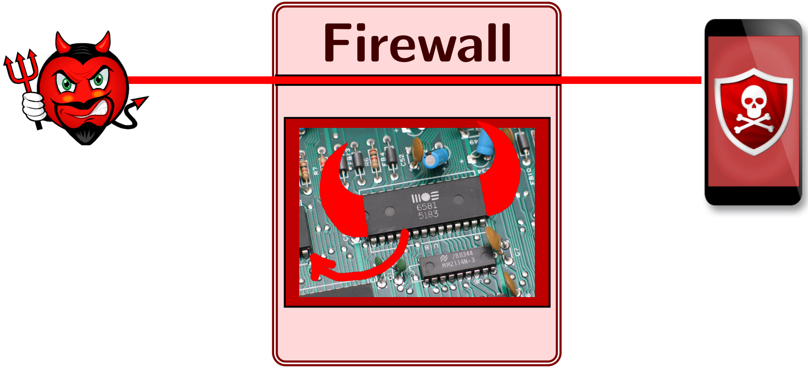


What if the chip's manufacturer inserts a **back door**?

Threat: incorrect execution of the packet filter

(Other concerns, e.g., secret state, are important but orthogonal)

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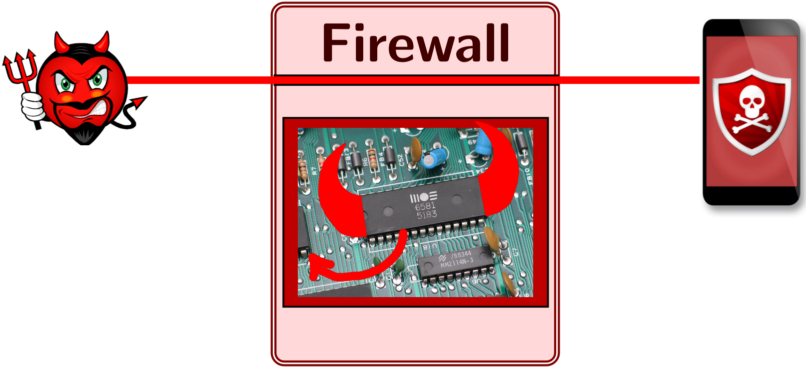


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The Cybercrime Economy

## Fake tech gear has infiltrated the U.S. government

by David Goldman @DavidGoldmanCNN

November 8, 2012: 3:10 PM ET

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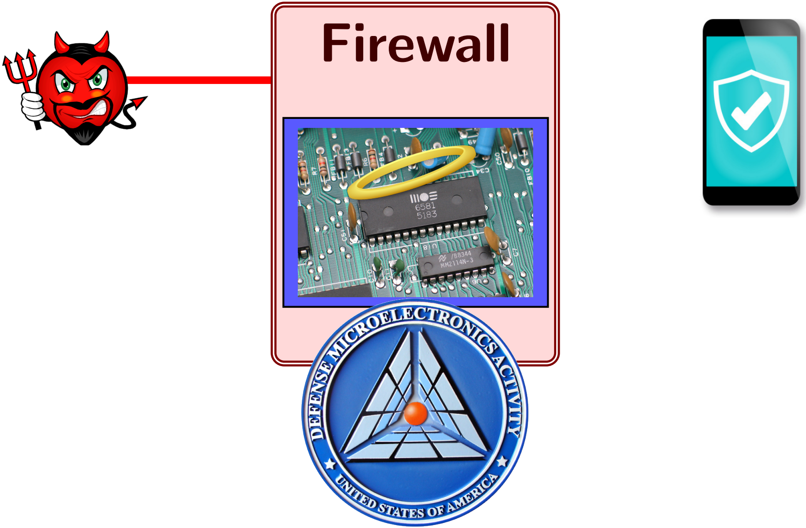


US DoD controls supply chain with **trusted foundries**.

# Trusted fabs are the only way to get strong guarantees

For example, stealthy trojans can thwart post-fab detection
[A2: Analog Malicious Hardware, Yang et al., Oakland16; Stealthy Dopant-Level Trojans, Becker et al., CHES13]

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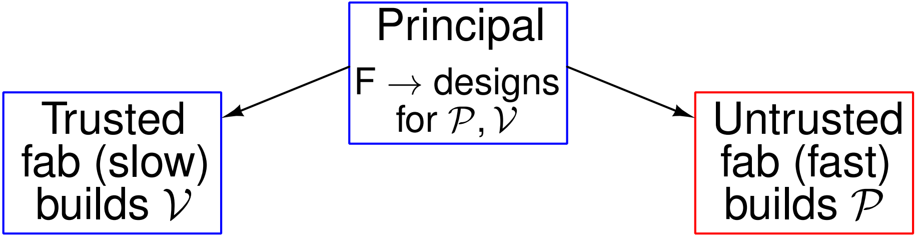
**Idea:** outsource computations to untrusted chips

# Verifiable ASICs [WHGsW16]

Principal

F $\rightarrow$ designs for $\mathcal{P}, \mathcal{V}$

# Verifiable ASICs [WHGsW16]



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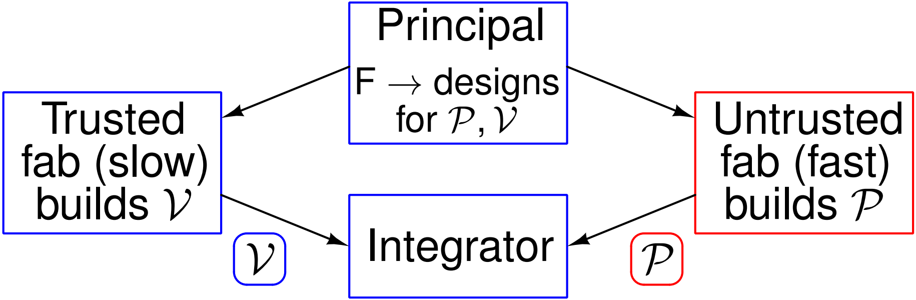

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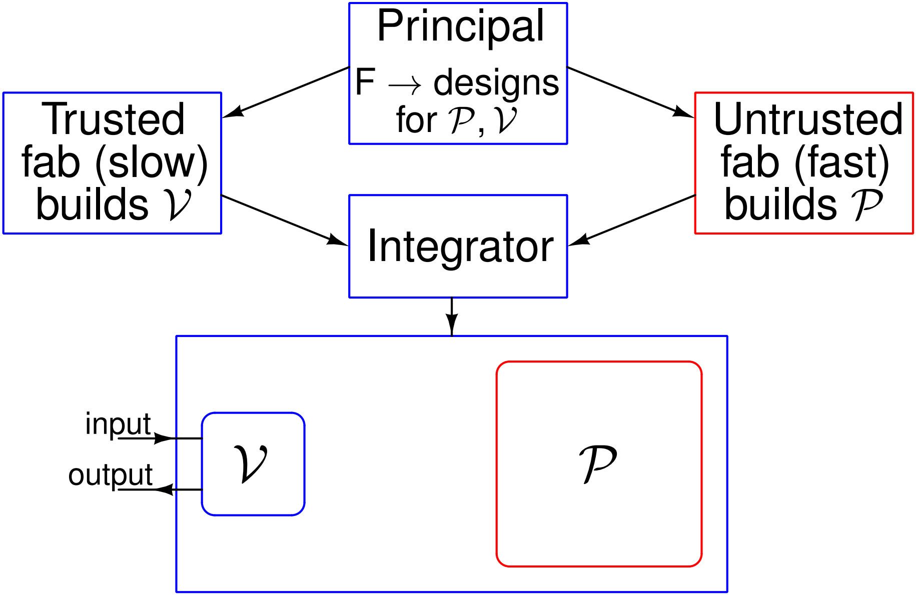

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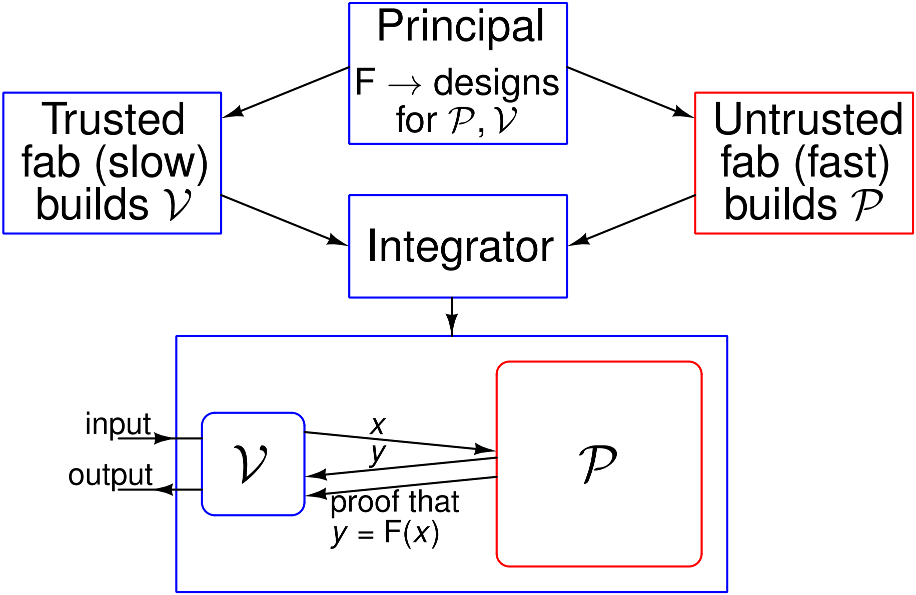
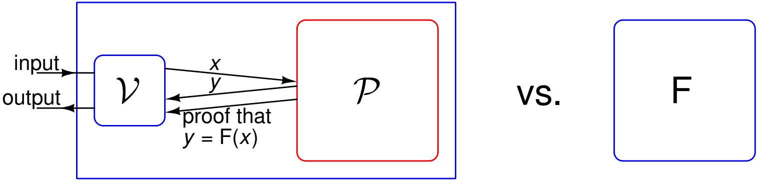


# Can Verifiable ASICs be practical?

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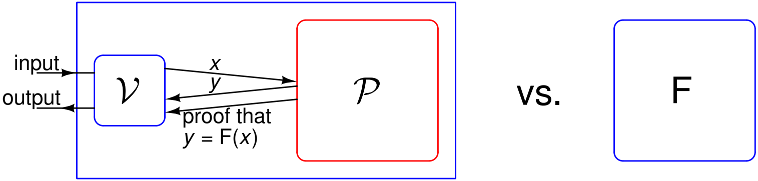


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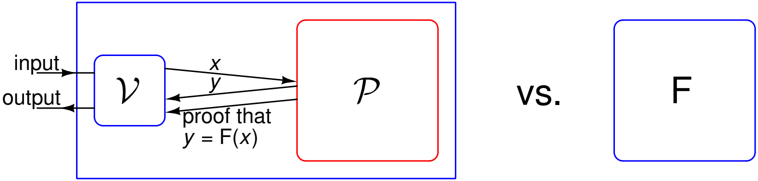


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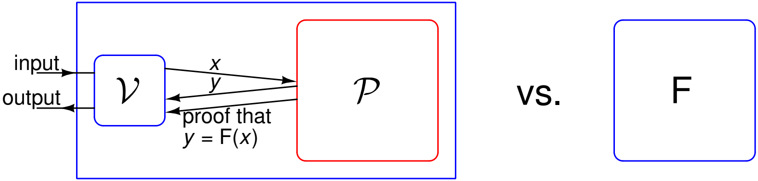


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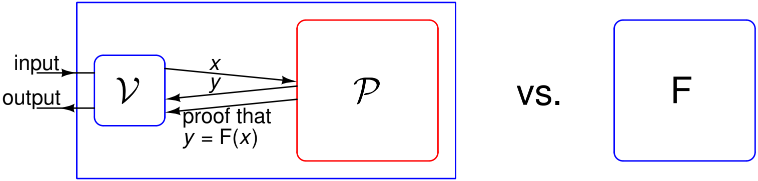


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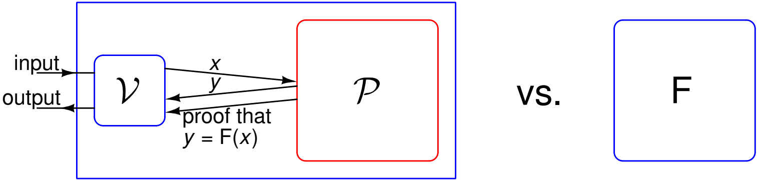


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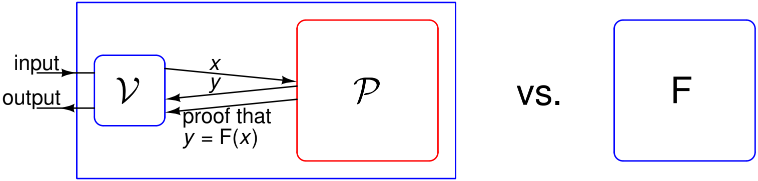


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Our goal:

$$\mathcal{V} + \mathcal{P} + \text{Precomp} < \text{F}$$

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2. Giraffe: a high-level view
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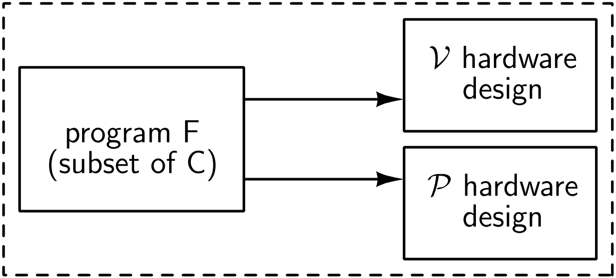
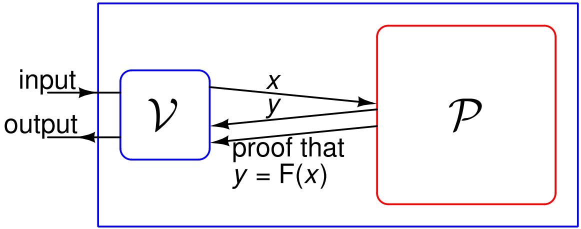
# Giraffe: a high-level view



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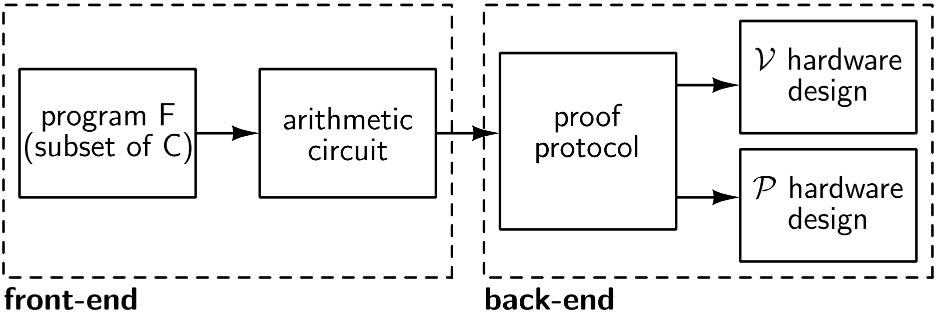


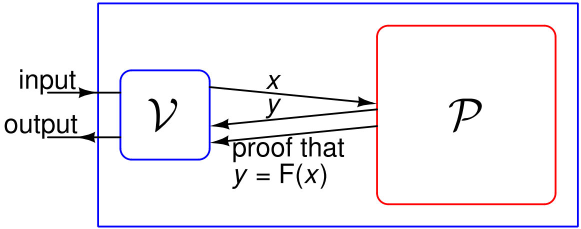

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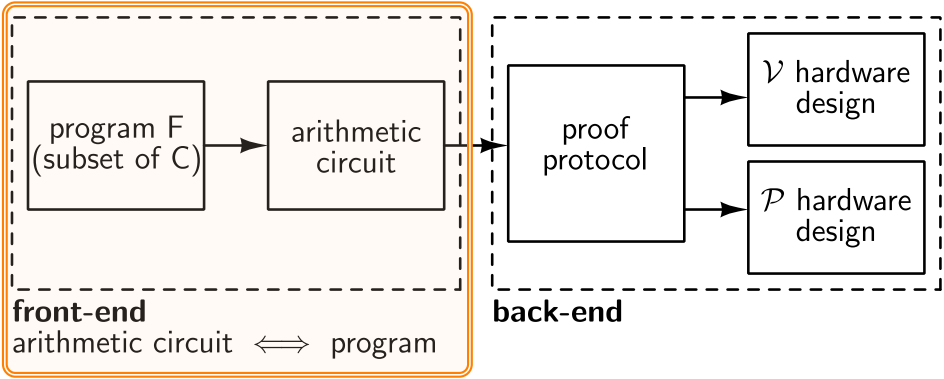


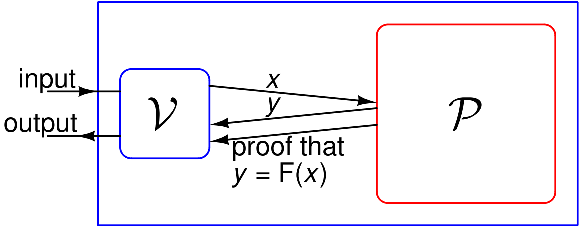

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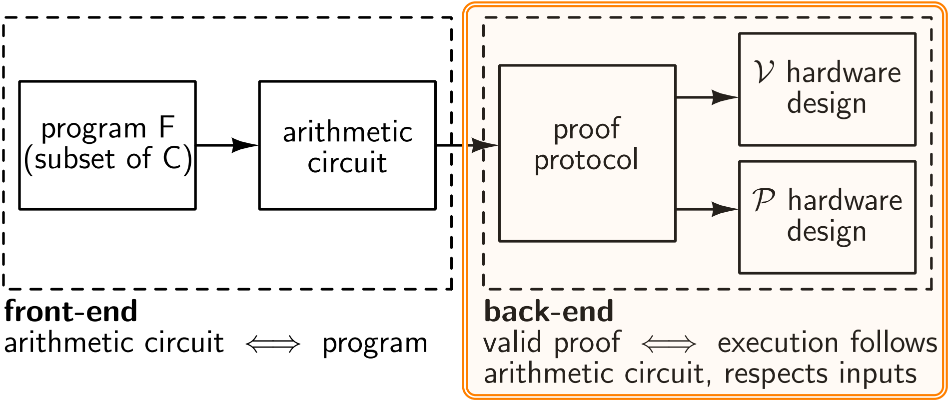


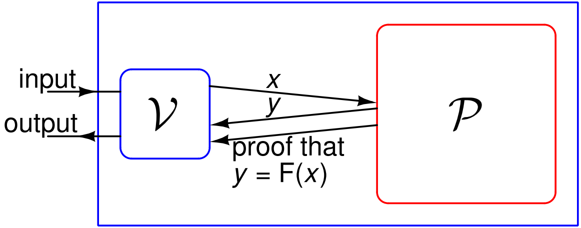

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GKR08 base protocol

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|---|---|
| GKR08 | base protocol |
| CMT12 | reduces $\mathcal{P}$ and precomp costs for all ckts |
| Thaler13 | reduces precomp for structured circuits |
| Giraffe | reduces $\mathcal{P}$ cost for structured circuits (plus optimizations for $\mathcal{V}$; see paper) |

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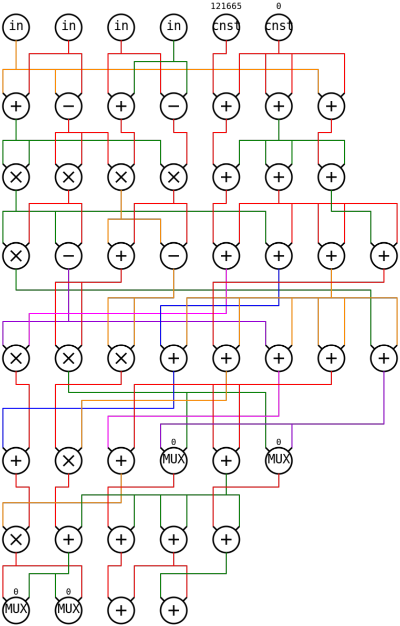
Giraffe reduces $\mathcal{P}$ cost for structured circuits
(plus optimizations for $\mathcal{V}$; see paper)

Let's take a high-level look at how these optimizations work.
(The following all use a nice simplification [Thaler15].)

# GKR08: an IP for arithmetic circuit evaluation

F must be expressed as a *layered* arithmetic circuit.



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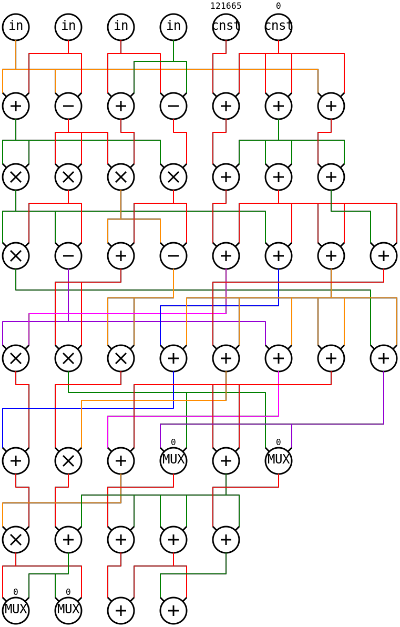


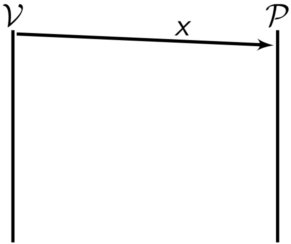

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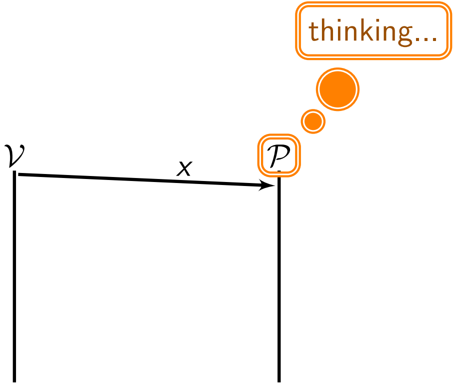


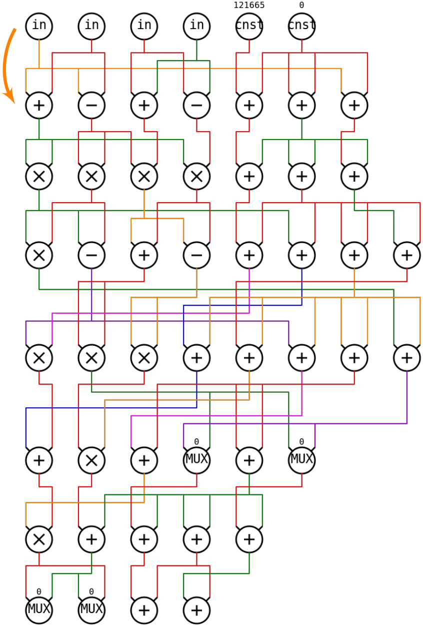

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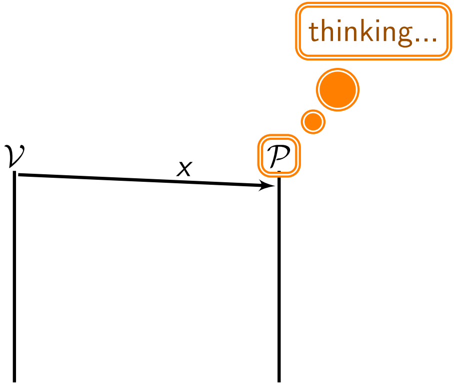


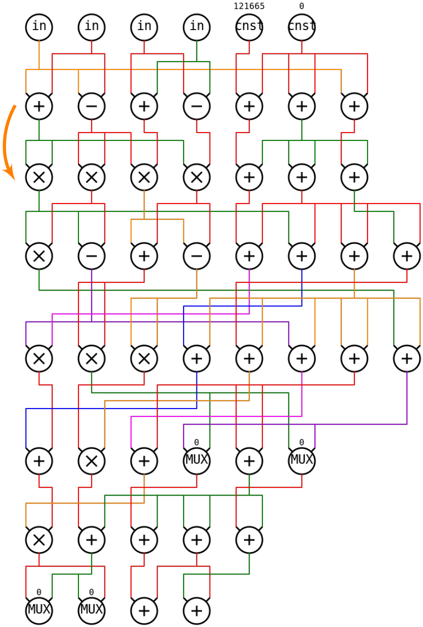

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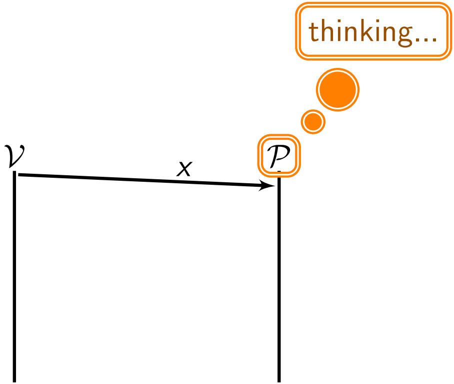


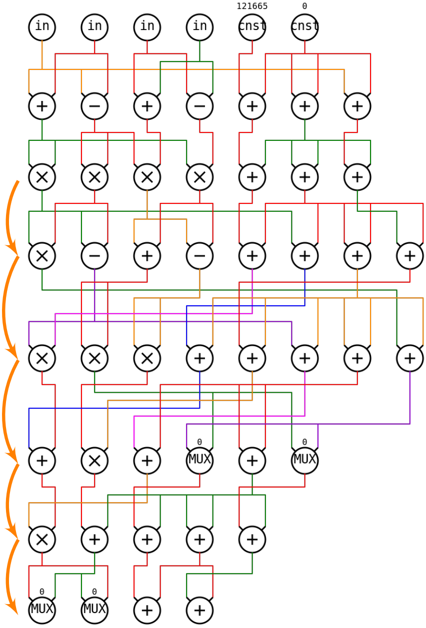

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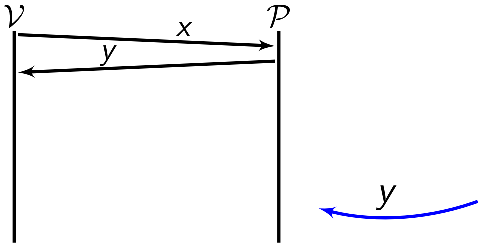


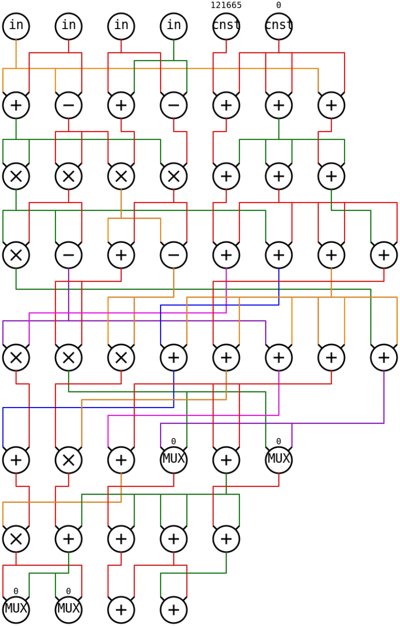

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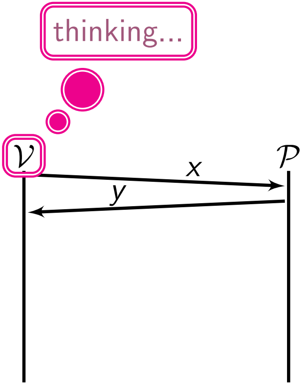


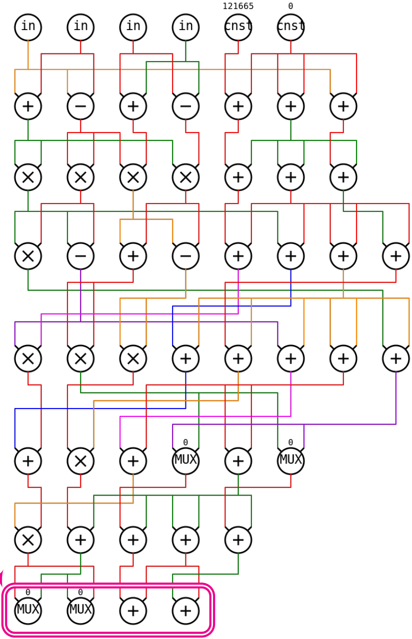

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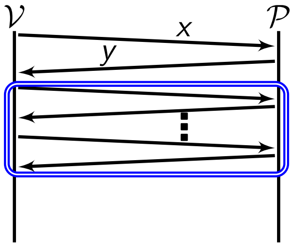
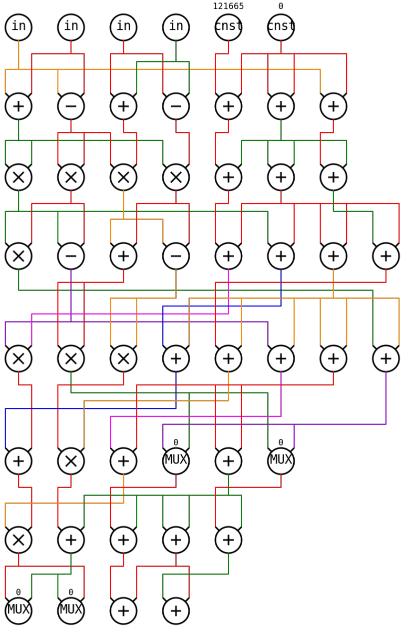
4. $\mathcal{V}$ engages $\mathcal{P}$ in a sum-check




sum-check [LFKN90]



# GKR08: an IP for arithmetic circuit evaluation

1. $\mathcal{V}$ sends inputs
2. $\mathcal{P}$ evaluates, returns output $y$
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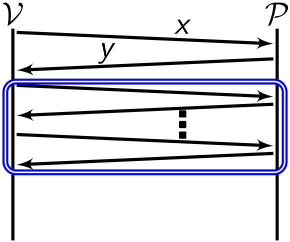
4. $\mathcal{V}$ engages $\mathcal{P}$ in a sum-check, gets claim about second-last layer

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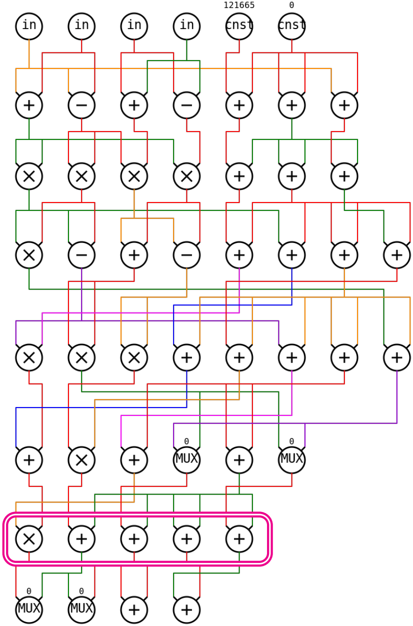

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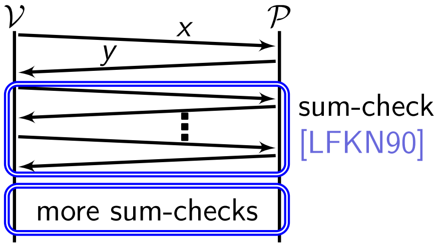


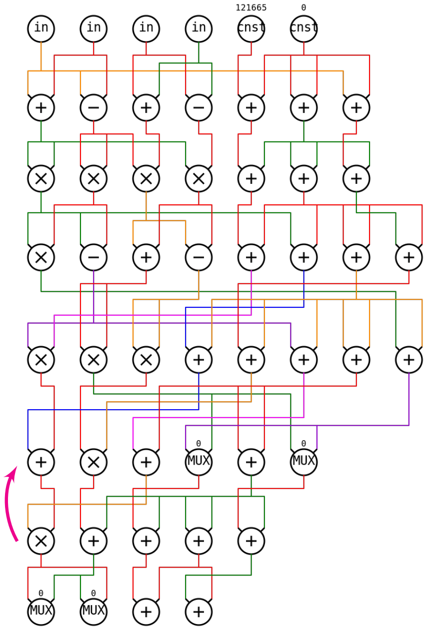

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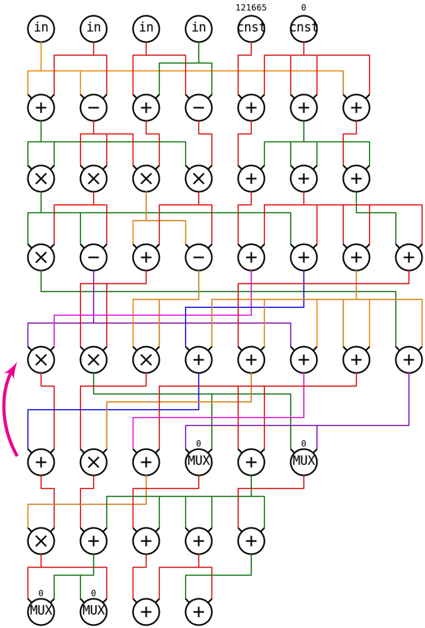


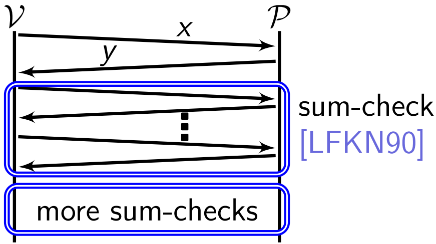

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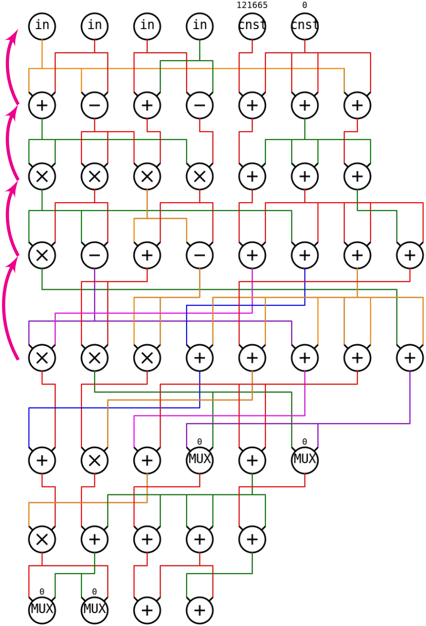


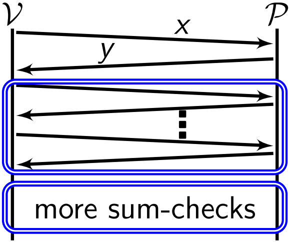


sum-check
[LFKN90]

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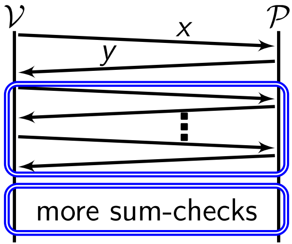
5. $\mathcal{V}$ iterates, gets claim about inputs, which it can check

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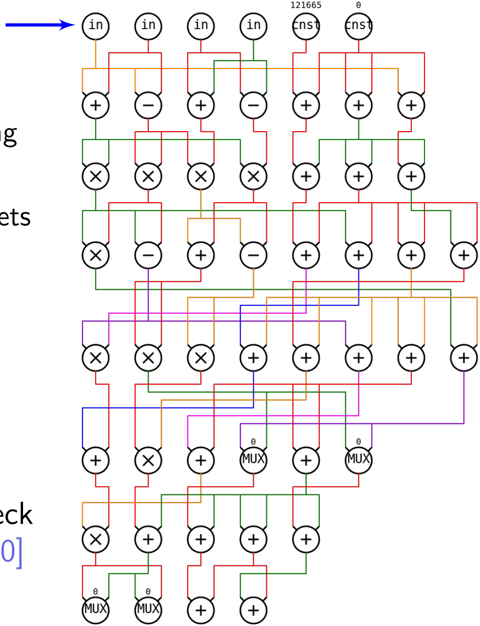
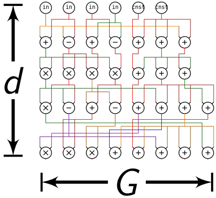


# GKR08: polynomial-time $\mathcal{P}$

For each layer, $\mathcal{P}$ and $\mathcal{V}$ engage in a sum-check protocol.



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For each layer, $\mathcal{P}$ and $\mathcal{V}$ engage in a sum-check protocol.

In the first round, $\mathcal{P}$ computes ($q \in \mathbb{F}^{\log G}$):

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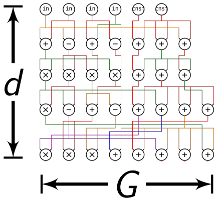

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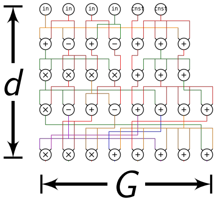
This has $2^{2 \log G} = G^2$ terms. In total, $\mathcal{P}$'s work is $\boxed{\text{O}(\text{poly}(G))}$.



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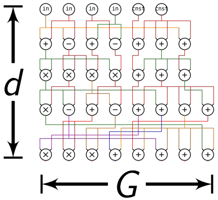
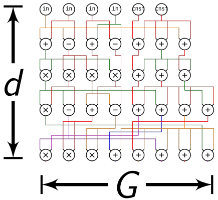
Precomputation is one evaluation of $\tilde{\text{add}}$ and $\tilde{\text{mul}}$, costing O(poly($G$)).



# CMT12: from polynomial to quasilinear

$\mathrm{add}(g_O, g_L, g_R) = 0$ except when $g_O$ is $+$ with inputs $g_L, g_R$



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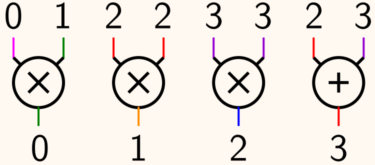
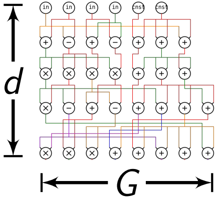



$\mathrm{add}(3, 2, 3) = 1$, otherwise $\mathrm{add}(\cdots) = 0$



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This means we can rewrite $\mathcal{P}$'s sum in the first round as:

$$\sum_{(h_0,h_1)\in S_{\mathrm{add}}} \tilde{\mathrm{add}}(q, h_0, h_1)\left(\tilde{\mathrm{V}}(h_0) + \tilde{\mathrm{V}}(h_1)\right) +$$
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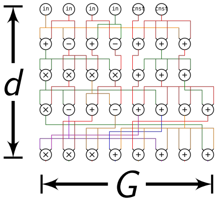

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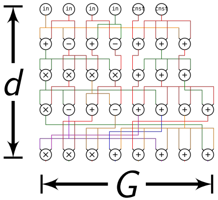
$G$ terms/round for $2\log G$ rounds: $\mathcal{P}$'s work is $\boxed{\mathrm{O}(G\log G)}$.



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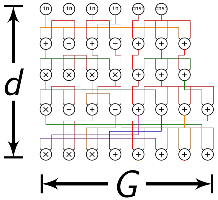
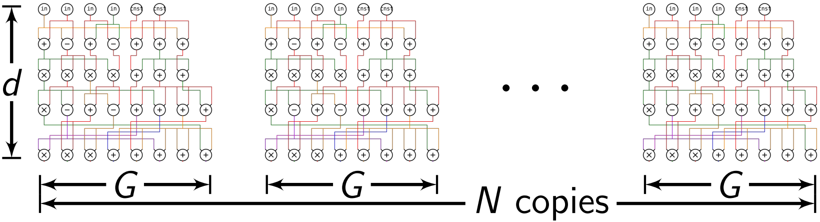
Using a related trick, precomputing $\tilde{\mathrm{add}}$ and $\tilde{\mathrm{mul}}$ costs $\mathrm{O}(G)$ in total.



# Thaler13: more structure, less precomputation

Idea: for a *batch* of identical subckts, $\widetilde{\mathrm{add}}$ and $\widetilde{\mathrm{mul}}$ can be "small."



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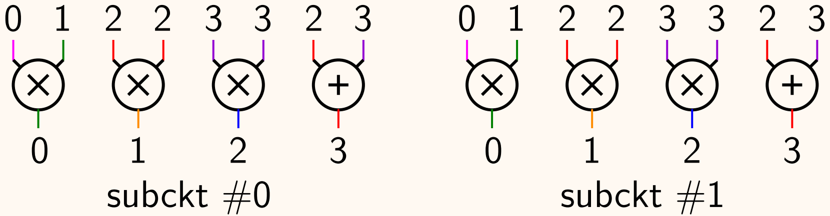
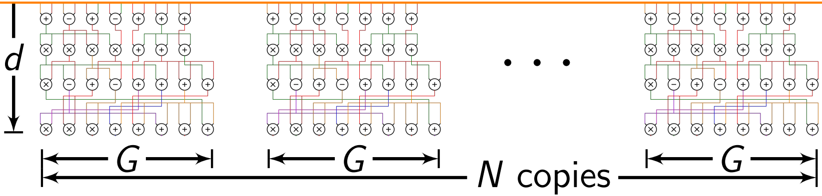



$\widetilde{\text{add}}(3, 2, 3) = 1$, otherwise $\widetilde{\text{add}}(\cdots) = 0$

Notice that $\widetilde{\text{add}}$ does not comprehend subcircuit number!



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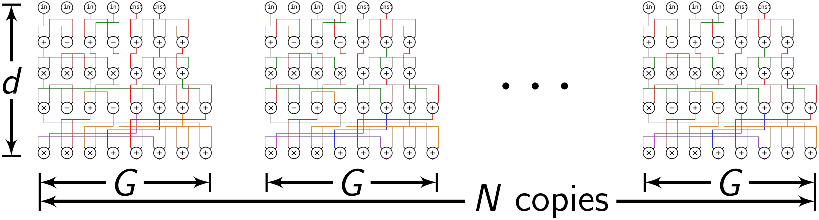
➔ Precomp costs $O(G)$, amortized over $N$ copies!



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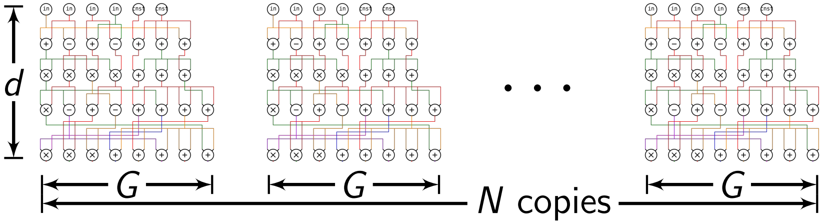

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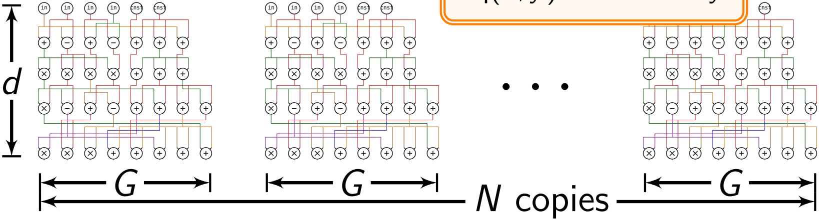
$\text{eq}(x, y) = 1$ iff $x = y$



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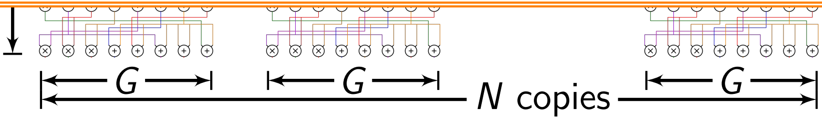
For each gate,



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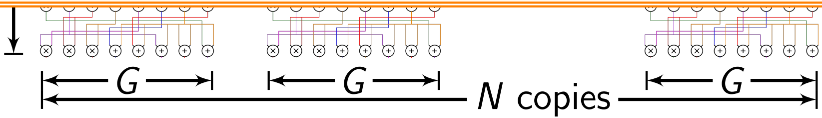
For each gate, sum over each subcircuit.



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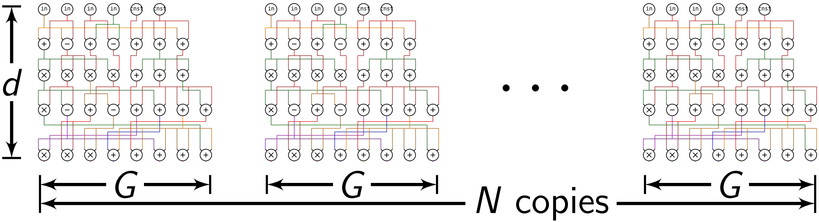
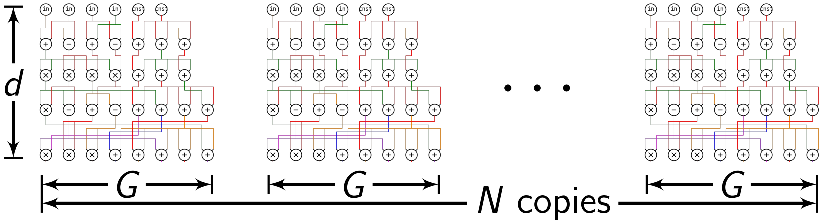
$NG$ terms/round in first $2 \log G$ rounds: $\mathcal{P}$'s work is $\boxed{\Omega(NG \log G)}$.



# Giraffe: leveraging structure to reduce $\mathcal{P}$ costs

Idea: arrange for copies to "collapse" during sum-check protocol.



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Rewriting the prior sum and changing sumcheck order:

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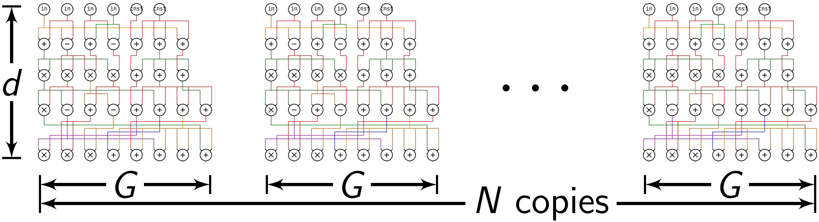

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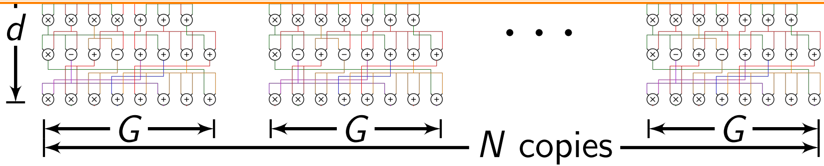
For each subcircuit,



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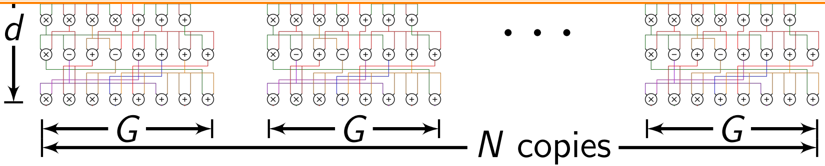
For each subcircuit, sum over each gate.



# Giraffe: leveraging structure to reduce $\mathcal{P}$ costs

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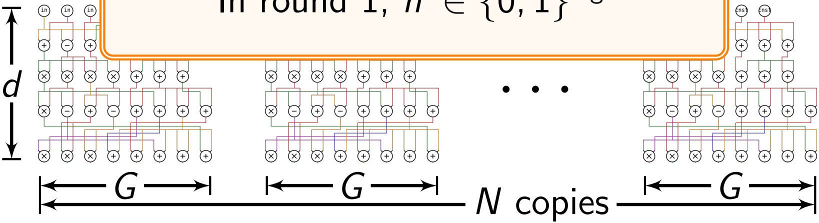
In round 1, $h' \in \{0,1\}^{\log N}$



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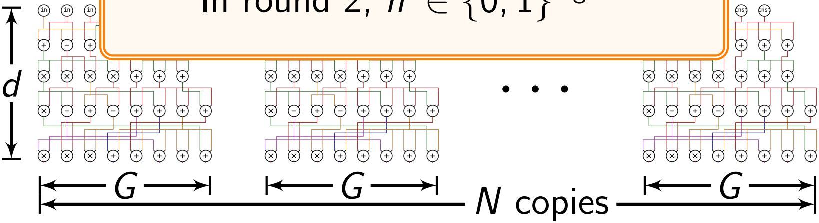
In round 2, $h' \in \{0,1\}^{\log N - 1}$



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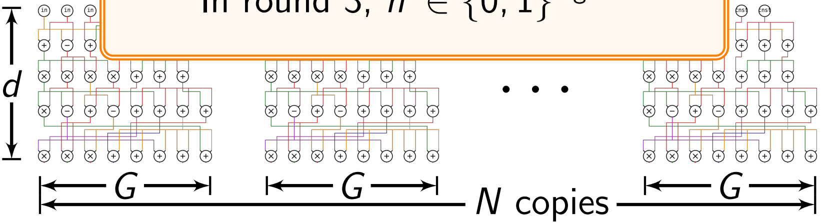
In round 3, $h' \in \{0,1\}^{\log N - 2}$



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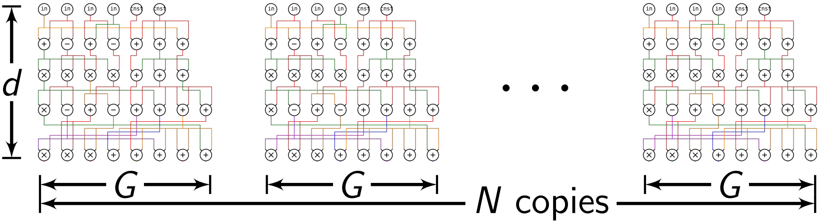
$\mathcal{P}$ does $\left(N + \frac{N}{2} + \frac{N}{4} + \ldots\right) G + 2G \log G = \boxed{\mathrm{O}(NG + G \log G)}$ work.



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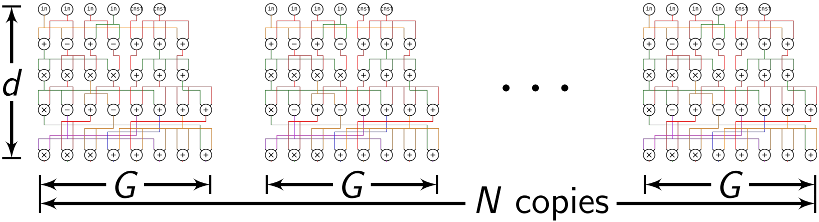
➔ Linear in size of computation when $N > \log G$!



# Roadmap

1. Verifiable ASICs
2. Giraffe: a high-level view
3. Evaluation

# Implementation

Giraffe is an end-to-end hardware generator:

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- a hardware *design template*
  - given computation, chip parameters (technology, size, ...), produces optimized hardware designs for $\mathcal{P}$ and $\mathcal{V}$

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- a hardware *design template*
  given computation, chip parameters (technology, size, ...), produces optimized hardware designs for $\mathcal{P}$ and $\mathcal{V}$
- a (subset of) C compiler
  produces the representation used by the design template

# Evaluation questions

How does Giraffe perform on real-world computations?

1. Curve25519 point multiplication
2. Image matching

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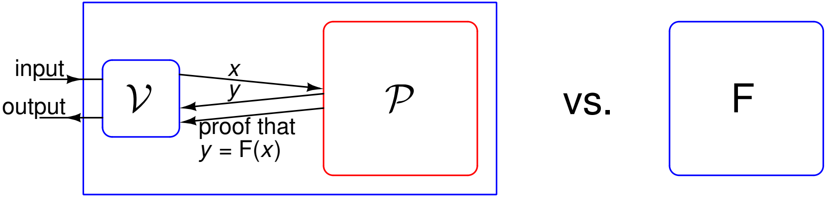
1. Curve25519 point multiplication
2. Image matching

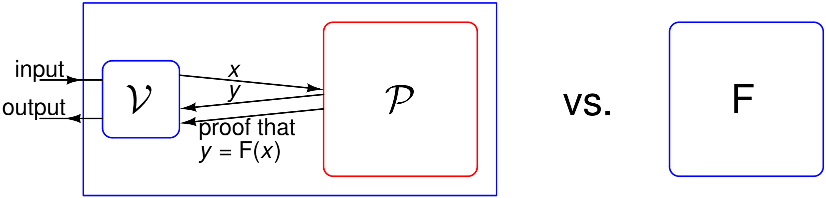
**Goal:** total cost of $\mathcal{V}$, $\mathcal{P}$, and precomputation should be less than building F on a trusted chip

# Evaluation method




Baselines: Zebra; implementation of F in same technology as $\mathcal{V}$

# Evaluation method

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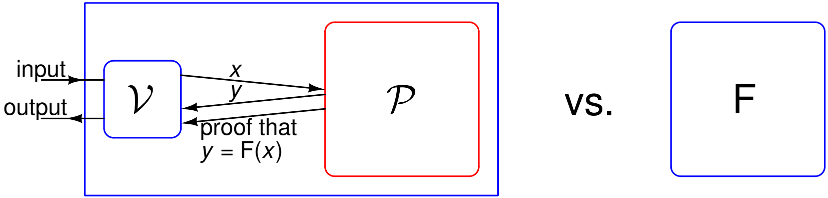
Metric: total energy consumption

# Evaluation method

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Metric: total energy consumption

Measurements: based on circuit synthesis and simulation, published chip designs, and CMOS scaling models

Charge for $\mathcal{V}$, $\mathcal{P}$, communication; precomputation; PRNG

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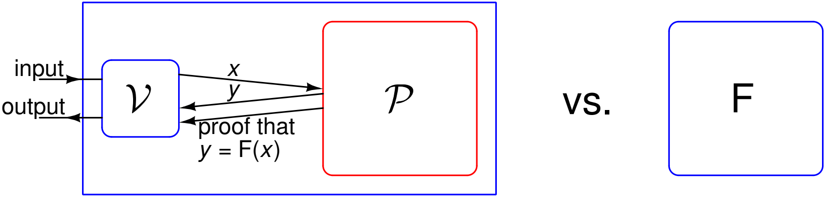


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Metric: total energy consumptio

Measurements: based on circuit
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350 nm: 1997 (Pentium II)
7 nm: $\approx$ 2018
$\approx$ 20 year gap between
trusted and untrusted fab

Charge for $\mathcal{V}$, $\mathcal{P}$, communication; precomputation; PRN

Constraints: trusted fab = 350 nm; untrusted fab = 7 nm
200 mm$^2$ max chip area; 150 W max total power

# Application #1: Curve25519 point multiplication

Curve25519: a commonly-used elliptic curve

Point multiplication: primitive, e.g., for ECDH

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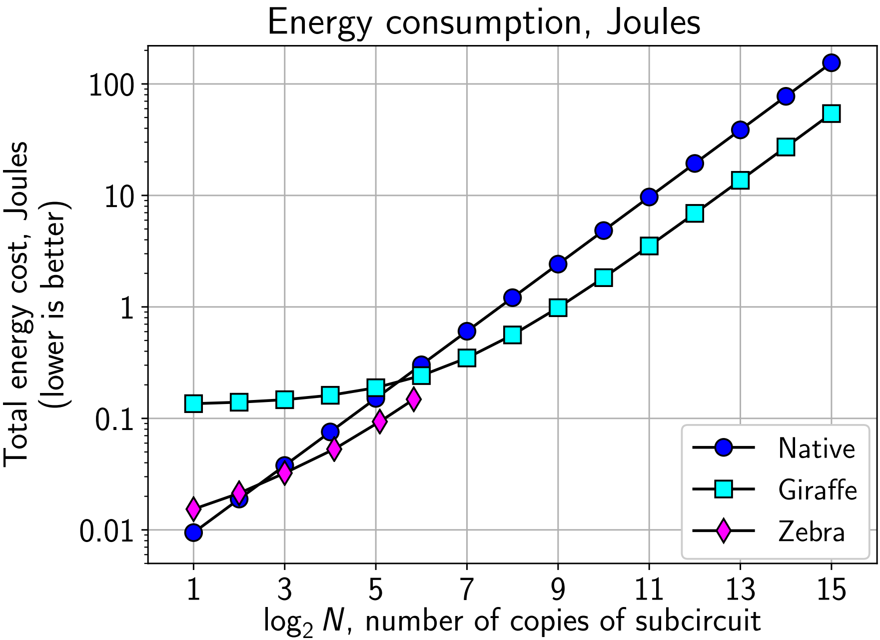

# Application #2: Image matching

Image matching via Fast Fourier transform

C implementation, compiled by Giraffe's front-end to $\mathcal{V}$ and $\mathcal{P}$ hardware designs—no hand tweaking!

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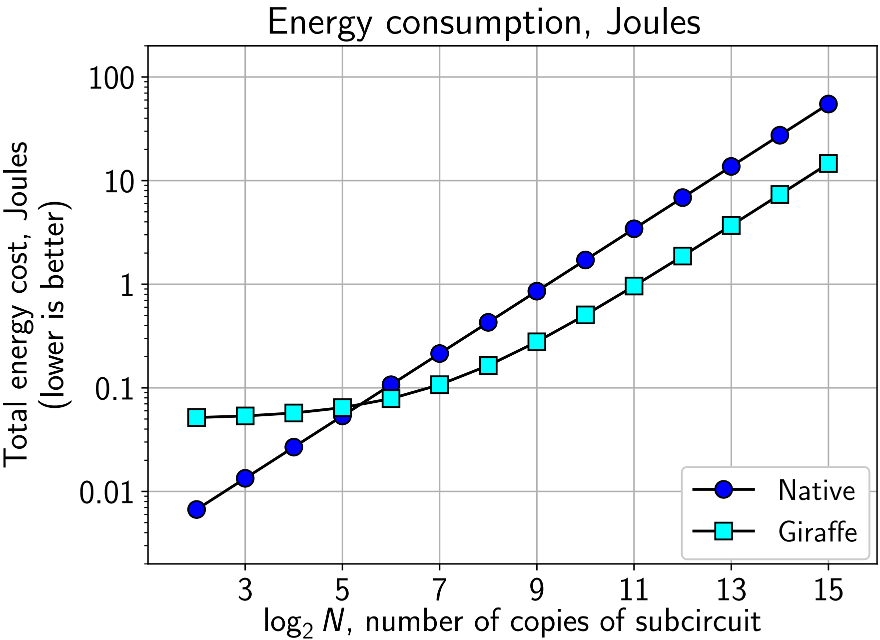
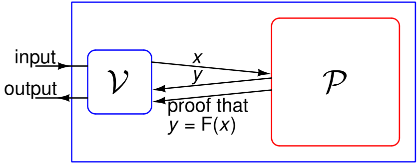


# Recap: is it **practical**?



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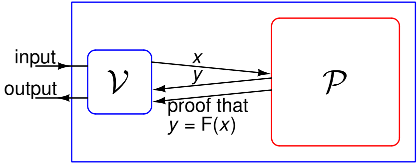


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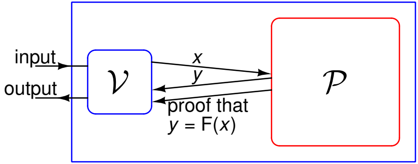


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Giraffe's front-end includes two static analysis passes:

**Slicing** extracts only the parts of programs that can be efficiently outsourced

**Squashing** extracts batch-parallelism from serial computations

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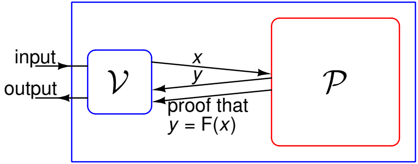


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✓ Giraffe's proof protcol and optimizations save orders of magnitude compared to prior work

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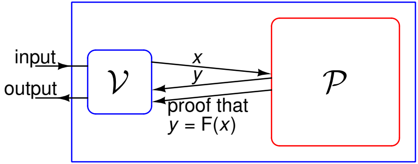


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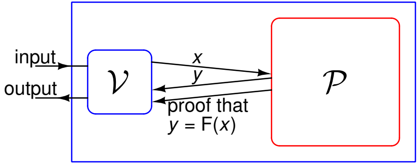


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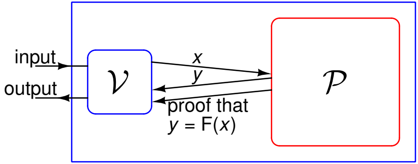


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`https://giraffe.crypto.fyi`

`https://www.pepper-project.org`