Verifying Multithreaded Software with Impact

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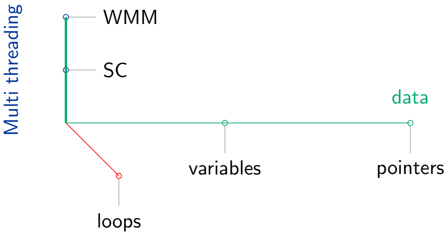
Intro

- Multi-threading
  - C/C++ with POSIX/WIN 32 threads
  - event processing, device drivers, web servers, databases, ...
  - coming to embedded systems
- Verification Challenges



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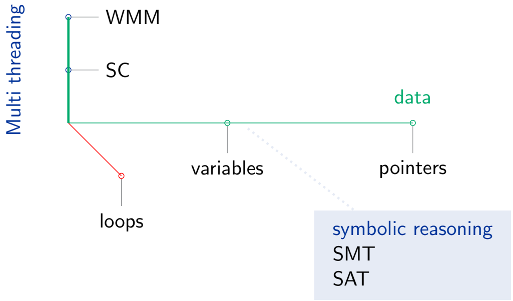

Multi threading

WMM

SC

data

variables

pointers

loops

symbolic reasoning

SMT

SAT

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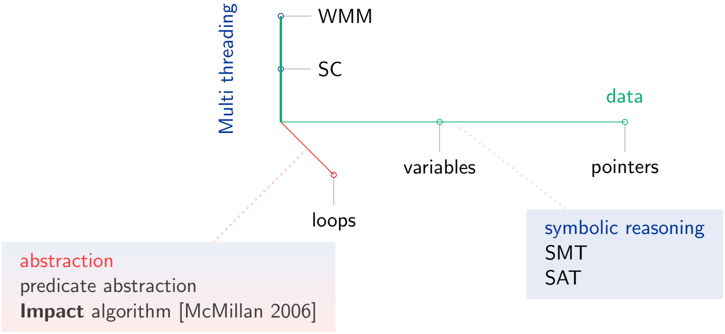

abstraction
predicate abstraction
Impact algorithm [McMillan 2006]

symbolic reasoning
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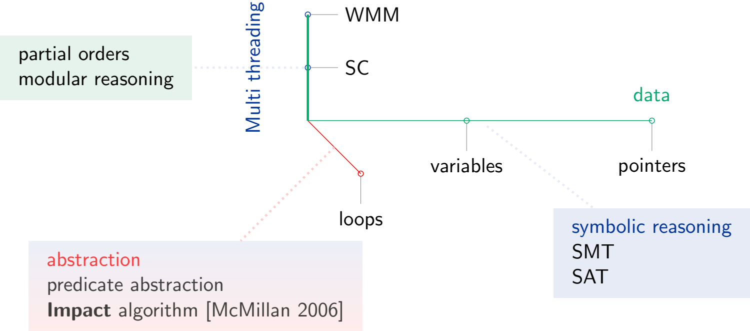

Multi threading

WMM

SC

partial orders
modular reasoning

data

variables

pointers

loops

abstraction
predicate abstraction
Impact algorithm [McMillan 2006]

symbolic reasoning
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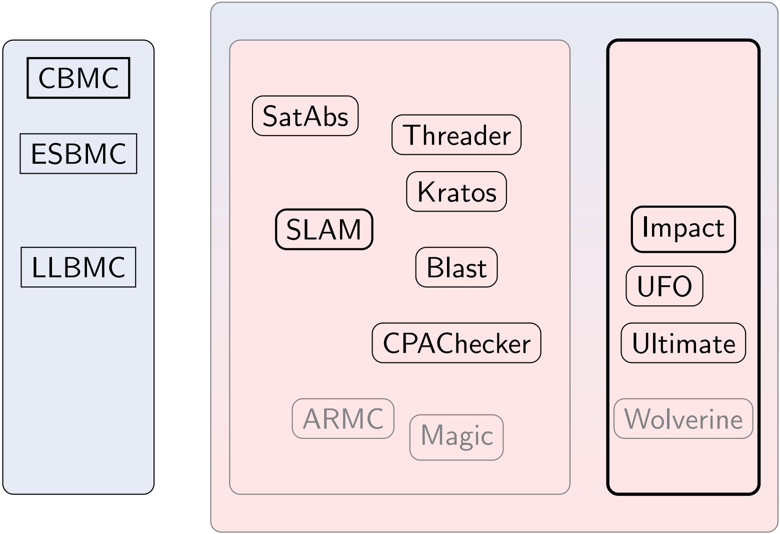
Software model checkers



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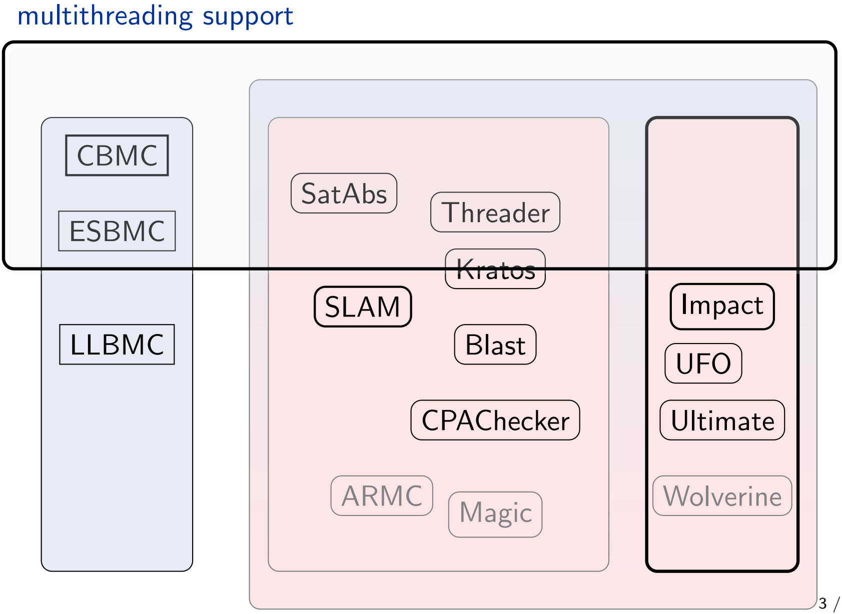

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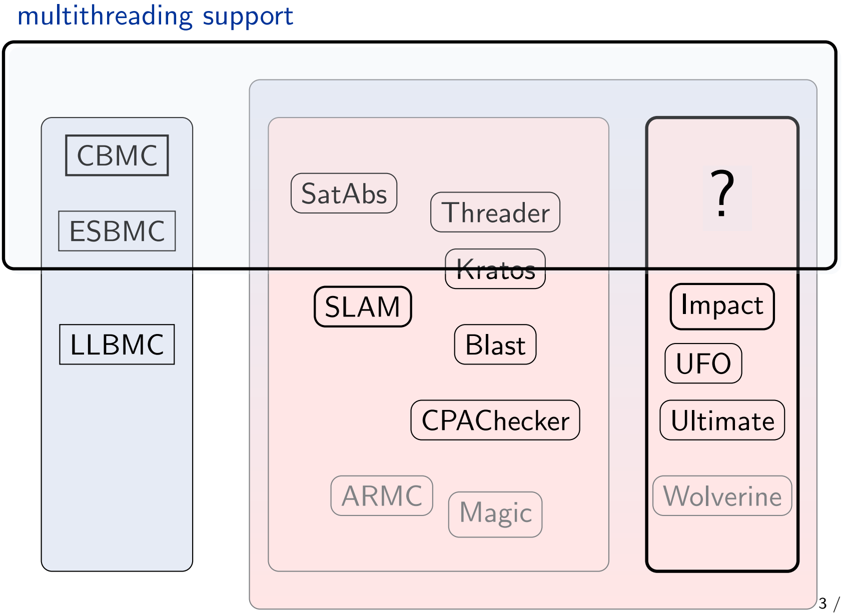
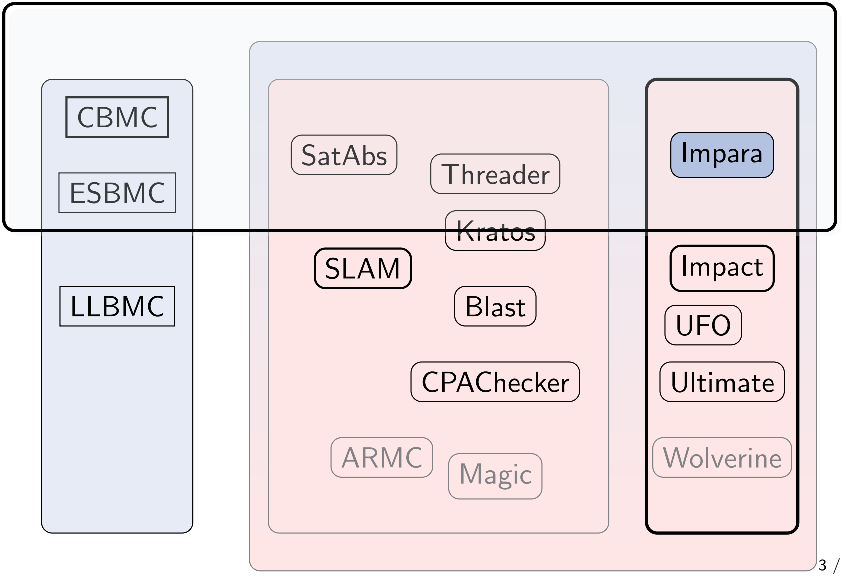


Software model checkers

multithreading support



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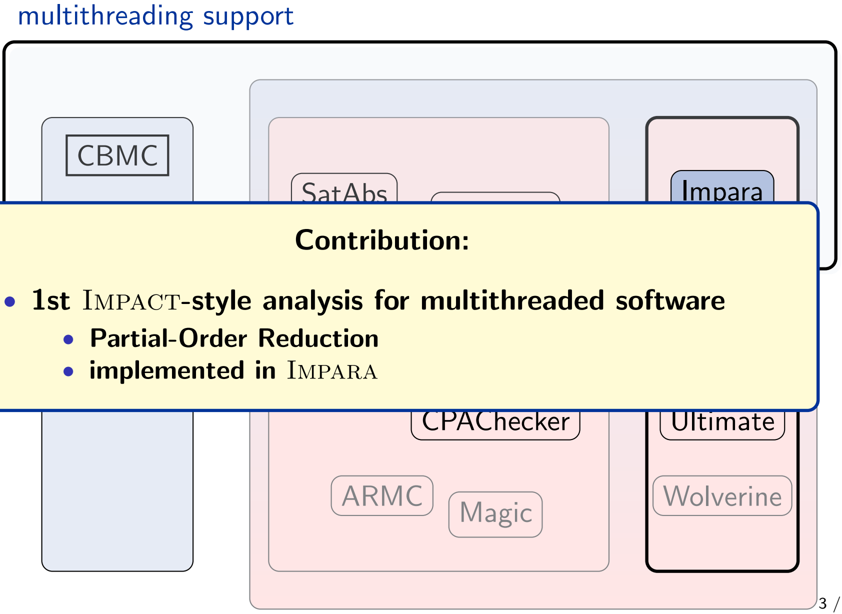


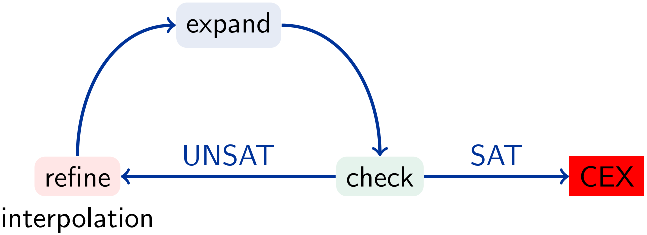
Contribution:

- **1st Impact-style analysis for multithreaded software**
  - **Partial-Order Reduction**
  - **implemented in Impara**

Outline

- Recap: Impact for Sequential Software
- Impact for Multithreaded Software
    - Partial order reduction
- Experiments with our tool Impara

Impact algorithm



- maintain abstract reachability tree
  - node labels
  - covering relation $\triangleright$

$$v \triangleright w \text{ implies } label(v) \Rightarrow label(w)$$

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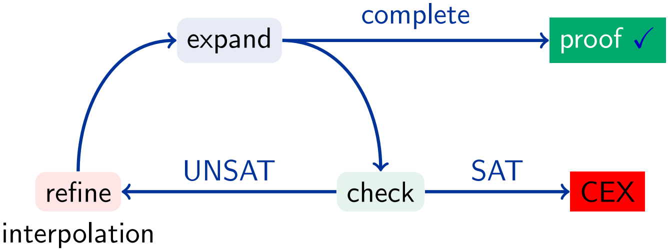

- maintain abstract reachability tree
  - node labels
  - covering relation $\triangleright$

$$v \triangleright w \text{ implies } label(v) \Rightarrow label(w)$$

- complete iff all nodes either
  - covered
  - expanded

Classical SLAM example

```
do {
  lock();
  old=new;
  if(*) {
    unlock();
    new++;
  }
} while (new!=old);
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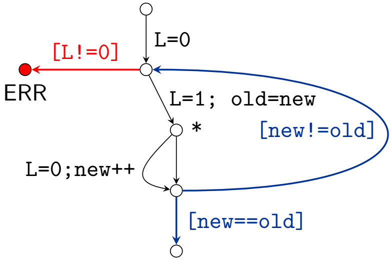
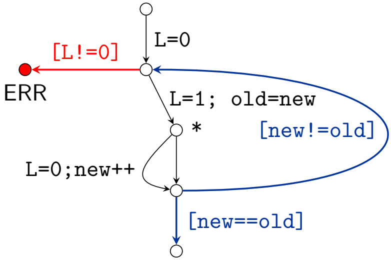
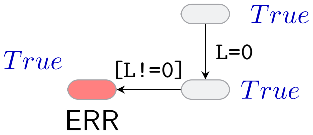


- reachable states ⊆ label



Abstract Reachability Tree



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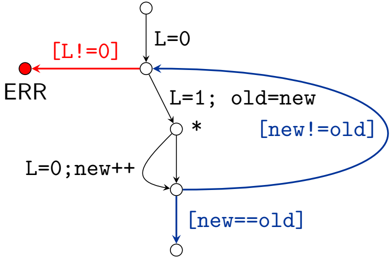

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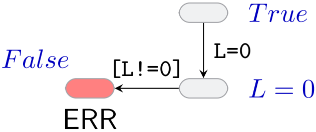

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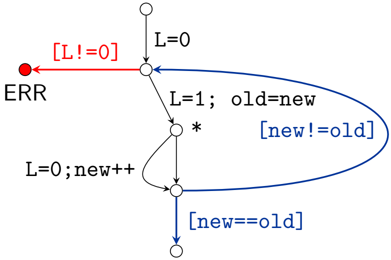

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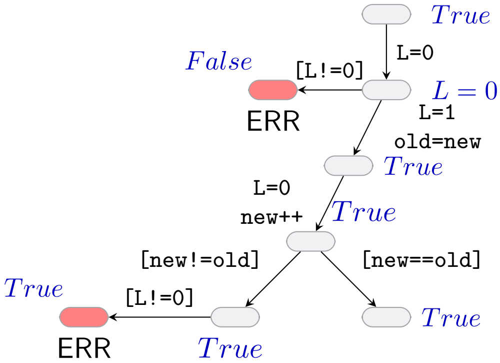
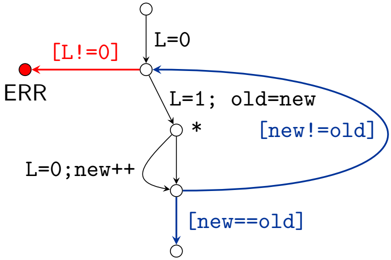


- reachable states $\subseteq$ label



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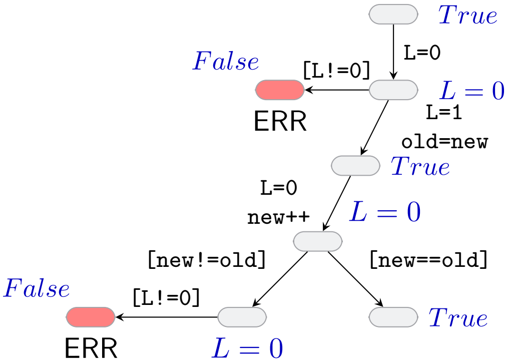

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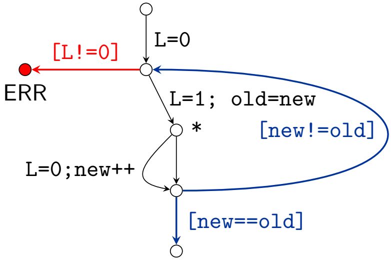

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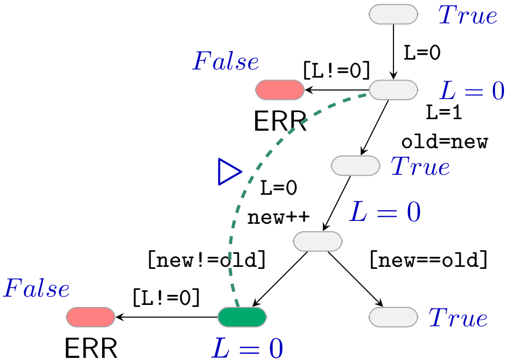

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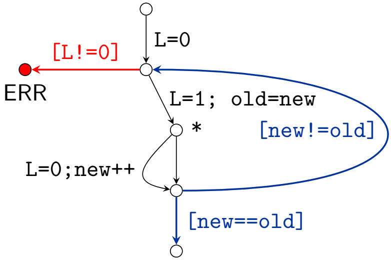

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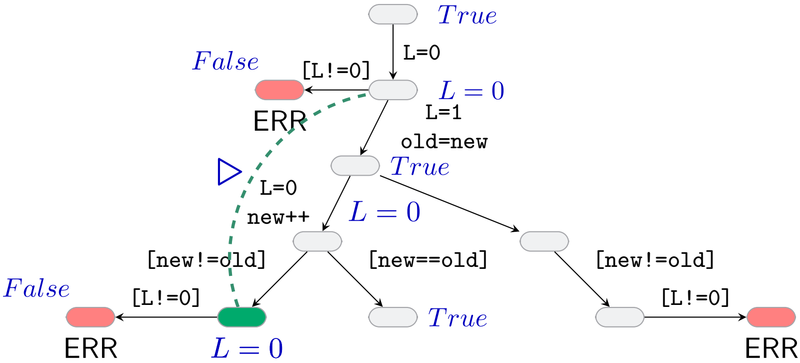

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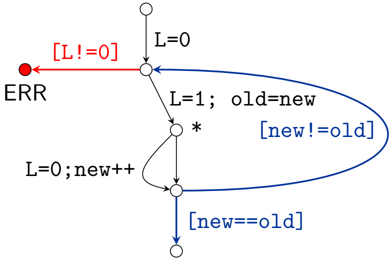

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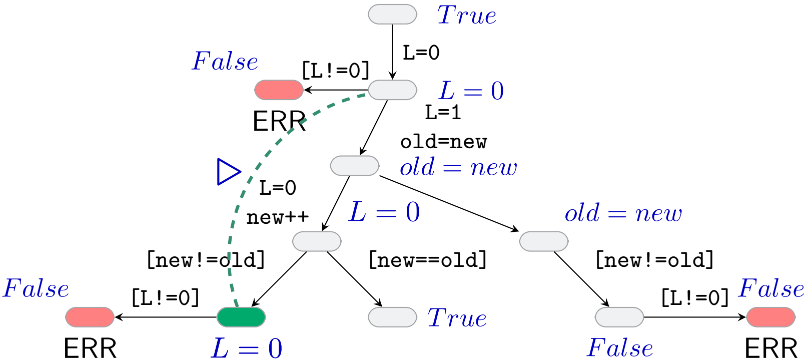
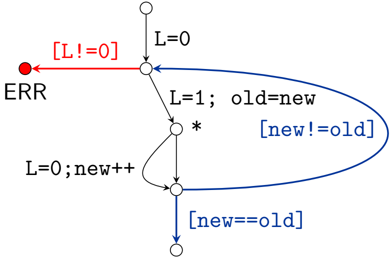


- reachable states ⊆ label
- terminates if all nodes
  - covered
  - or fully expanded



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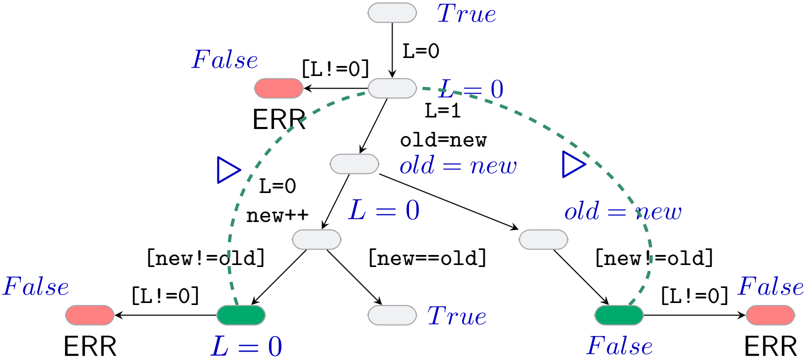
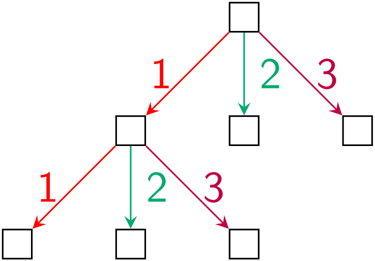


Impact for Multithreaded Software

Naive Impact for Multi-threading

- interleave at every step



threads 1,2,3

Example

`int x=0;`

thread 1	thread 2
`0:  assert(x==0);`	`0:  if(*)`
`1:`	`1:    x=1;`
	`2:  x=0;`
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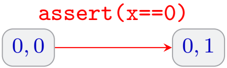

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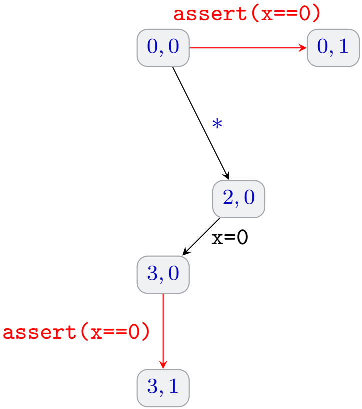

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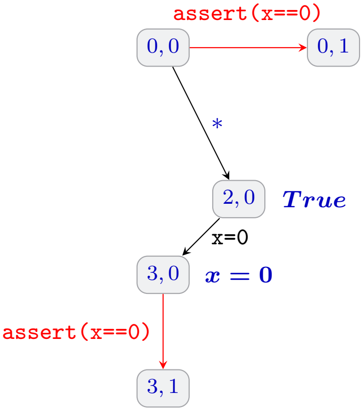

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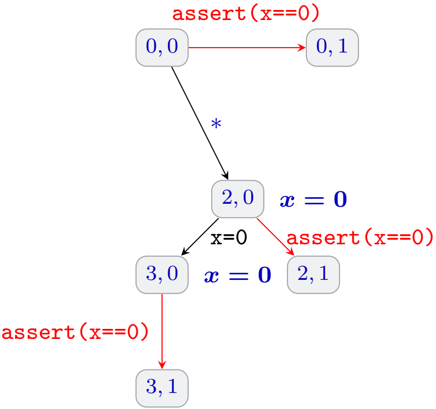

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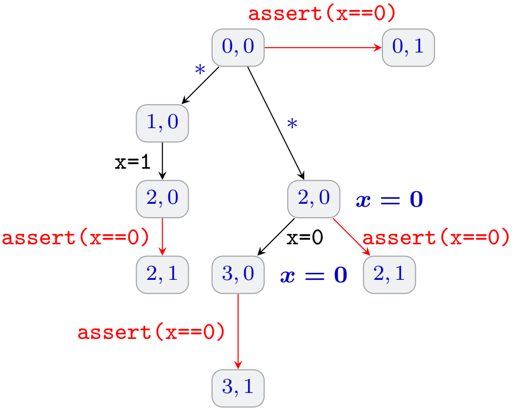

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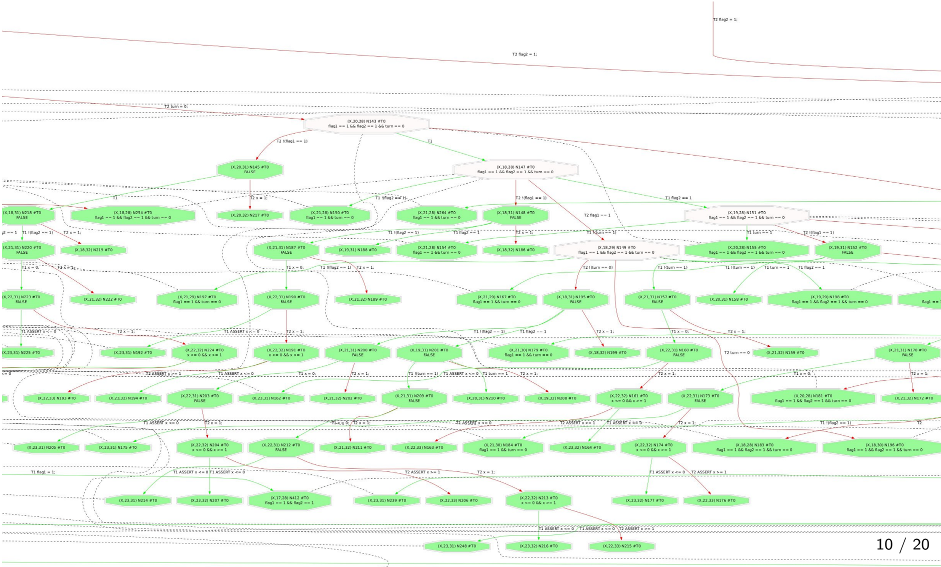
CEX

Naive Impact blows up

ART from a concrete case study (Peterson's algorithm)



Partial-Order Reduction [Godefroid'94, Peled'93, Valmari'90]

avoid unnecessary interleavings resulting in same state

main()	thread 1	thread 2
assume(i!=j);		
v[i]=0; v[j]=0;	A : v[i]=1;	a : v[j]=-2;
pthread_create(T_1);	B : v[i]=v[i]+1;	b : v[j]=v[j]+1;
pthread_create(T_2);	C : v[i]=v[j];	c : v[i]=v[i]+1;
pthread_join(T_1);		
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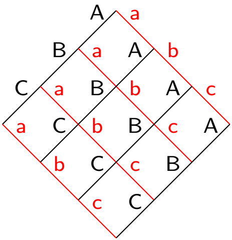
assert(v[j] $\geq$ 0);		



$A \mid\mid a$ and $TID(A) < TID(a)$

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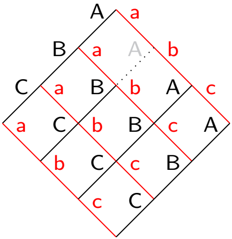

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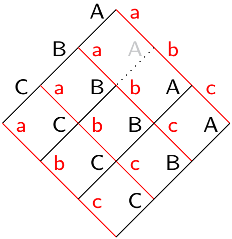

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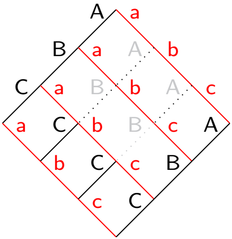

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Algorithm: POR+Impact (First Attempt)

- POR restricts expansion

```
procedure $\textsc{Expand}_{\Diamond}(v)$
    for $T \in \mathcal{T}$ with $\neg\textsc{Skip}_{\Diamond}(v, T)$ do
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Is that sound?

Impact + **POR**

`int x=0;`

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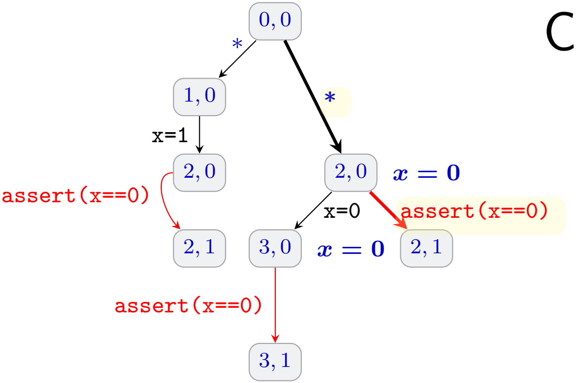
CEX



- $*$ and `assert(x==0)` independent

Impact + POR

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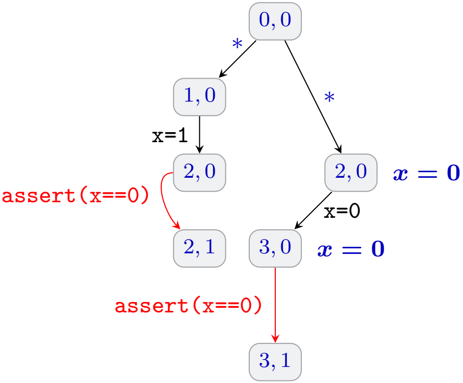

CEX

- $*$ and `assert(x==0)` independent
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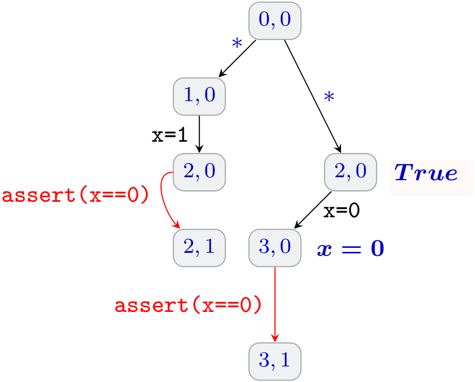

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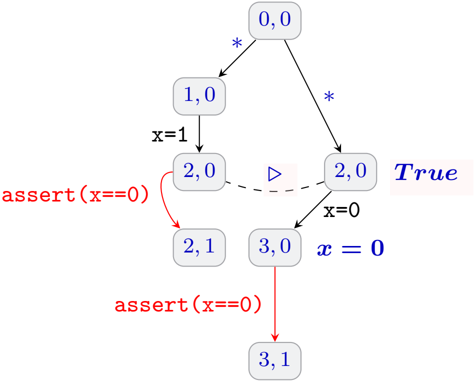

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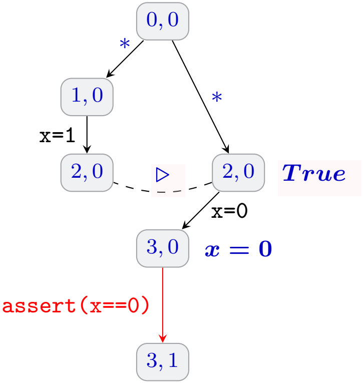

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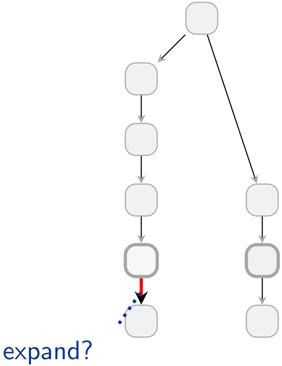
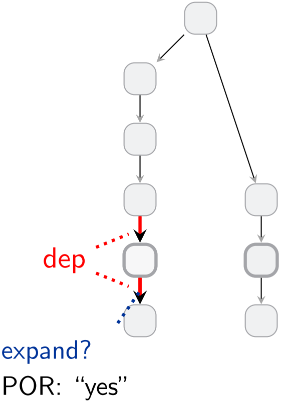
Let's take a step back



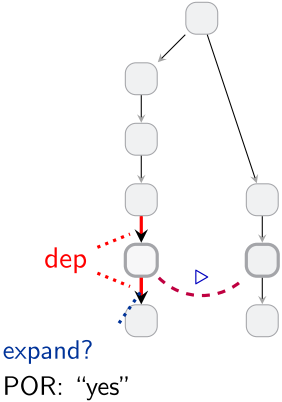
Let's take a step back

- POR inspects node history



Let's take a step back

- POR inspects node history
- covers merge distinct histories



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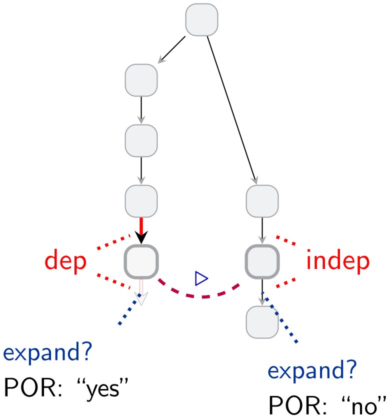

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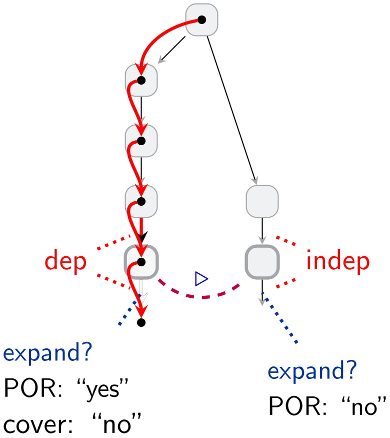
⇒ incomplete: lost program path

  - no corresponding ART path



expand?

POR: “yes”

cover: “no”

expand?

POR: “no”

Let's take a step back

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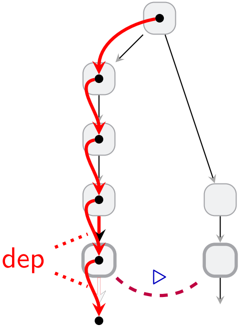
- How to fix this?
  - corresponding path?
  - allow cover edges
  - jump to more abstract node



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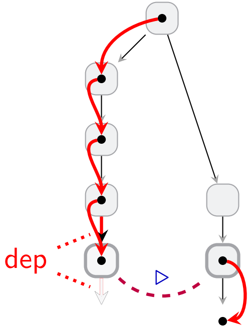
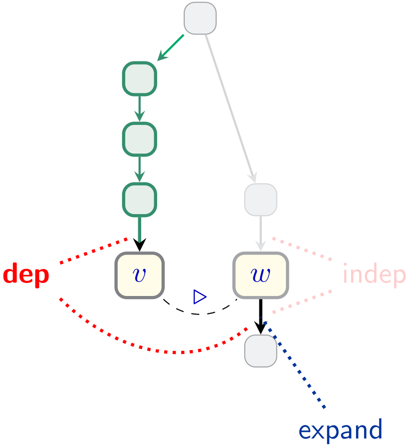


Complete Algorithm

- $v \rhd w$

$\Rightarrow$ consider **both** **histories**

- v's and w's



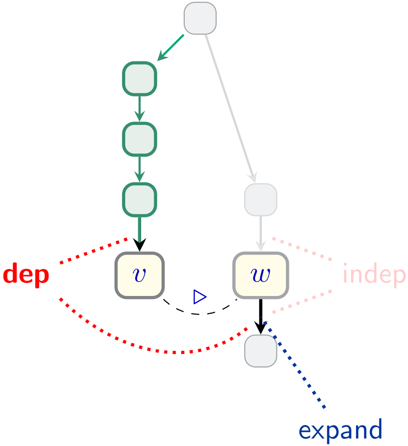
Complete Algorithm

- $v \rhd w$

$\Rightarrow$ consider **both** **histories**

  - v's and w's

- Note: we're still doing POR



Π-completeness

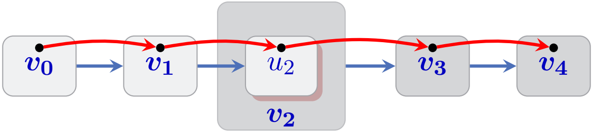
Π determined by POR strategy

Definition (Π-complete ART)

ART $\mathcal{A}$ is Π-complete iff:

for every $\boldsymbol{\pi} \in \prod$, there is a corresponding path $v_0, \ldots, v_n$.

Π-completeness



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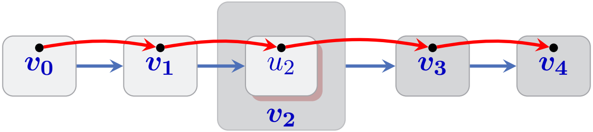

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$\Rightarrow$ **Soundness**

Impara

- C++ implementation
- CBMC frontend
- bit-precise interpolation
    - unsatisfiable cores + weakest preconditions

Impara vs. other tools

	CBMC 4.5	ESMBC	SatAbs	Threader	Impara
technique	BMC	BMC	Pred. Abs.	Pred. Abs.	Interpolation
threads	PO encoding	POR	POR	Modular Reasoning	POR
unbounded loops			✓	✓	✓
bit-precise	✓	✓	✓		✓
weak memory	✓		✓*		✓*

SVCOMP'13 multi-threading benchmarks

program	safe	CBMC	ESBMC	SatAbs	Threader	Impara
`dekker`	y	0.6*	2.2*	0.2	TO	**0.1**
`lamport`	y	12.4*	18.1*	**0.3**	38.1	**0.3**
`peterson`	y	0.2*	2.0*	0.3	4.8	**0.1**
`szymanski`	y	0.5*	4.7*	**0.2**	13.5	**0.2**
`read_write_u`	n	**0.2**	TO	0.8	58.4	0.6
`read_write_s`	y	**0.4**	TO	0.8	58.1	0.9
`time_var_mutex`	y	0.2	110.3	95.4	4.3	**0.1**
`stack_u`	n	1.0	TO	TO	80.6	**0.5**
`stack_s`	y	**33.5**	TO	TO	250.1	38.8

Conclusion

- IMPACT abstraction + POR
    - take-home message: **look at both histories**
- Experiments
    - SVCOMP'13
    - weak memory benchmarks (low-lock algorithms)
        - IMPARA gives correct results
        - which gives us confidence
- Binary & benchmarks at:

`http://www.cprover.org/concurrent-impact/`

Thank you!