Computer Organization and Design, The Hardware/Software Interface, Fourth Edition

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Errata list as of 10/26/09

Chapter		Page #		Description	Correction
Preface		xxi		Email messages to "cod4ebugs@mkp.com" bounce or are undeliverable	Fixed, messages are now delivered to Morgan Kaufmann
1		6		Figure 1.1, vertical axes lacks the indication that the scale is in millions.	Y axis should be labeled millions
1		12		There is no pseudoinstruction for MIPS with the mnemonic "muli" as listed in the middle of Figure 1.3.	"muli" should read "multi"
1		12		Figure 1.3: When decoded, the listed binary machine language only matches the mnemonics of the assembly code and different operand registers are used except for the jr $31 instruction.	Binary patterns at bottom of Fig 1.3 should be: BEFORE "00000000101000010000000000011000" "00000000000011000000110000100001" "10001100011000100000000000000000" "10001100111100100000000000000100" "10101100111100100000000000000000" "10101100011000100000000000000100" "00000011111000000000000000001000" AFTER "00000000101000100000000100011000" "00000000100000100001000001000001" "10001101111000100000000000000000" "10001110000100100000000000000100" "10101110000100100000000000000000" "10101101111000100000000000000100" "00000011111000000000000000001000"
1		49		Figure 1.20, page 49: The column heading Clock cycle time has (seconds x 10^9) as its unit.	Should read (seconds x 10^-9) since the unit should be nanosecond in the description for that figure.
1		61		**Exercise 1.5.3:** Row B shows a total of 1750.	Total should be **2000**
2		101		**Check Yourself:** All choices specify combinations of registers $s0, $s1, and $s2, but either the register numbers used in the diagram should be changed from 8, 9, and 10 to 16, 17, and 18 respectively, or the symbolic register numbers should be changed to $t0, $t1, and $t2.	Add the s's with t's in the choices ($s0 -> $t0, $s1->$t1, $s2->$t2)
2		101		**Check Yourself** problem on p. 101 is buggy as printed.	To make the problem solvable, replace all the $s registers in the alternatives with $t registers. Also change 1 and 3 from "add" to "sub".
2		145		Cannot get 1000 0000_h from 8000_h($gp) where $gp is pointed to 1000 800_h. Likewise, cannot come up with 1000 0020_h from 8020_h($gp).	Should be **-8000_h** and **-7980_h** respectively.
2		221		**Answers to Check Yourself:** inaccurate reference to Section 2.6, page 104	Should read **Section 26, page 105**.
3		272		On page 235, the text refers to Hi and Lo "registers". On page 272, the text confusingly implies that Hi and Lo are not registers.	Text should read: "The x86 has regular multiply and divide instructions that operate entirely on its normal registers, unlike the reliance on separate Hi and Lo registers in MIPS."
3		280		On page 280, the text states that "All instructions are listed [in Figure 3.26] that were responsible for at least 0.3% of the instruction executed." The caption of Figure 3.26 states that the cutoff is 1%. The contents of Figure 3.26 reveal that even a 0.3% cutoff is violated.	Change all values to 0.2%.
3		283		Section 3.10 should refer to the 18th IEEE Symposium on Computer Arithmetic.	Will be updated in future printing.
3		297		**Answers to Check Yourself:** Last line on page 297 refers to Section 3.4	The correct section is 3.5.

4		315		In Figure 4.11, it appears as if the Zero output of the main ALU goes into the data memory. At this point in the text, it should go off to nowhere. (Figure 4.9 shows it as going to the branch control logic, but the control hasn't been introduced yet and Figure 4.11 is a datapath diagram anyway.)	Delete the arrow that goes from Zero to Data Memory
4		331		Top of Figure 4.25: The gray for the "storer" is missing (e.g. from 7:30 PM to 8 PM).	Every 4th slot in the upper figure should be dark gray. 730-8PM, 9:30-10PM. 11:30-12PM, 1:30-2AM
4		339		The first sentence on page 339 refers to the "following" code segment. The word should be "preceding" (or equivalent).	Will be updated in future printing.
4		369		Page 369, first sentence at the top of the page reads: ... ,provided it is not register 0, then steer the multiplexor to pick the value instead from the pipeline register EX/MEM.	Should read: ... ,provided it is not register 0, then steer the multiplexor to pick the value instead from the pipeline register MEM/WB.
4		388		Page 388, EXAMPLE The last two instructions in the code are: 80000180hex sw $25, 1000($0) 80000184hex sw $26, 1004($0)	The code should read: 80000180hex sw $26, 1000($0) 80000184hex sw $27, 1004($0) The registers $26 and $27 are reserved for the kernel.
4		389		Page 389, Figure 4.67 In the lower drawing, the instruction displayed in the "Fetch" stage is: sw $25, 1000($0)	The correct version should be: sw $26, 1000($0)
App C		C-6		Inverse Laws: $A \cdot \overline{A} = 1$.	Inverse Laws: $A \cdot \overline{A} = 0$
General				The book refers to SPEC2006, SPEC2000 etc.	The correct references are SPEC CPU2006 or SPEC CPU2000. Note that this typo occurs in both the printed text and in the accompanying CD.