

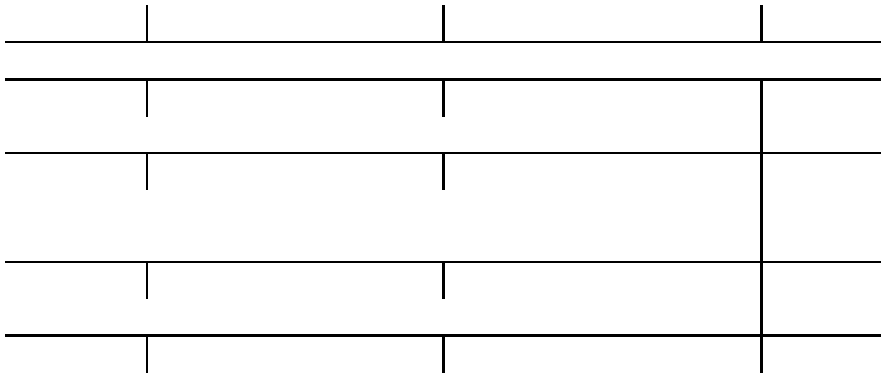
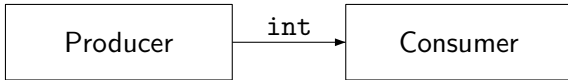
# A Temporal Language for SystemC

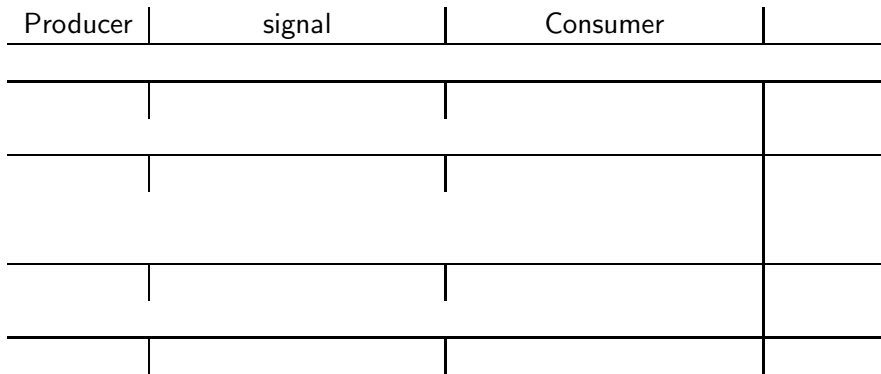
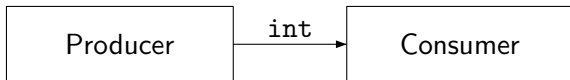
Deian Tabakov, Moshe Y. Vardi, Gila Kamhi, Eli Singerman

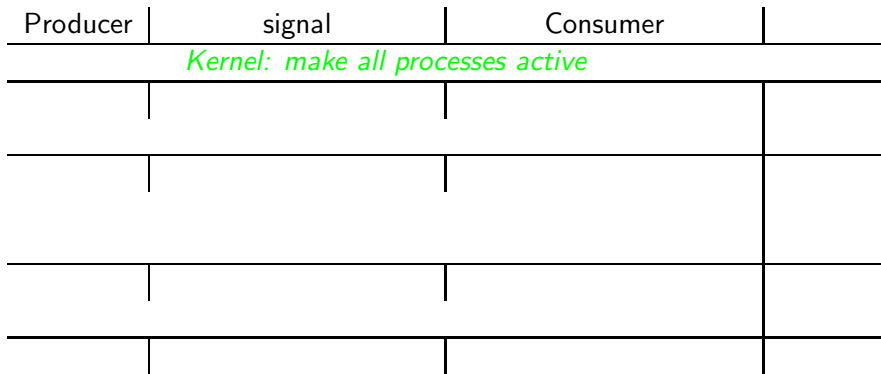
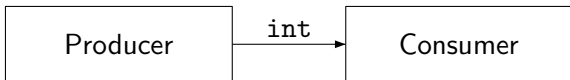
Rice University  
Houston, TX

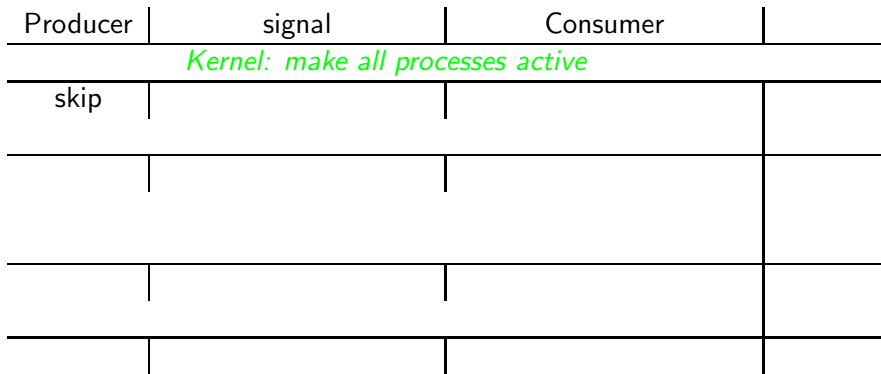
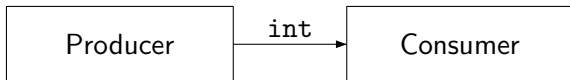
November 20, 2008

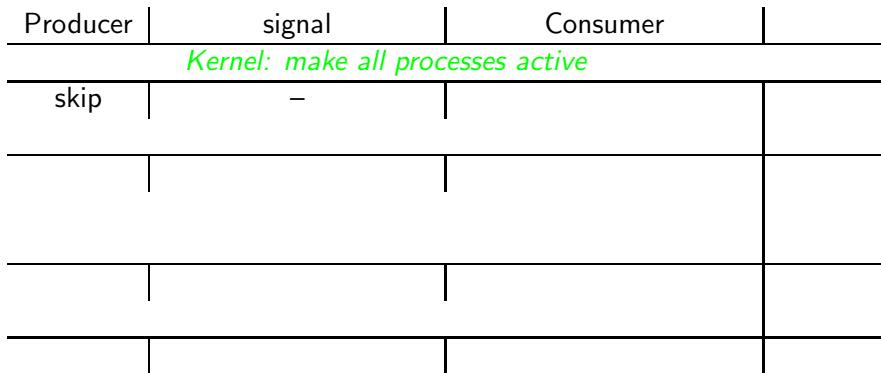
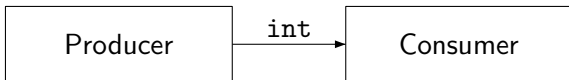
- System-level modeling language: C++ based, OO used for abstraction, modularity, and compositionality
- Rich set of data types: C++ plus hardware
- Rich set of libraries for modeling at different levels: signals, FIFOs, TLM (transaction-level modeling)
- Processes; SC\_METHODs and SC\_THREADS
- Simulation kernel – event driven
  - Processes run until suspension
  - Processes notify events (immediate, delta, timed)
  - Notified events wake suspended processes
  - Kernel manages scheduling of processes

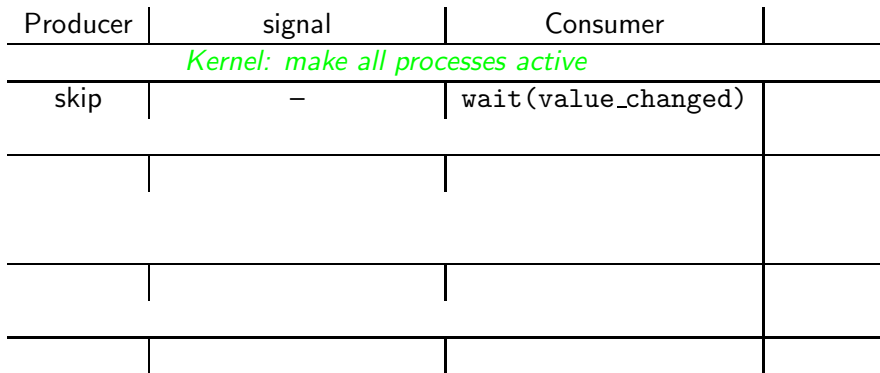
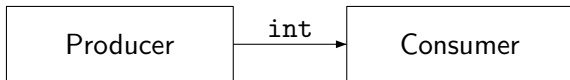




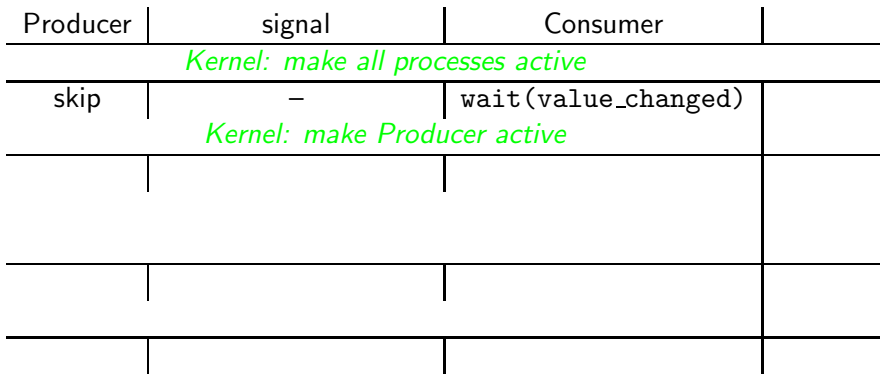
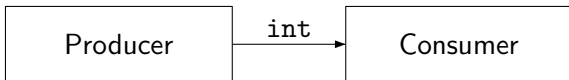


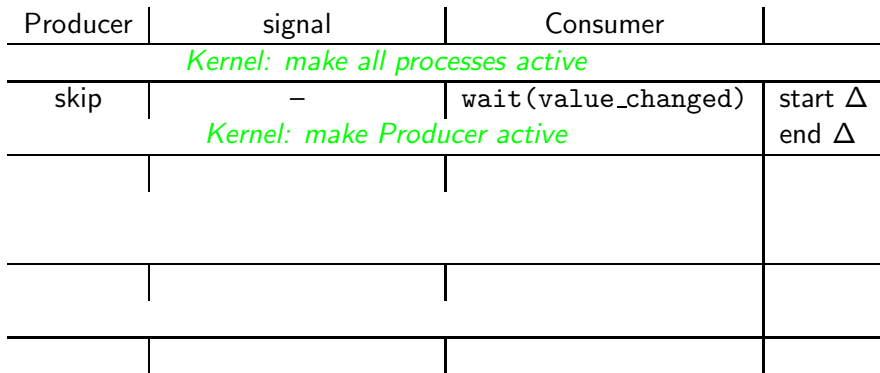
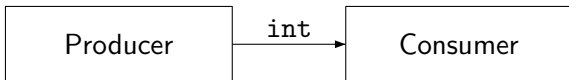


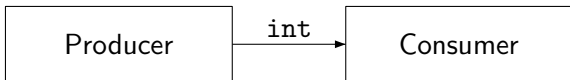




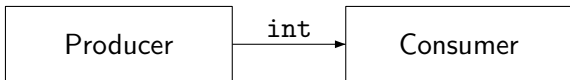




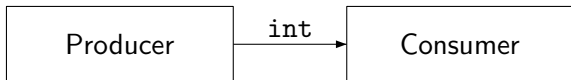




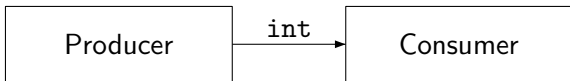
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<i>Kernel: make all processes active</i>			
skip	–	wait(value_changed)	start $\Delta$
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write(1)			end $\Delta$



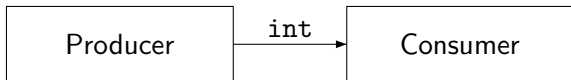
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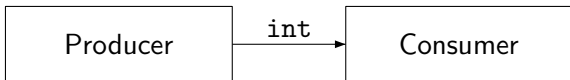
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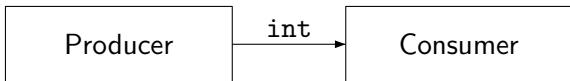


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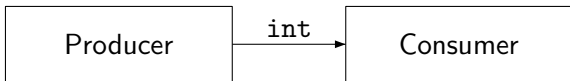


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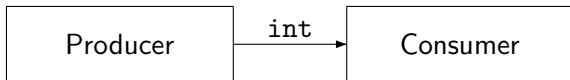




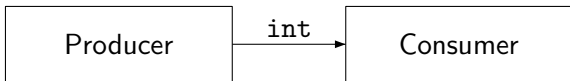
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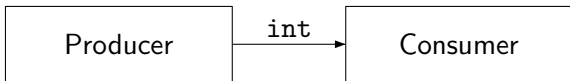
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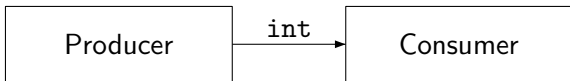
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write(2)	1		



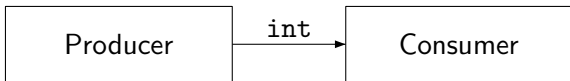
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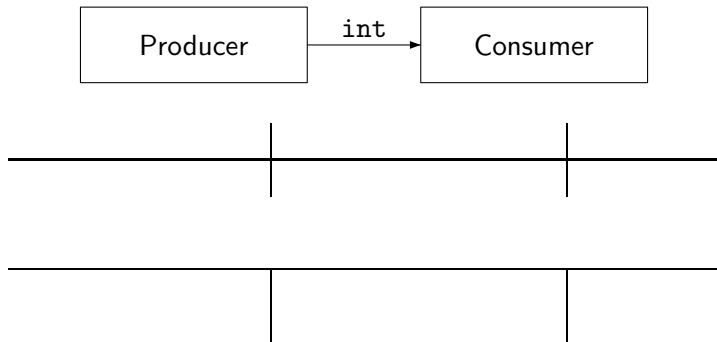
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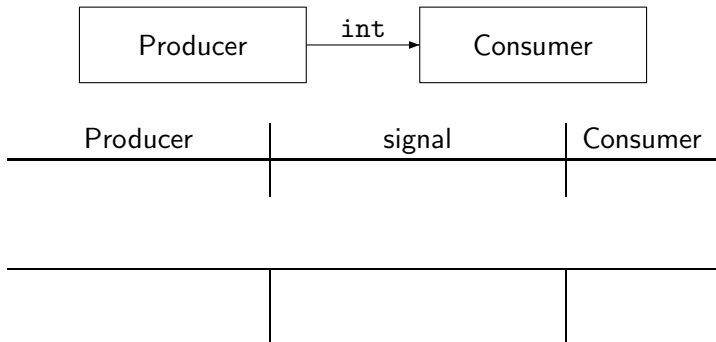
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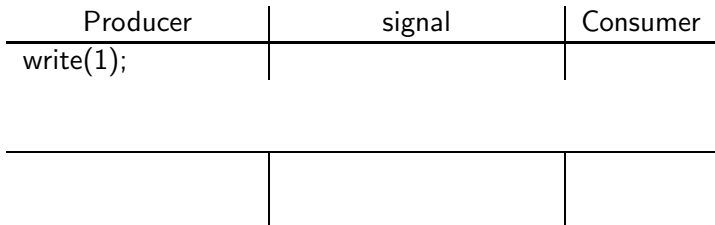
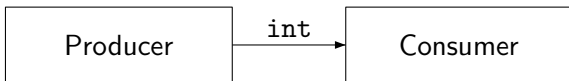


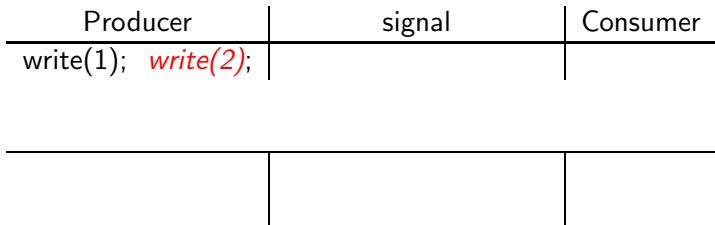
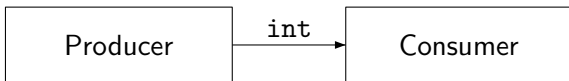
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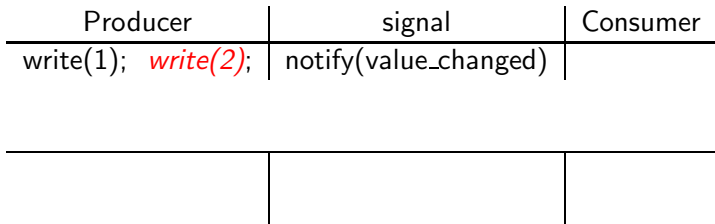
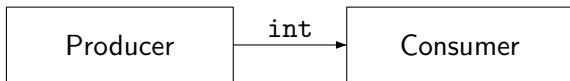


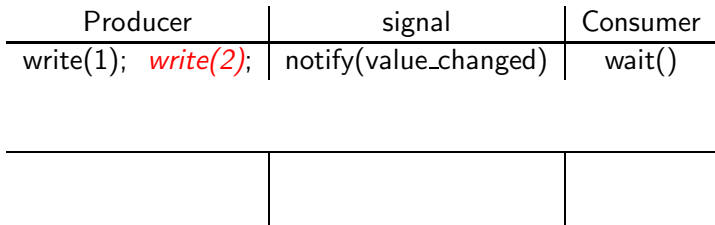
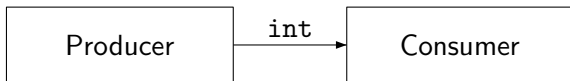


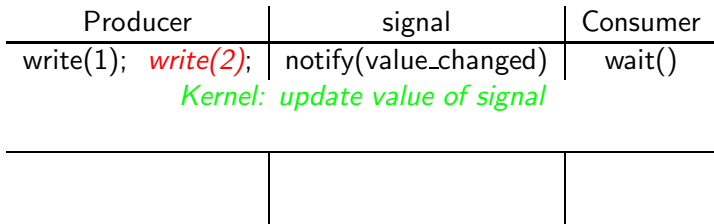
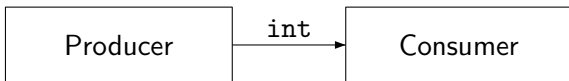


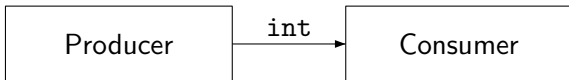




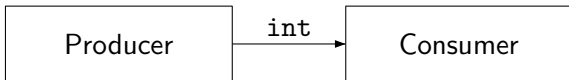






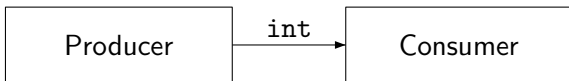


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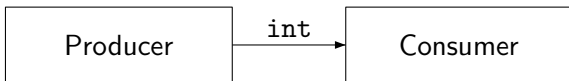


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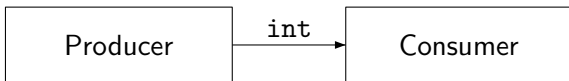




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**Desideratum:** Express properties at sub- $\Delta$ -cycle resolution

## Three types of `sc_event`

- Immediate events have an immediate effect
  - Can cause deadlocks
- Delta events
  - Accumulated while processes are running
  - Have an effect only after all immediate events
- Timed events
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**Key observation:** No canonical notion of a cycle

# “Useful” SystemC properties: examples

- A signal is written to at most once
- The value of variable “balance” is always equal to “deposits” - “withdrawals”
- “Request”  $\rightarrow$  within[3] “grant”

- A signal is written to at most once within ...
  - ... execution of an individual process
  - ... a complete delta cycle
  - ... between two clock ticks
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  - ... in all stable states (no process running)
  - ... at beginning of each delta cycle
  - ... at each clock tick
- “Request”  $\rightarrow$  within[3] “grant”



# “Useful” SystemC properties: examples

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  - ... in all stable states (no process running)
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  - ... at each clock tick
- “Request”  $\rightarrow$  within[3] “grant”
  - Within 3 “what”?

- Recognize of SystemC's ability to bridge different levels of abstraction
  - Specify clockless and clocked modules working together
  - Systematic way to refine properties as design is refined
- Recognize SystemC's unique simulation semantics
  - Expose notification of events
  - Allow different levels temporal resolution
- Give precise definition of a trace
  - No existing language addresses this issue

*Augment* existing languages (PSL/SVA), not develop a new one

- Define a precise notion of a trace of execution for SystemC models
- Identify important Boolean properties relevant to execution or specification of SystemC

Plug-in our framework in existing specification languages

- Richer set of Boolean properties
- Much more flexible temporal resolution: by leveraging the ability of temporal languages to use Boolean expressions as clock expressions

Why deal with the kernel?

- Many important properties at sub- $\Delta$  cycle resolution
- Adapt specifications to level of abstraction

Example: Invariance properties, say, ALWAYS  $x > 10$

- Must hold at *all* times
- Must hold when processes suspend
- Must hold at delta-cycle boundary
- Must hold at clock-cycle boundary

This is possible *only* if we require the kernel to expose information about its internal state.

## Complications

- Many implementations
- 15K lines of code (in reference implementation)
- What is the right abstraction?

## Our solution

- Follow the LRM
- Abstract kernel's implementations, but expose semantics
- Enable coarser abstractions via clock expression
- Expose event notifications

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**Bottom line:** expose kernel state and event notifications

## Code (Consumer.h)

```
while ( true ) {  
    wait(in.value_changed_event);  
    int x = in.read();  
    int y = f(x); // some one-way function  
    float z = 10/y;  
    ...  
}
```

## Code (Consumer.h)

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    ...  
}
```

**Desideratum:** Statement-level assertions



## Our approach

- Each statement defines a new state
- Expose protected and private variables (white box)
- Expose properties of function calls (arguments and return value)
- Expose properties of SystemC primitives (e.g.. number of elements in a `sc_fifo`)

- A SystemC trace is a sequence of states corresponding to execution of model
- Expose alternation of control
  - kernel
  - user code
  - libraries
- “large-step semantics” vs “small-step semantics”
  - $y = (x++) + (x--);$

- $\text{Balance} = \text{Deposits} - \text{Withdrawals}$

- Balance = Deposits - Withdrawals
  - At end of all  $\Delta$  cycles

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  - Every 10 clock cycles

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  - When no process is running
  - At end of a particular process
  - When a particular function returns
- Process A must execute
  - Every delta cycle
  - Every clock cycle
  - Every 10 clock cycles
  - Only once

HW/SW co-design: Treating SystemC as software

- Pre- and post- conditions
- Properties about the actual parameters of function calls
- Properties about the return values of function calls
- Library state only via APIs

Relevant prior work

- SLIC and Blast allow the specification of C interfaces via specifying properties related to function calls
- Blast allows access to syntax of executing statements

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**Key Observation:** Expose the syntax

## Summary

- Precise definition of an execution trace
- A family of expressions that enrich the Boolean layer of any specification language
- Mechanism for sampling underlying trace at different levels of abstraction without changing language
- SystemC as software

## Discussion

- Framework applicable to formal and dynamic verification
- Our approach requires very small modifications of SystemC kernel
- Current focus: translate specifications into SystemC monitors and instrument user code

## Appendix



# Semantics of SystemC Simulation I

- 1:  $PC \leftarrow$  all primitive channels
- 2:  $P \leftarrow$  all processes
- 3:  $R \leftarrow P$  /\* Set of runnable processes \*/
- 4:  $D \leftarrow \emptyset$  /\* Set of pending delta notifications \*/
- 5:  $U \leftarrow \emptyset$  /\* Set of update requests \*/
- 6:  $T \leftarrow \emptyset$  /\* Set of pending timed notifications \*/
- 7: **for all**  $chan \in PC$  **do**
- 8:     **run**  $chan.update()$
- 9: **for all**  $p \in R$  **do**
- 10:    **if**  $p$  is initializable **then**
- 11:      **run**  $p$
- 12: **for all**  $d \in D$  **do**
- 13:     $D \leftarrow D \setminus d$
- 14: **for all**  $p \in P$  **do**
- 15:    **if**  $n$  triggers  $p$  **then**
- 16:       $R \leftarrow R \cup p$

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17: repeat
18:   while  $R \neq \emptyset$  do /* New delta cycle begins */
19:     for all  $r \in R$  do
20:        $R \leftarrow R \setminus r$ 
21:       run  $r$  until it invokes wait() or returns
22:     for all  $chan \in U$  do /* Update phase */
23:       run  $chan.update()$ 
24:     for all  $d \in D$  do /* Delta notification phase */
25:        $D \leftarrow D \setminus d$ 
26:       for all  $p \in P$  do
27:         if  $d$  triggers  $p$  then
28:            $R \leftarrow R \cup p$  /*  $p$  is now runnable */
29:   /* End of delta cycle */
```

```
30:  if  $T \neq \emptyset$  then  
31:      Advance clock to earliest timed delay  $t$ .  
32:       $T \leftarrow T \setminus t$   
33:      for all  $p \in P$  do  
34:          if  $t$  triggers  $p$  then  
35:               $R \leftarrow R \cup p$  /*  $p$  is now runnable */  
36:  until end of simulation
```

Our approach: keep track of current phase

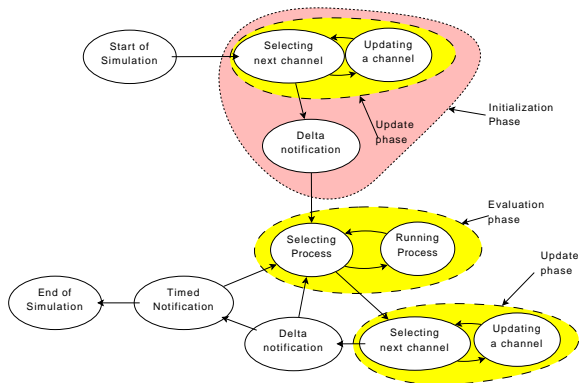


Figure: Captured Kernel States

# Kernel States in Moy's Abstraction

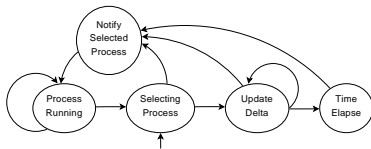


Figure: Kernel states proposed by Moy et al.