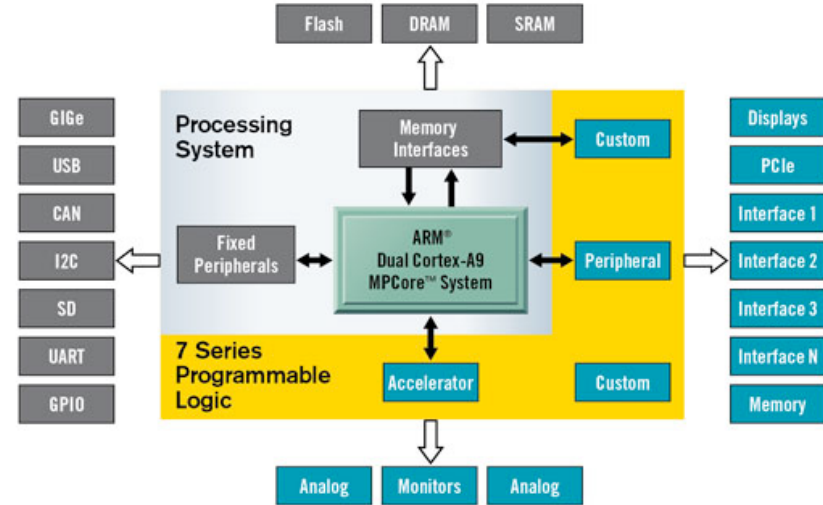
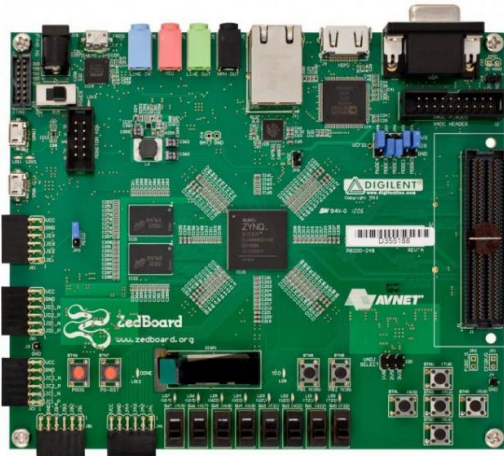


# *BLIS* A ~~Brief~~ Affair with FPGAs

Zhipeng Zhao, Qi Guo, Tze Meng Low  
Carnegie Mellon University

# FPGAs

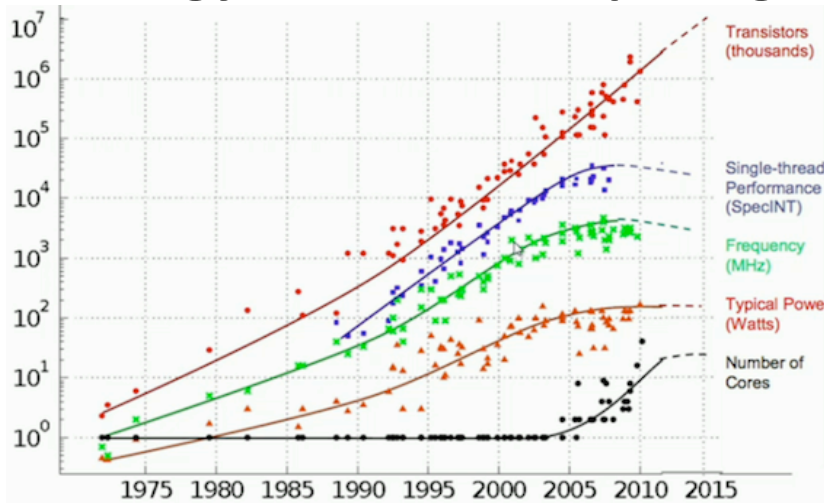
## System on Chip (SoC)



## DIY Hardware

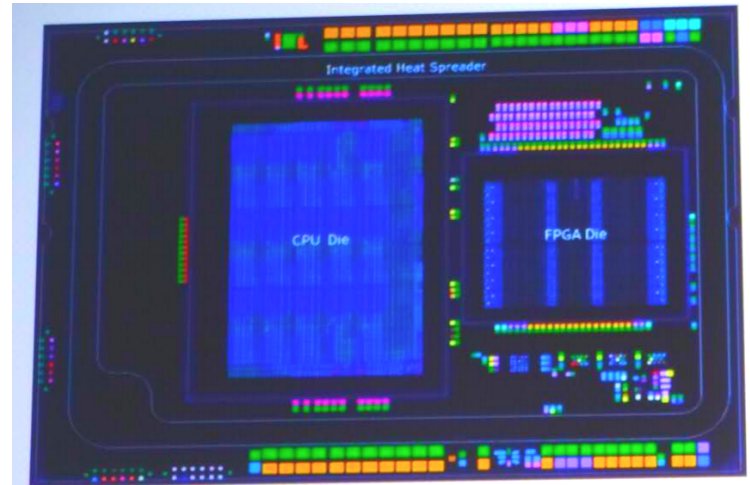


## Energy-efficient computing



Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten  
Dotted line extrapolations by C. Moore

## Heterogeneous architecture



Broadwell + Arria 10 GX MCP

## Used in Datacenters and Cloud Services



# High Level Synthesis

## High Level Synthesis (HLS)

**Altera® SDK**  
for OpenCL



C / OpenCL



RTL

```

100  complete_val[1] for (int k = 0; k < M; k++)
101  {
102  @include
103  for (int l = 0; l < M; l++)
104  {
105  @include
106  }
107  }
108  }
109  }
110  }
111  }
112  }
113  }
114  }
115  }
116  }
117  }
118  }
119  }
120  }
121  }
122  }
123  }
124  }
125  }
126  }
127  }
128  }
129  }
130  }
131  }
132  }
133  }
134  }
135  }
136  }
137  }
138  }
139  }
140  }
141  }
142  }
143  }
144  }
145  }
146  }
147  }
148  }
149  }
150  }
151  }
152  }
153  }
154  }
155  }
156  }
157  }
158  }
159  }
160  }
161  }
162  }
163  }
164  }
165  }
166  }
167  }
168  }
169  }
170  }
171  }
172  }
173  }
174  }
175  }
176  }
177  }
178  }
179  }
180  }
181  }
182  }
183  }
184  }
185  }
186  }
187  }
188  }
189  }
190  }
191  }
192  }
193  }
194  }
195  }
196  }
197  }
198  }
199  }
200  }
201  }
202  }
203  }
204  }
205  }
206  }
207  }
208  }
209  }
210  }
211  }
212  }
213  }
214  }
215  }
216  }
217  }
218  }
219  }
220  }
221  }
222  }
223  }
224  }
225  }
226  }
227  }
228  }
229  }
230  }
231  }
232  }
233  }
234  }
235  }
236  }
237  }
238  }
239  }
240  }
241  }
242  }
243  }
244  }
245  }
246  }
247  }
248  }
249  }
250  }
251  }
252  }
253  }
254  }
255  }
256  }
257  }
258  }
259  }
260  }
261  }
262  }
263  }
264  }
265  }
266  }
267  }
268  }
269  }
270  }
271  }
272  }
273  }
274  }
275  }
276  }
277  }
278  }
279  }
280  }
281  }
282  }
283  }
284  }
285  }
286  }
287  }
288  }
289  }
290  }
291  }
292  }
293  }
294  }
295  }
296  }
297  }
298  }
299  }
300  }
301  }
302  }
303  }
304  }
305  }
306  }
307  }
308  }
309  }
310  }
311  }
312  }
313  }
314  }
315  }
316  }
317  }
318  }
319  }
320  }
321  }
322  }
323  }
324  }
325  }
326  }
327  }
328  }
329  }
330  }
331  }
332  }
333  }
334  }
335  }
336  }
337  }
338  }
339  }
340  }
341  }
342  }
343  }
344  }
345  }
346  }
347  }
348  }
349  }
350  }
351  }
352  }
353  }
354  }
355  }
356  }
357  }
358  }
359  }
360  }
361  }
362  }
363  }
364  }
365  }
366  }
367  }
368  }
369  }
370  }
371  }
372  }
373  }
374  }
375  }
376  }
377  }
378  }
379  }
380  }
381  }
382  }
383  }
384  }
385  }
386  }
387  }
388  }
389  }
390  }
391  }
392  }
393  }
394  }
395  }
396  }
397  }
398  }
399  }
400  }
401  }
402  }
403  }
404  }
405  }
406  }
407  }
408  }
409  }
410  }
411  }
412  }
413  }
414  }
415  }
416  }
417  }
418  }
419  }
420  }
421  }
422  }
423  }
424  }
425  }
426  }
427  }
428  }
429  }
430  }
431  }
432  }
433  }
434  }
435  }
436  }
437  }
438  }
439  }
440  }
441  }
442  }
443  }
444  }
445  }
446  }
447  }
448  }
449  }
450  }
451  }
452  }
453  }
454  }
455  }
456  }
457  }
458  }
459  }
460  }
461  }
462  }
463  }
464  }
465  }
466  }
467  }
468  }
469  }
470  }
471  }
472  }
473  }
474  }
475  }
476  }
477  }
478  }
479  }
480  }
481  }
482  }
483  }
484  }
485  }
486  }
487  }
488  }
489  }
490  }
491  }
492  }
493  }
494  }
495  }
496  }
497  }
498  }
499  }
500  }
501  }
502  }
503  }
504  }
505  }
506  }
507  }
508  }
509  }
510  }
511  }
512  }
513  }
514  }
515  }
516  }
517  }
518  }
519  }
520  }
521  }
522  }
523  }
524  }
525  }
526  }
527  }
528  }
529  }
530  }
531  }
532  }
533  }
534  }
535  }
536  }
537  }
538  }
539  }
540  }
541  }
542  }
543  }
544  }
545  }
546  }
547  }
548  }
549  }
550  }
551  }
552  }
553  }
554  }
555  }
556  }
557  }
558  }
559  }
560  }
561  }
562  }
563  }
564  }
565  }
566  }
567  }
568  }
569  }
570  }
571  }
572  }
573  }
574  }
575  }
576  }
577  }
578  }
579  }
580  }
581  }
582  }
583  }
584  }
585  }
586  }
587  }
588  }
589  }
590  }
591  }
592  }
593  }
594  }
595  }
596  }
597  }
598  }
599  }
600  }
601  }
602  }
603  }
604  }
605  }
606  }
607  }
608  }
609  }
610  }
611  }
612  }
613  }
614  }
615  }
616  }
617  }
618  }
619  }
620  }
621  }
622  }
623  }
624  }
625  }
626  }
627  }
628  }
629  }
630  }
631  }
632  }
633  }
634  }
635  }
636  }
637  }
638  }
639  }
640  }
641  }
642  }
643  }
644  }
645  }
646  }
647  }
648  }
649  }
650  }
651  }
652  }
653  }
654  }
655  }
656  }
657  }
658  }
659  }
660  }
661  }
662  }
663  }
664  }
665  }
666  }
667  }
668  }
669  }
670  }
671  }
672  }
673  }
674  }
675  }
676  }
677  }
678  }
679  }
680  }
681  }
682  }
683  }
684  }
685  }
686  }
687  }
688  }
689  }
690  }
691  }
692  }
693  }
694  }
695  }
696  }
697  }
698  }
699  }
700  }
701  }
702  }
703  }
704  }
705  }
706  }
707  }
708  }
709  }
710  }
711  }
712  }
713  }
714  }
715  }
716  }
717  }
718  }
719  }
720  }
721  }
722  }
723  }
724  }
725  }
726  }
727  }
728  }
729  }
730  }
731  }
732  }
733  }
734  }
735  }
736  }
737  }
738  }
739  }
740  }
741  }
742  }
743  }
744  }
745  }
746  }
747  }
748  }
749  }
750  }
751  }
752  }
753  }
754  }
755  }
756  }
757  }
758  }
759  }
760  }
761  }
762  }
763  }
764  }
765  }
766  }
767  }
768  }
769  }
770  }
771  }
772  }
773  }
774  }
775  }
776  }
777  }
778  }
779  }
780  }
781  }
782  }
783  }
784  }
785  }
786  }
787  }
788  }
789  }
790  }
791  }
792  }
793  }
794  }
795  }
796  }
797  }
798  }
799  }
800  }
801  }
802  }
803  }
804  }
805  }
806  }
807  }
808  }
809  }
810  }
811  }
812  }
813  }
814  }
815  }
816  }
817  }
818  }
819  }
820  }
821  }
822  }
823  }
824  }
825  }
826  }
827  }
828  }
829  }
830  }
831  }
832  }
833  }
834  }
835  }
836  }
837  }
838  }
839  }
840  }
841  }
842  }
843  }
844  }
845  }
846  }
847  }
848  }
849  }
850  }
851  }
852  }
853  }
854  }
855  }
856  }
857  }
858  }
859  }
860  }
861  }
862  }
863  }
864  }
865  }
866  }
867  }
868  }
869  }
870  }
871  }
872  }
873  }
874  }
875  }
876  }
877  }
878  }
879  }
880  }
881  }
882  }
883  }
884  }
885  }
886  }
887  }
888  }
889  }
890  }
891  }
892  }
893  }
894  }
895  }
896  }
897  }
898  }
899  }
900  }
901  }
902  }
903  }
904  }
905  }
906  }
907  }
908  }
909  }
910  }
911  }
912  }
913  }
914  }
915  }
916  }
917  }
918  }
919  }
920  }
921  }
922  }
923  }
924  }
925  }
926  }
927  }
928  }
929  }
930  }
931  }
932  }
933  }
934  }
935  }
936  }
937  }
938  }
939  }
940  }
941  }
942  }
943  }
944  }
945  }
946  }
947  }
948  }
949  }
950  }
951  }
952  }
953  }
954  }
955  }
956  }
957  }
958  }
959  }
960  }
961  }
962  }
963  }
964  }
965  }
966  }
967  }
968  }
969  }
970  }
971  }
972  }
973  }
974  }
975  }
976  }
977  }
978  }
979  }
980  }
981  }
982  }
983  }
984  }
985  }
986  }
987  }
988  }
989  }
990  }
991  }
992  }
993  }
994  }
995  }
996  }
997  }
998  }
999  }
1000  }
    
```

**Performance Estimates**

Timing (ns)

Summary	Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.41	1.25	

Latency (clock cycles)

Summary	Latency	Interval	Type		
	min	max	min	max	Type
	10979	10979	10980	10980	none

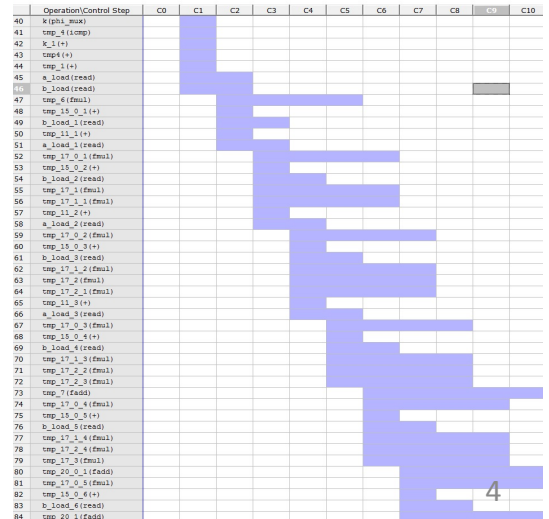
Detail

- Instance
- Loop

**Utilization Estimates**

Summary

Name	BRAM_18K	DSP48E	FF	LUT
Expression	-	-	0	2
FIFO	-	-	-	-
Instance	0	20	5389	5729
Memory	-	-	-	-
Multiplexer	-	-	-	1269
Register	-	-	2350	-
<b>Total</b>	<b>0</b>	<b>20</b>	<b>7739</b>	<b>7000</b>
<b>Available</b>	<b>280</b>	<b>220</b>	<b>106400</b>	<b>53200</b>
<b>Utilization (%)</b>	<b>0</b>	<b>9</b>	<b>7</b>	<b>13</b>



# High Level Synthesis

C / OpenCL



High Level Synthesis  
(HLS)

**Altera® SDK**  
for OpenCL



RTL

```

100  complete_row[0] for (int k = 0; k < M; k++)
101  {
102  for (int l = 0; l < M; l++)
103  {
104  for (int i = 0; i < M; i++)
105  {
106  tmp[i][k] += (float)A[i][l]*B[l][k];
107  }
108  }
109  }
110  }
111  }
112  }
113  }
114  }
115  }
116  }
117  }
118  }
119  }
120  }
121  }
122  }
123  }
124  }
125  }
126  }
127  }
128  }
129  }
130  }
131  }
132  }
133  }
134  }
135  }
136  }
137  }
138  }
139  }
140  }
141  }
142  }
143  }
144  }
145  }
146  }
147  }
148  }
149  }
150  }
151  }
152  }
153  }
154  }
155  }
156  }
157  }
158  }
159  }
160  }
161  }
162  }
163  }
164  }
165  }
166  }
167  }
168  }
169  }
170  }
171  }
172  }
173  }
174  }
175  }
176  }
177  }
178  }
179  }
180  }
181  }
182  }
183  }
184  }
185  }
186  }
187  }
188  }
189  }
190  }
191  }
192  }
193  }
194  }
195  }
196  }
197  }
198  }
199  }
200  }
201  }
202  }
203  }
204  }
205  }
206  }
207  }
208  }
209  }
210  }
211  }
212  }
213  }
214  }
215  }
216  }
217  }
218  }
219  }
220  }
221  }
222  }
223  }
224  }
225  }
226  }
227  }
228  }
229  }
230  }
231  }
232  }
233  }
234  }
235  }
236  }
237  }
238  }
239  }
240  }
241  }
242  }
243  }
244  }
245  }
246  }
247  }
248  }
249  }
250  }
251  }
252  }
253  }
254  }
255  }
256  }
257  }
258  }
259  }
260  }
261  }
262  }
263  }
264  }
265  }
266  }
267  }
268  }
269  }
270  }
271  }
272  }
273  }
274  }
275  }
276  }
277  }
278  }
279  }
280  }
281  }
282  }
283  }
284  }
285  }
286  }
287  }
288  }
289  }
290  }
291  }
292  }
293  }
294  }
295  }
296  }
297  }
298  }
299  }
300  }
301  }
302  }
303  }
304  }
305  }
306  }
307  }
308  }
309  }
310  }
311  }
312  }
313  }
314  }
315  }
316  }
317  }
318  }
319  }
320  }
321  }
322  }
323  }
324  }
325  }
326  }
327  }
328  }
329  }
330  }
331  }
332  }
333  }
334  }
335  }
336  }
337  }
338  }
339  }
340  }
341  }
342  }
343  }
344  }
345  }
346  }
347  }
348  }
349  }
350  }
351  }
352  }
353  }
354  }
355  }
356  }
357  }
358  }
359  }
360  }
361  }
362  }
363  }
364  }
365  }
366  }
367  }
368  }
369  }
370  }
371  }
372  }
373  }
374  }
375  }
376  }
377  }
378  }
379  }
380  }
381  }
382  }
383  }
384  }
385  }
386  }
387  }
388  }
389  }
390  }
391  }
392  }
393  }
394  }
395  }
396  }
397  }
398  }
399  }
400  }
401  }
402  }
403  }
404  }
405  }
406  }
407  }
408  }
409  }
410  }
411  }
412  }
413  }
414  }
415  }
416  }
417  }
418  }
419  }
420  }
421  }
422  }
423  }
424  }
425  }
426  }
427  }
428  }
429  }
430  }
431  }
432  }
433  }
434  }
435  }
436  }
437  }
438  }
439  }
440  }
441  }
442  }
443  }
444  }
445  }
446  }
447  }
448  }
449  }
450  }
451  }
452  }
453  }
454  }
455  }
456  }
457  }
458  }
459  }
460  }
461  }
462  }
463  }
464  }
465  }
466  }
467  }
468  }
469  }
470  }
471  }
472  }
473  }
474  }
475  }
476  }
477  }
478  }
479  }
480  }
481  }
482  }
483  }
484  }
485  }
486  }
487  }
488  }
489  }
490  }
491  }
492  }
493  }
494  }
495  }
496  }
497  }
498  }
499  }
500  }
501  }
502  }
503  }
504  }
505  }
506  }
507  }
508  }
509  }
510  }
511  }
512  }
513  }
514  }
515  }
516  }
517  }
518  }
519  }
520  }
521  }
522  }
523  }
524  }
525  }
526  }
527  }
528  }
529  }
530  }
531  }
532  }
533  }
534  }
535  }
536  }
537  }
538  }
539  }
540  }
541  }
542  }
543  }
544  }
545  }
546  }
547  }
548  }
549  }
550  }
551  }
552  }
553  }
554  }
555  }
556  }
557  }
558  }
559  }
560  }
561  }
562  }
563  }
564  }
565  }
566  }
567  }
568  }
569  }
570  }
571  }
572  }
573  }
574  }
575  }
576  }
577  }
578  }
579  }
580  }
581  }
582  }
583  }
584  }
585  }
586  }
587  }
588  }
589  }
590  }
591  }
592  }
593  }
594  }
595  }
596  }
597  }
598  }
599  }
600  }
601  }
602  }
603  }
604  }
605  }
606  }
607  }
608  }
609  }
610  }
611  }
612  }
613  }
614  }
615  }
616  }
617  }
618  }
619  }
620  }
621  }
622  }
623  }
624  }
625  }
626  }
627  }
628  }
629  }
630  }
631  }
632  }
633  }
634  }
635  }
636  }
637  }
638  }
639  }
640  }
641  }
642  }
643  }
644  }
645  }
646  }
647  }
648  }
649  }
650  }
651  }
652  }
653  }
654  }
655  }
656  }
657  }
658  }
659  }
660  }
661  }
662  }
663  }
664  }
665  }
666  }
667  }
668  }
669  }
670  }
671  }
672  }
673  }
674  }
675  }
676  }
677  }
678  }
679  }
680  }
681  }
682  }
683  }
684  }
685  }
686  }
687  }
688  }
689  }
690  }
691  }
692  }
693  }
694  }
695  }
696  }
697  }
698  }
699  }
700  }
701  }
702  }
703  }
704  }
705  }
706  }
707  }
708  }
709  }
710  }
711  }
712  }
713  }
714  }
715  }
716  }
717  }
718  }
719  }
720  }
721  }
722  }
723  }
724  }
725  }
726  }
727  }
728  }
729  }
730  }
731  }
732  }
733  }
734  }
735  }
736  }
737  }
738  }
739  }
740  }
741  }
742  }
743  }
744  }
745  }
746  }
747  }
748  }
749  }
750  }
751  }
752  }
753  }
754  }
755  }
756  }
757  }
758  }
759  }
760  }
761  }
762  }
763  }
764  }
765  }
766  }
767  }
768  }
769  }
770  }
771  }
772  }
773  }
774  }
775  }
776  }
777  }
778  }
779  }
780  }
781  }
782  }
783  }
784  }
785  }
786  }
787  }
788  }
789  }
790  }
791  }
792  }
793  }
794  }
795  }
796  }
797  }
798  }
799  }
800  }
801  }
802  }
803  }
804  }
805  }
806  }
807  }
808  }
809  }
810  }
811  }
812  }
813  }
814  }
815  }
816  }
817  }
818  }
819  }
820  }
821  }
822  }
823  }
824  }
825  }
826  }
827  }
828  }
829  }
830  }
831  }
832  }
833  }
834  }
835  }
836  }
837  }
838  }
839  }
840  }
841  }
842  }
843  }
844  }
845  }
846  }
847  }
848  }
849  }
850  }
851  }
852  }
853  }
854  }
855  }
856  }
857  }
858  }
859  }
860  }
861  }
862  }
863  }
864  }
865  }
866  }
867  }
868  }
869  }
870  }
871  }
872  }
873  }
874  }
875  }
876  }
877  }
878  }
879  }
880  }
881  }
882  }
883  }
884  }
885  }
886  }
887  }
888  }
889  }
890  }
891  }
892  }
893  }
894  }
895  }
896  }
897  }
898  }
899  }
900  }
901  }
902  }
903  }
904  }
905  }
906  }
907  }
908  }
909  }
910  }
911  }
912  }
913  }
914  }
915  }
916  }
917  }
918  }
919  }
920  }
921  }
922  }
923  }
924  }
925  }
926  }
927  }
928  }
929  }
930  }
931  }
932  }
933  }
934  }
935  }
936  }
937  }
938  }
939  }
940  }
941  }
942  }
943  }
944  }
945  }
946  }
947  }
948  }
949  }
950  }
951  }
952  }
953  }
954  }
955  }
956  }
957  }
958  }
959  }
960  }
961  }
962  }
963  }
964  }
965  }
966  }
967  }
968  }
969  }
970  }
971  }
972  }
973  }
974  }
975  }
976  }
977  }
978  }
979  }
980  }
981  }
982  }
983  }
984  }
985  }
986  }
987  }
988  }
989  }
990  }
991  }
992  }
993  }
994  }
995  }
996  }
997  }
998  }
999  }
1000  }
    
```

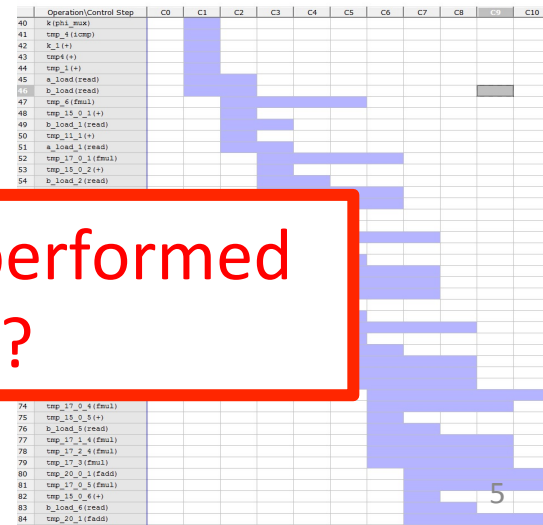
**Performance Estimates**

Timing (ns)

Summary			
Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.41	1.25

Latency (clock cycles)

Summary				
Latency	Interval	T <sub>ave</sub>		
min	max	min	max	T <sub>ave</sub>



Can FPGA design be efficiently performed by software developers?

Instance	0	20	5389	5729
Memory	-	-	-	-
Multiplexer	-	-	-	1269
Register	-	-	2350	-
Total	0	20	7739	7000
Available	280	220	106400	53200
Utilization (%)	0	9	7	13

			Naïve			
M	N	K	Cycle	DSP	FF	LUT
4	4	4	882	5	533	884
4	4	8	1626	5	537	889
4	8	4	1714	5	542	895
4	8	8	3162	5	547	900
8	4	4	1754	5	545	895
8	4	8	3234	5	550	900
8	8	4	3418	5	550	906
8	8	8	6306	5	554	911

```

for (int i = 0; i != m; ++i)
  for (int j = 0; j != n; ++j)
    for (int p = 0; p != k; ++p)
      c[i][j] += a[i][p]*b[p][j]

```

M	N	K	Naïve			
			Cycle	DSP	FF	LUT
4	4	4	882	5	533	884
4	4	8	1626	5	537	889
4	8	4	1714	5	542	895
4	8	8	3162	5	547	900
8	4	4	1754	5	545	895
8	4	8	3234	5	550	900
8	8	4	3418	5	550	906
8	8	8	6306	5	554	911

```

for (int i = 0; i != m; ++i)
  for (int j = 0; j != n; ++j)
    for (int p = 0; p != k; ++p)
      c[i][j] += a[i][p]*b[p][j]

```

**0.162 FLOPS / cycle**

M	N	K	Naïve			
			Cycle	DSP	FF	LUT
4	4	4	882	5	533	884
4	4	8	1626	5	537	889
4	8	4	1714	5	542	895
4	8	8	3162	5	547	900
8	4	4	1754	5	545	895
8	4	8	3234	5	550	900
8	8	4	3418	5	550	906
8	8	8	6306	5	554	911

```

for (int i = 0; i != m; ++i)
  for (int j = 0; j != n; ++j)
    for (int p = 0; p != k; ++p)
      c[i][j] += a[i][p]*b[p][j]

```

**2% of available resources**



M	N	K	Naïve				HPC			
			Cycle	DSP	FF	LUT	Cycle	DSP	FF	LUT
4	4	4	882	5	533	884	33	44	5407	8964
4	4	8	1626	5	537	889	53	44	5411	8970
4	8	4	1714	5	542	895	34	85	10908	17578
4	8	8	3162	5	547	900	54	85	10912	17585
8	4	4	1754	5	545	895	34	85	10748	17581
8	4	8	3234	5	550	900	54	85	10752	17589
8	8	4	3418	5	550	906	34	167	21142	34547
8	8	8	6306	5	554	911	54	167	21146	34555

**18.96 FLOPS / cycle**

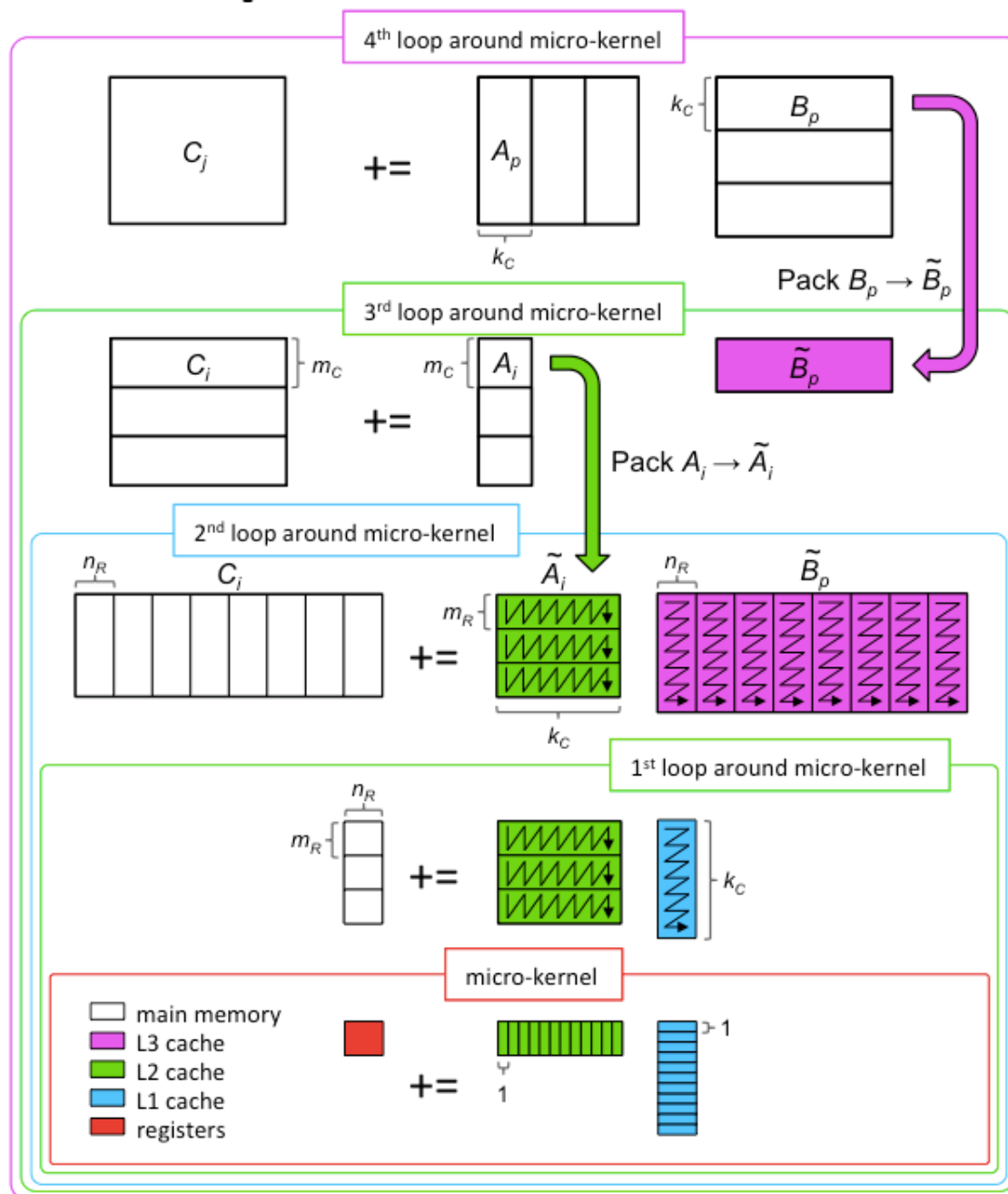
```
#pragma HLS ARRAY_PARTITION
      variable=C block factor=4 dim=1
```

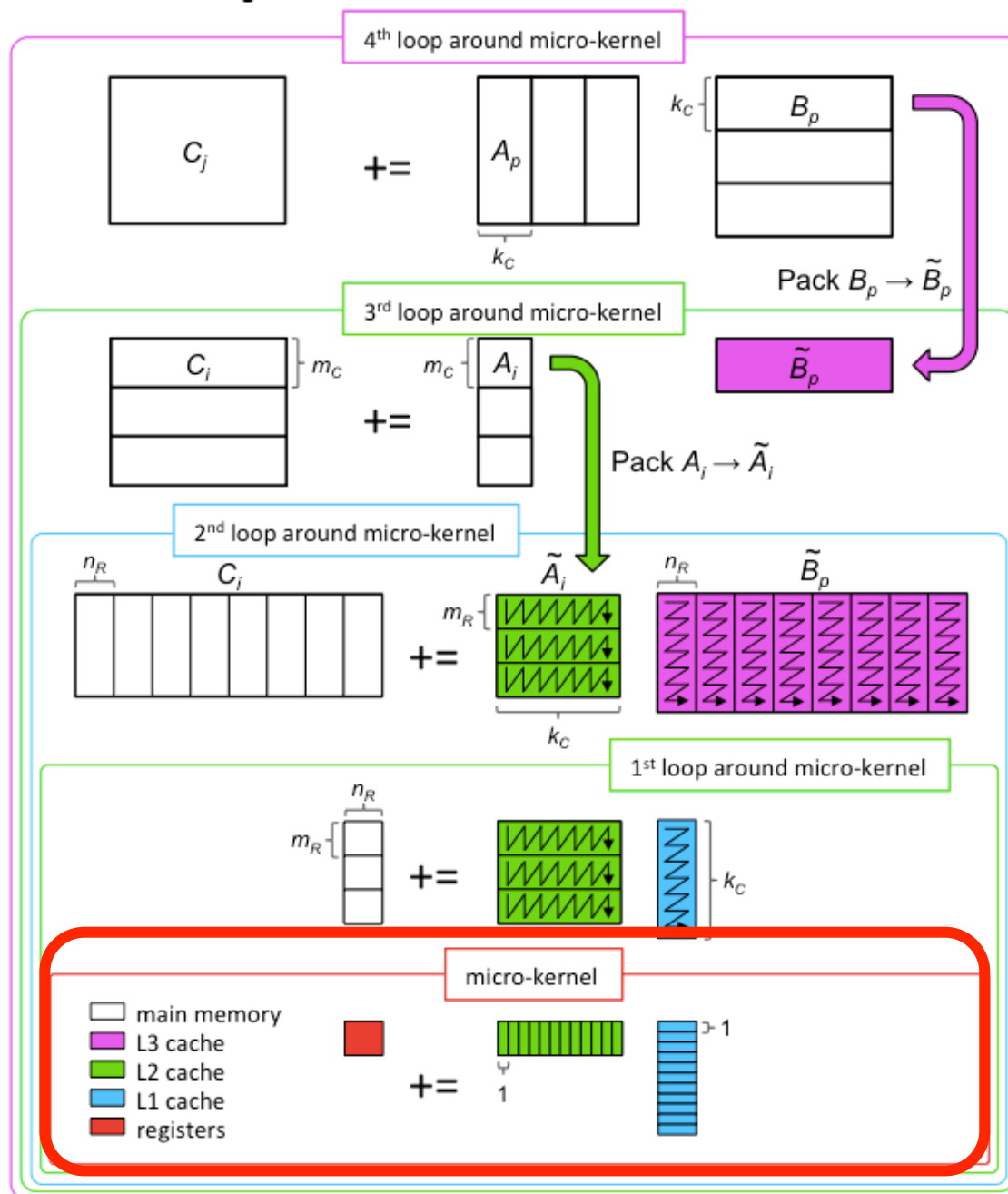
M	N	K	Naïve				HPC				HLS			
			Cycle	DSP	FF	LUT	Cycle	DSP	FF	LUT	Cycle	DSP	FF	LUT
4	4	4	882	5	533	884	33	44	5407	8964	33	44	5407	8964
4	4	8	1626	5	537	889	53	44	5411	8970	53	44	5411	8970
4	8	4	1714	5	542	895	34	85	10908	17578	34	85	10908	17578
4	8	8	3162	5	547	900	54	85	10912	17585	54	85	10912	17585
8	4	4	1754	5	545	895	34	85	10748	17581	34	85	10748	17581
8	4	8	3234	5	550	900	54	85	10752	17589	54	85	10752	17589
8	8	4	3418	5	550	906	34	167	21142	34547	34	167	21142	34547
8	8	8	6306	5	554	911	54	167	21146	34555	54	167	21146	34555

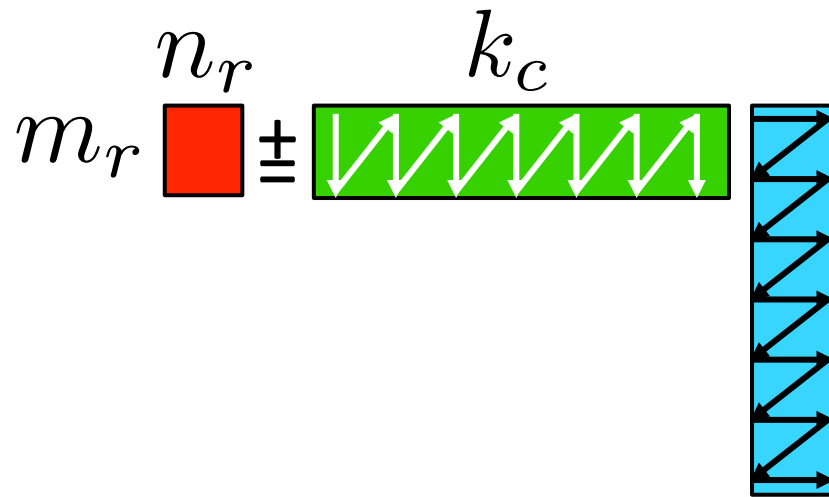
```

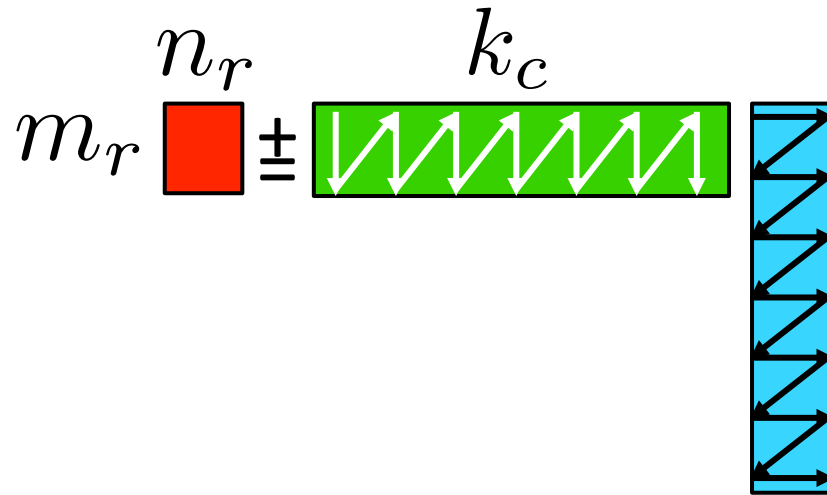
#pragma HLS ARRAY_PARTITION
        variable=C block factor=4 dim=1
#pragma HLS PIPELINE II=5
#pragma HLS UNROLL

```

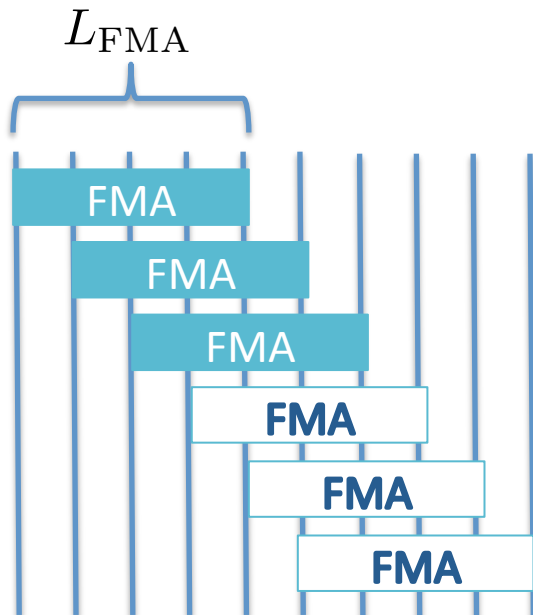


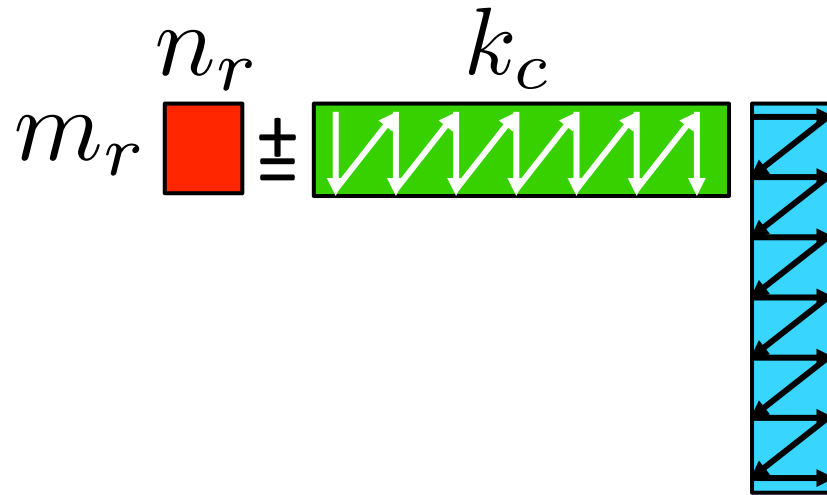




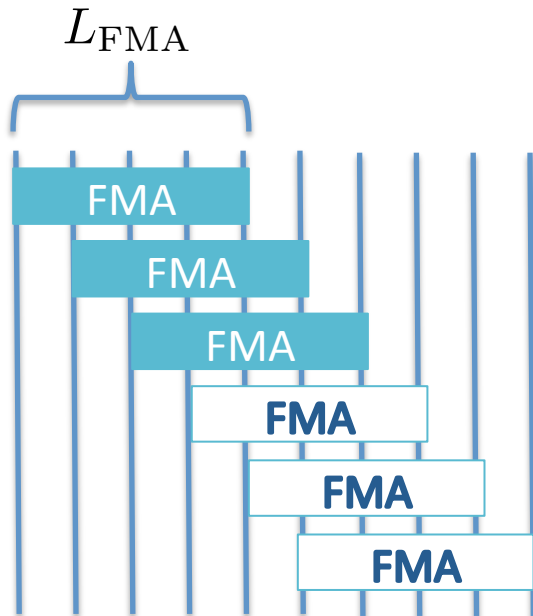


$$n_r n_r \geq N_{\text{FMA}} L_{\text{FMA}} N_{\text{vec}}$$



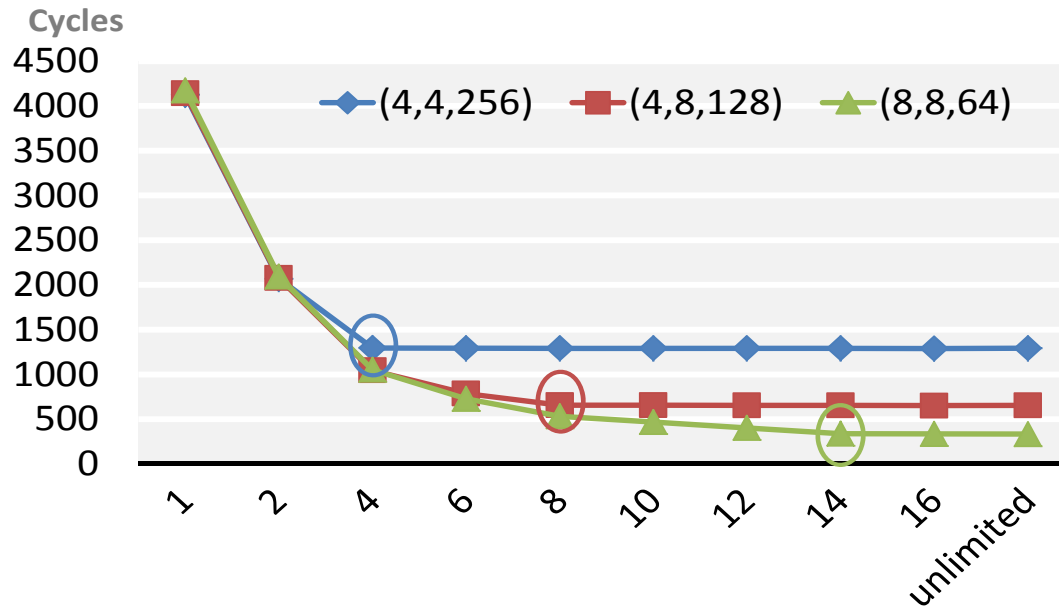


$$n_r n_r \geq N_{\text{FMA}} L_{\text{FMA}} N_{\text{vec}}$$

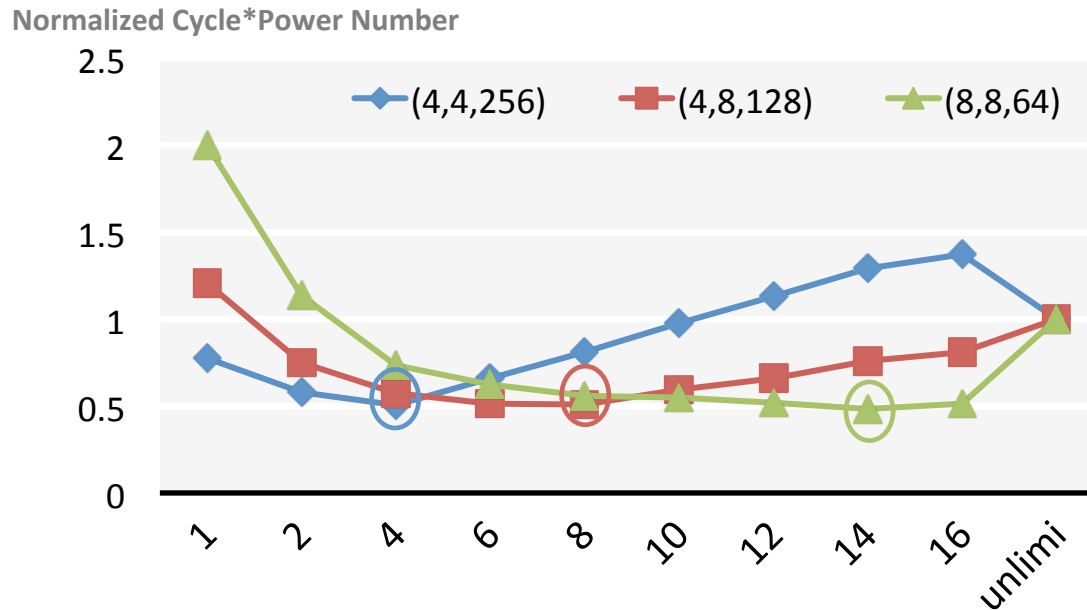


- Key Differences
  - Variable architecture
  - Fixed problem size  
 $n_r \quad n_r$
  - Dependent on HLS implementation for  $L_{\text{FMA}}$

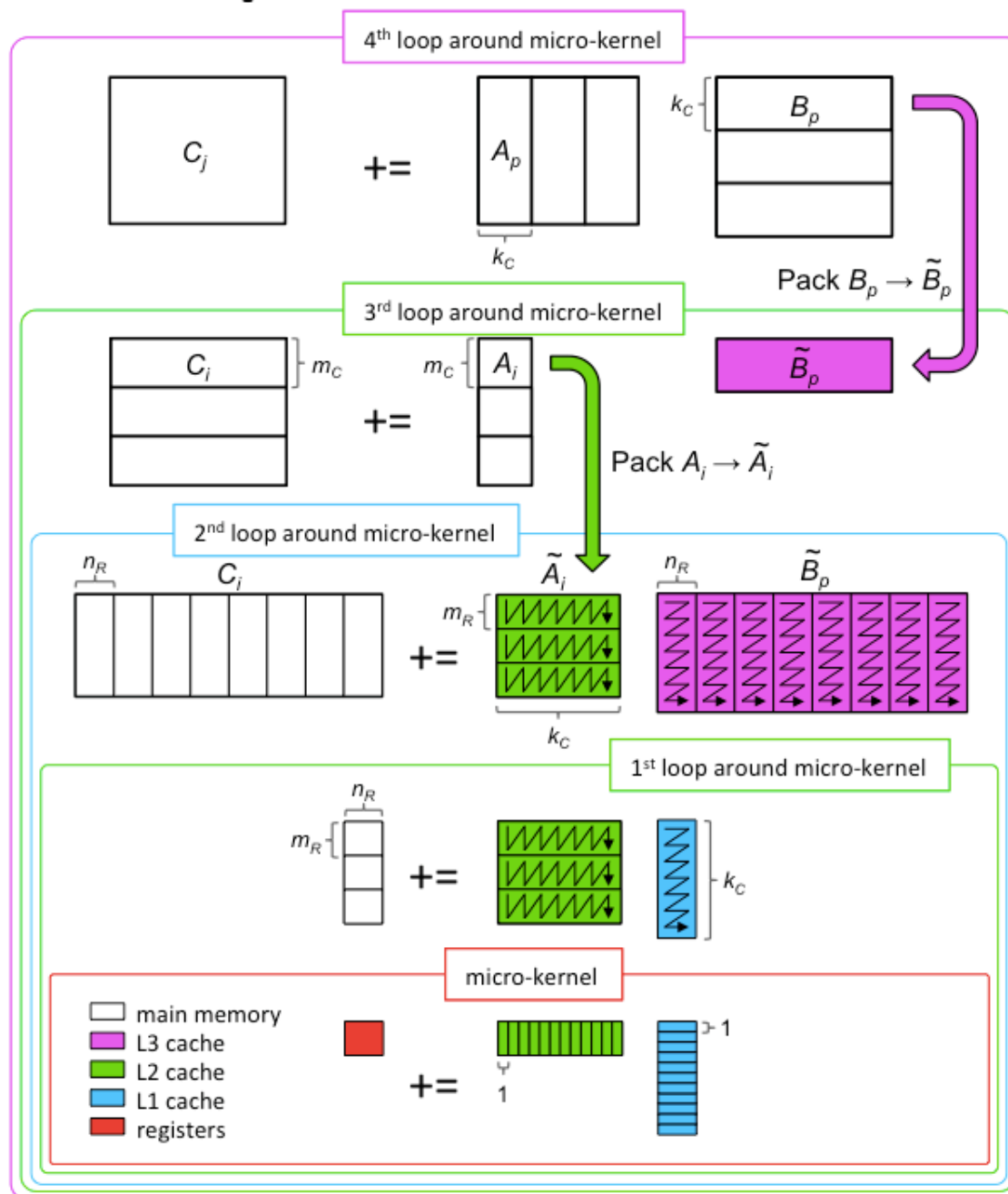
### Execution Cycles given Different Number of PEs



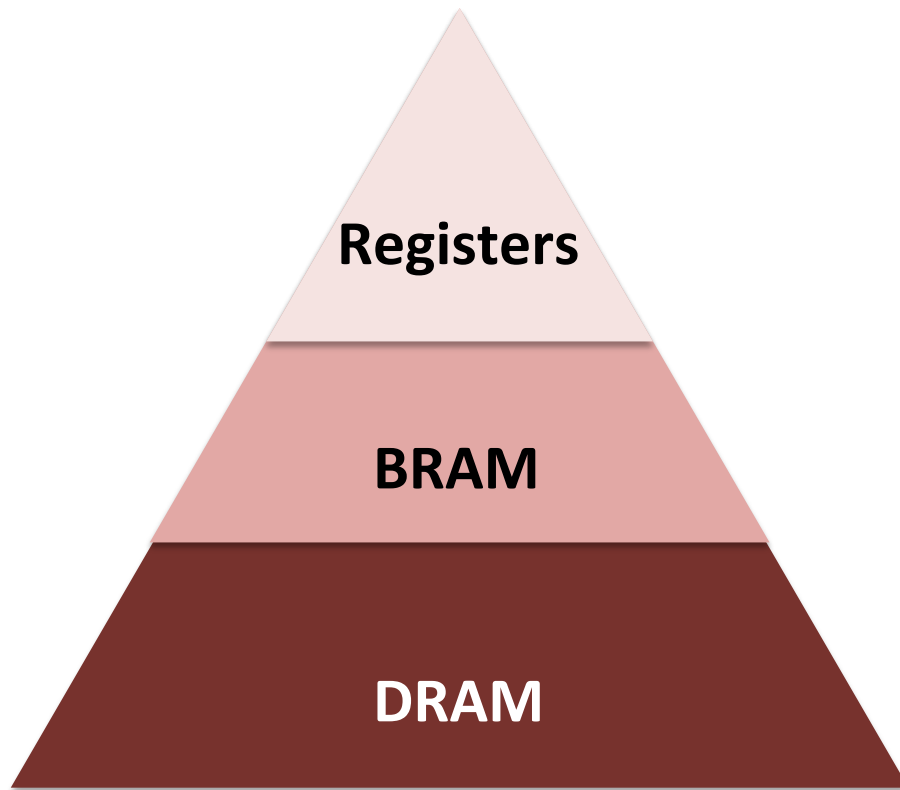
### Power Efficiency given Different Number of PEs



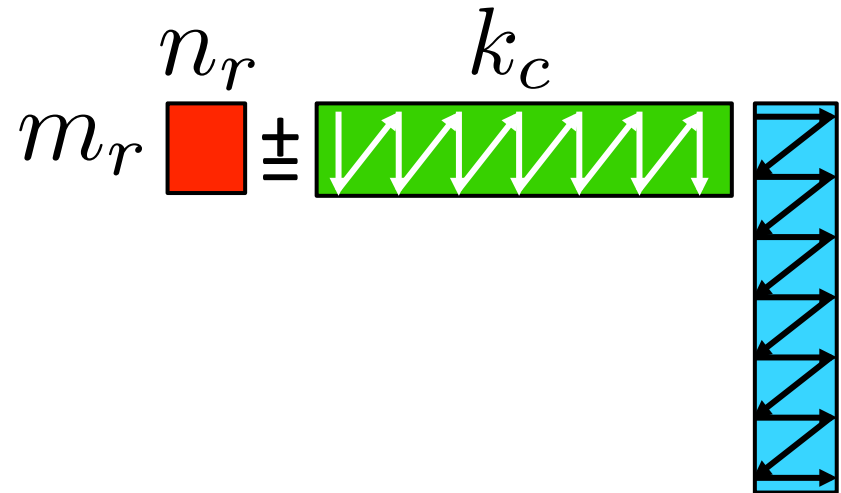
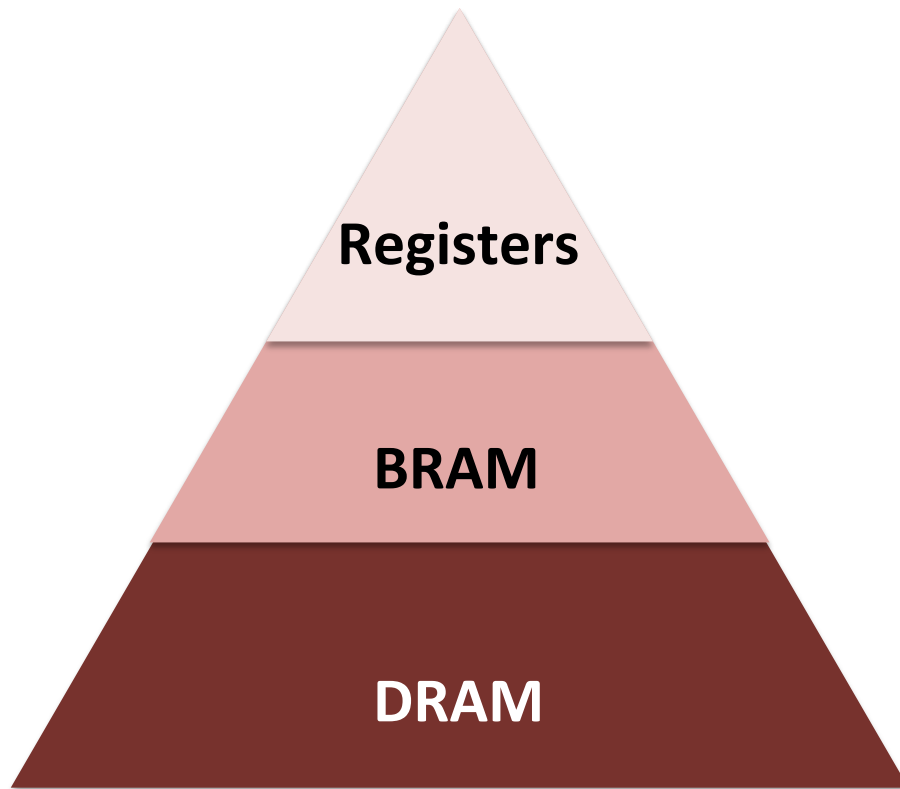




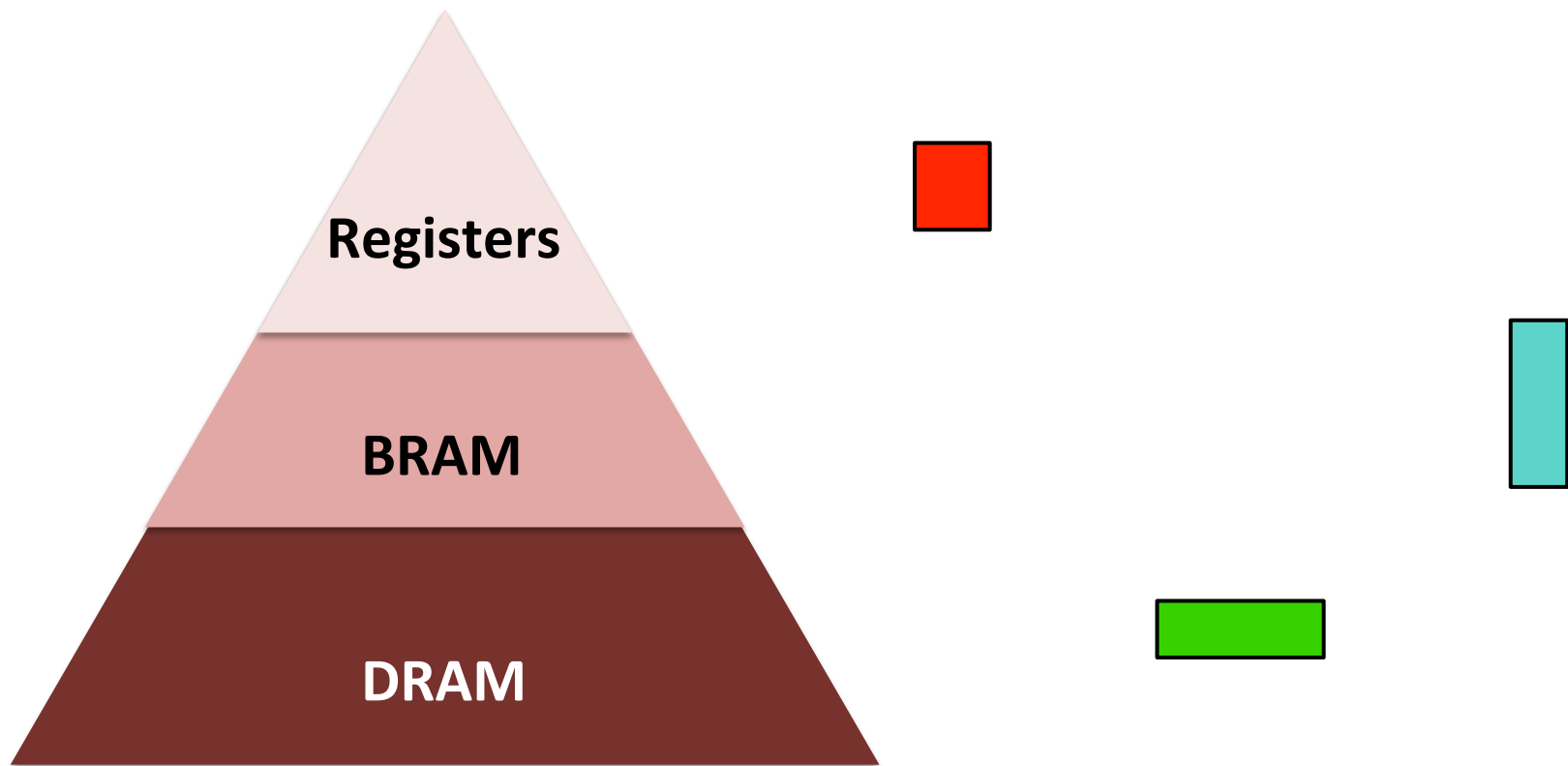
# Data Movement



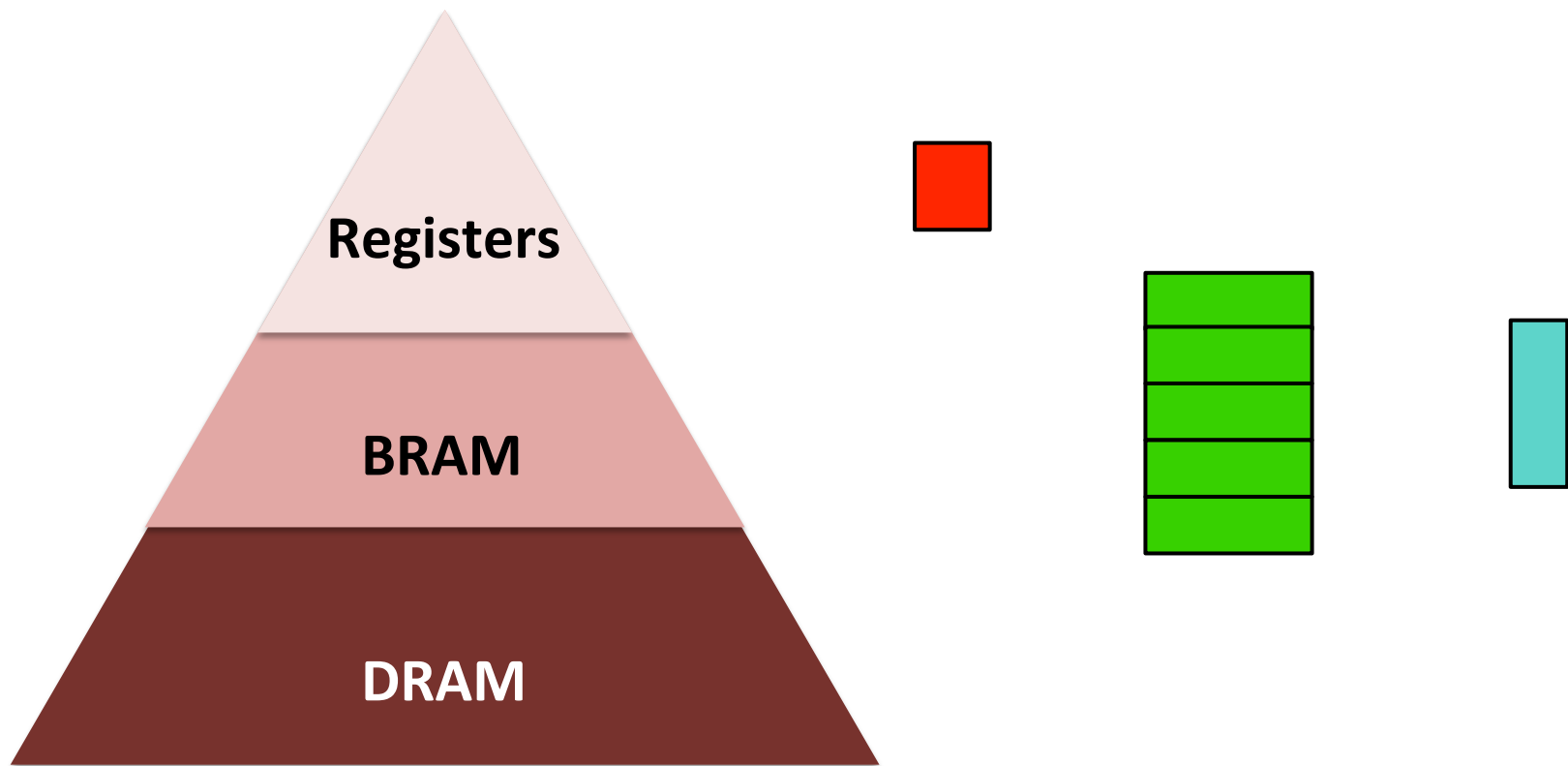
# Data Movement

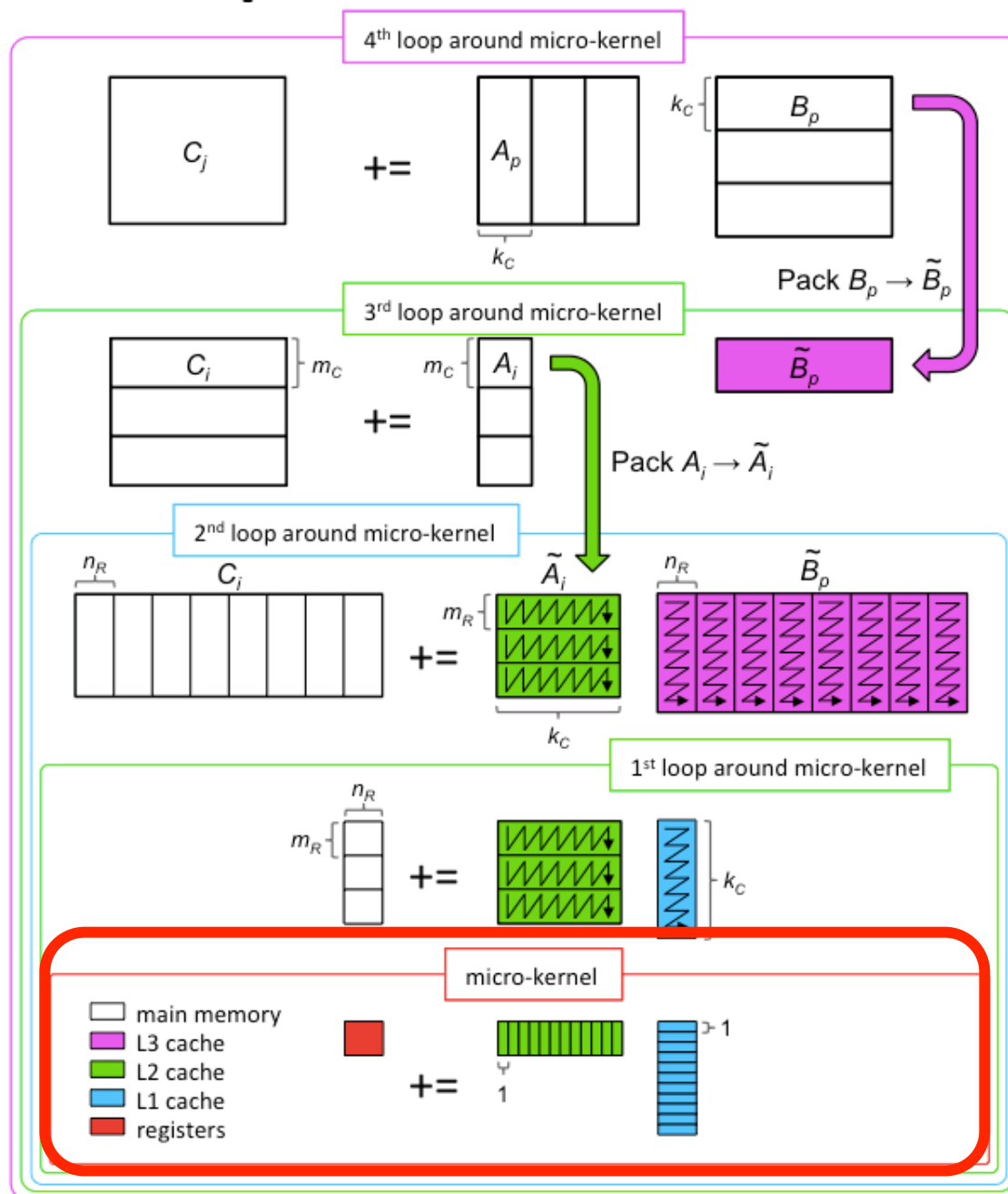


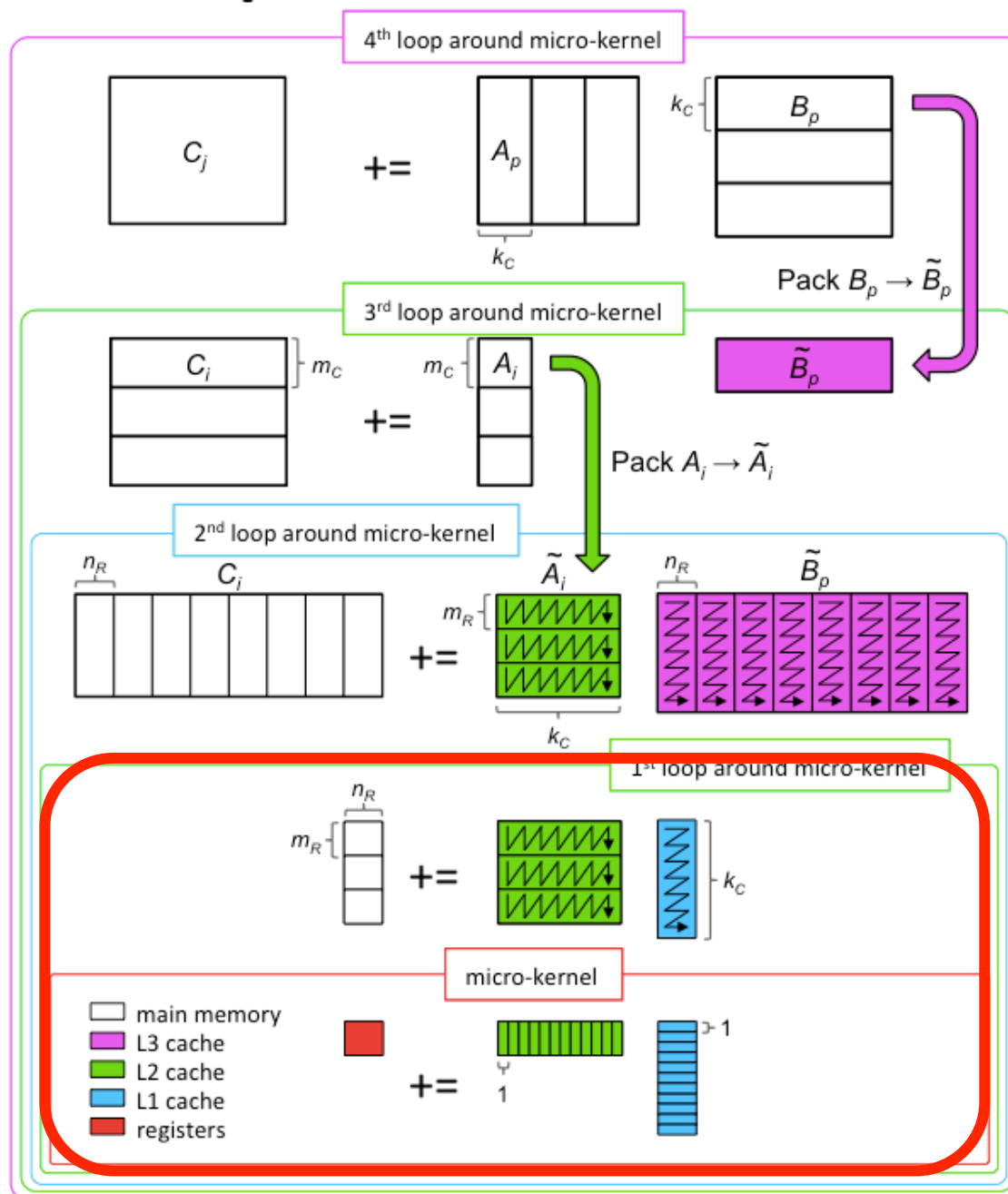
# Data Movement



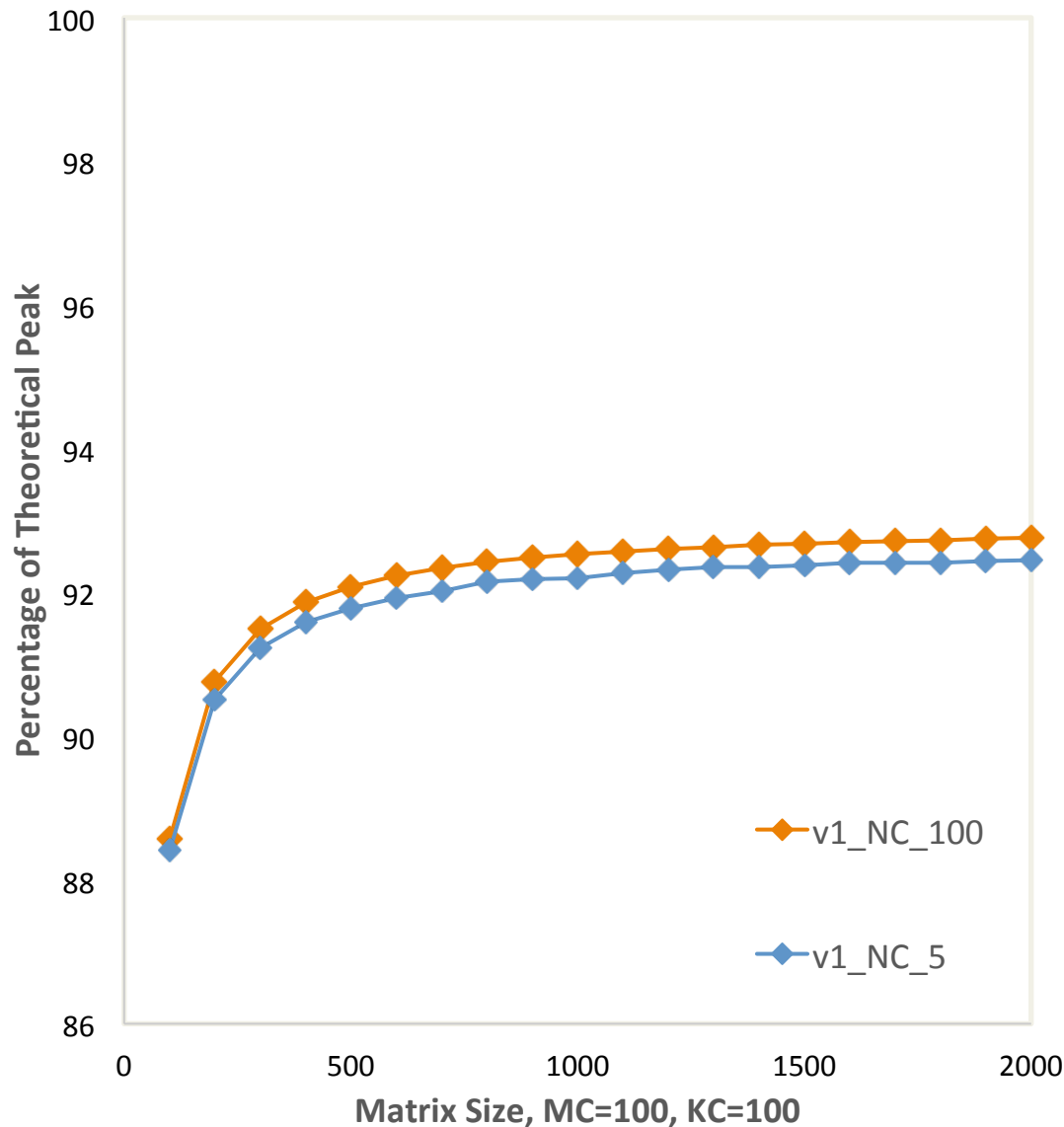
# Data Movement







## Percentage of peak as matrix size increases



Based on 4 FMA units

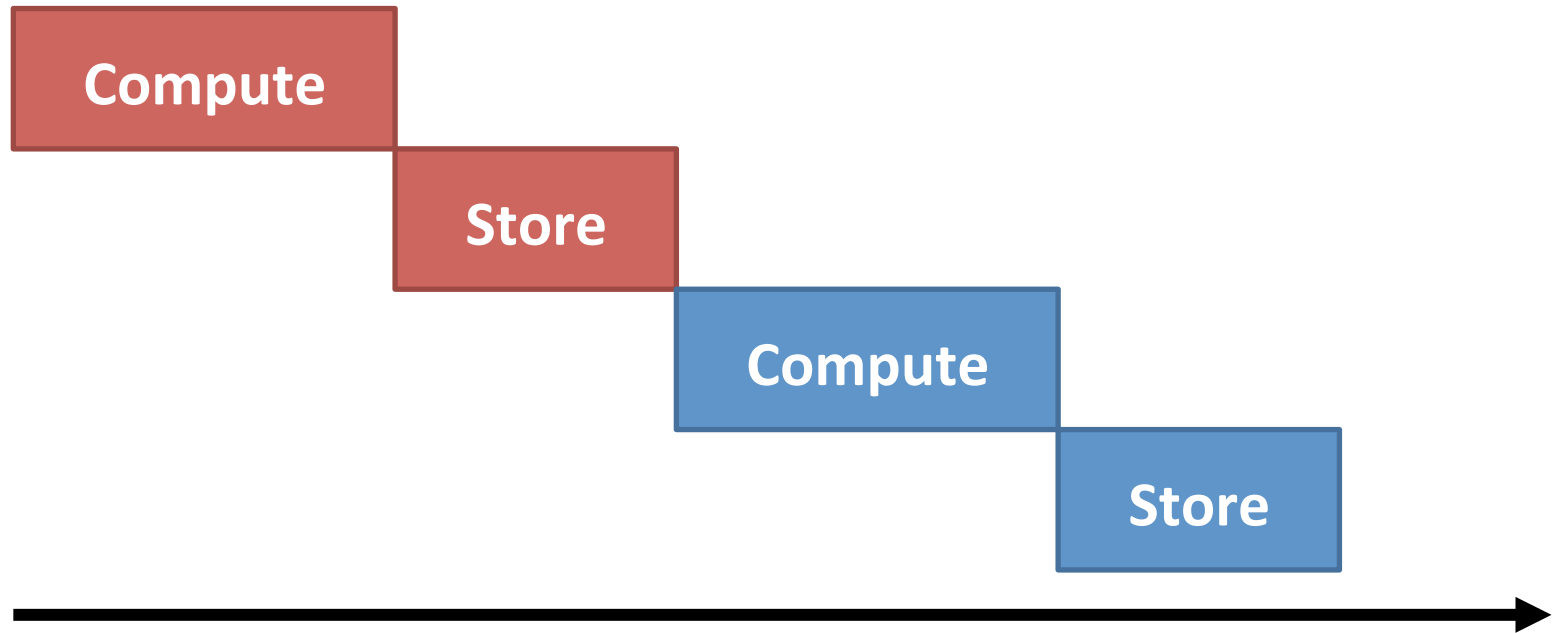
$$m_r = 4$$

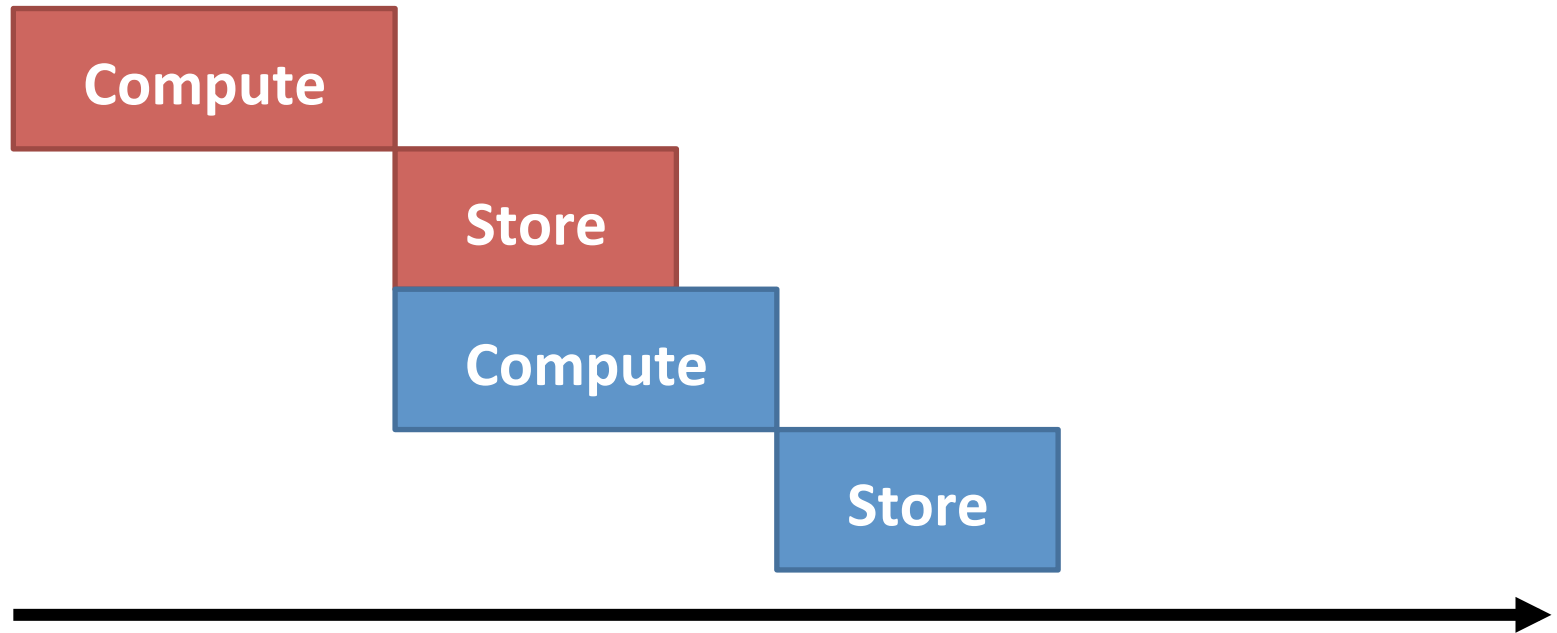
$$n_r = 5$$

$$k_c = 100$$

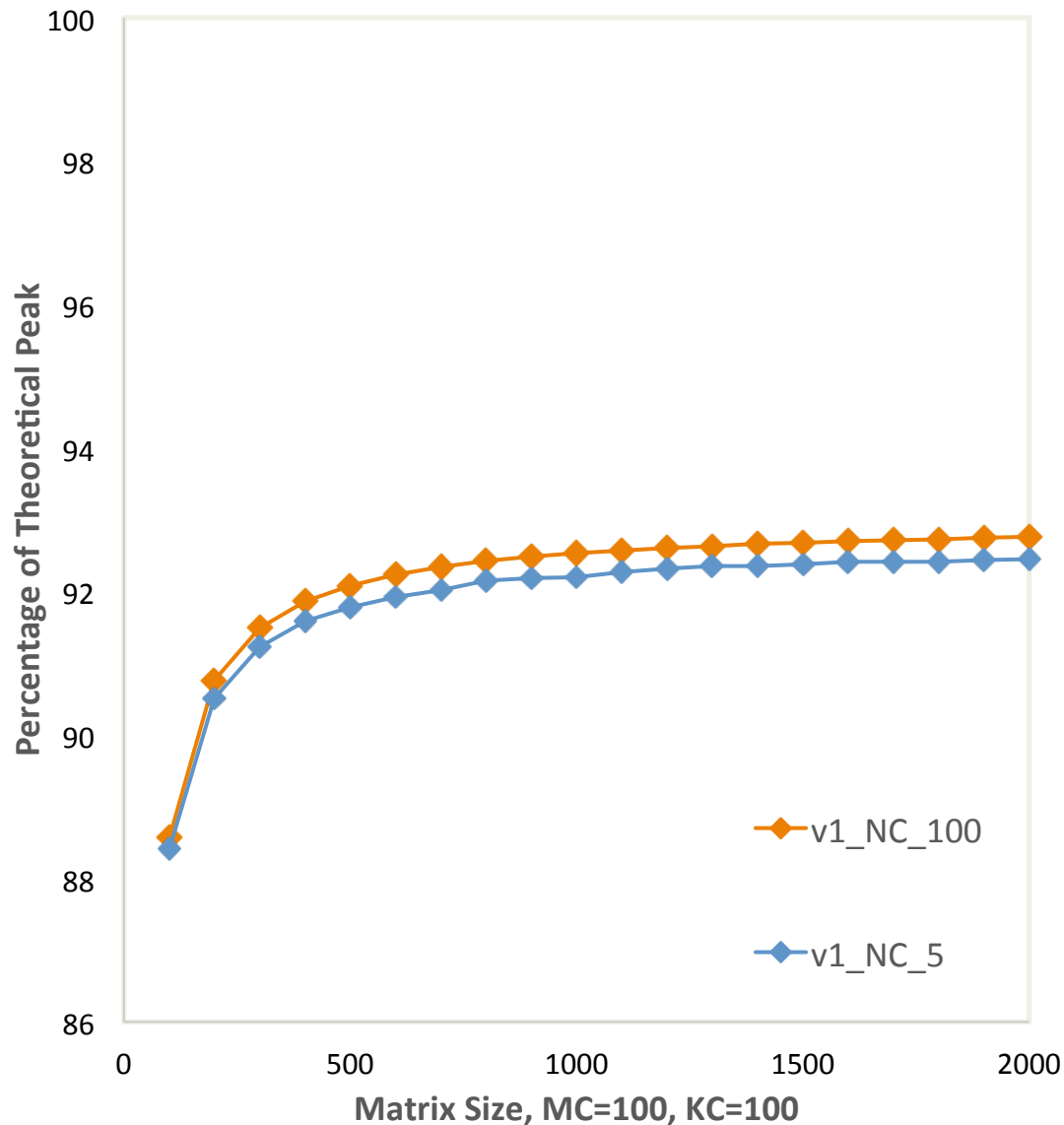
$$m_c = 20$$







## Percentage of peak as matrix size increases



Based on 4 FMA units

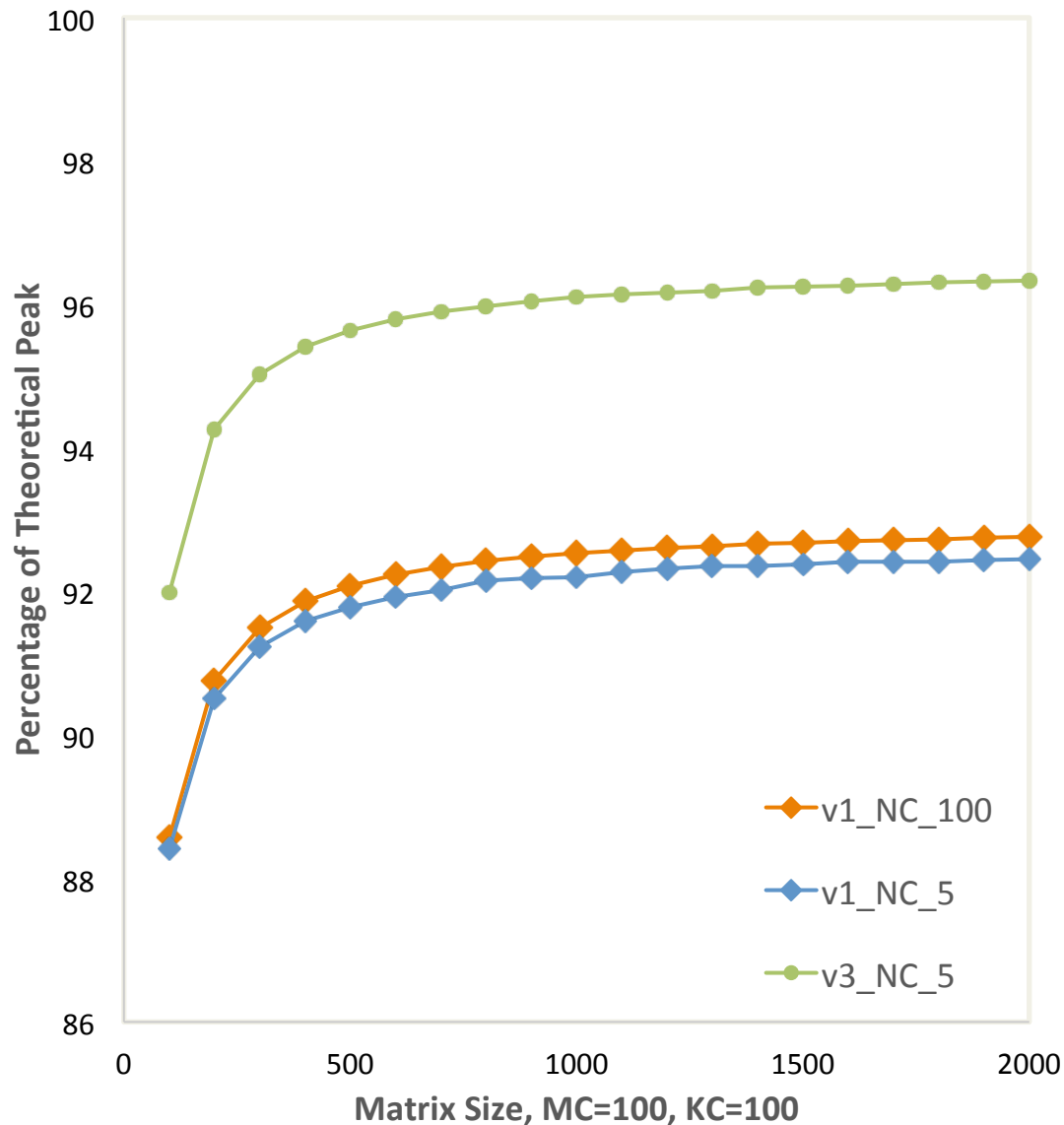
$$m_r = 4$$

$$n_r = 5$$

$$k_c = 100$$

$$m_c = 20$$

## Percentage of peak as matrix size increases



Based on 4 FMA units

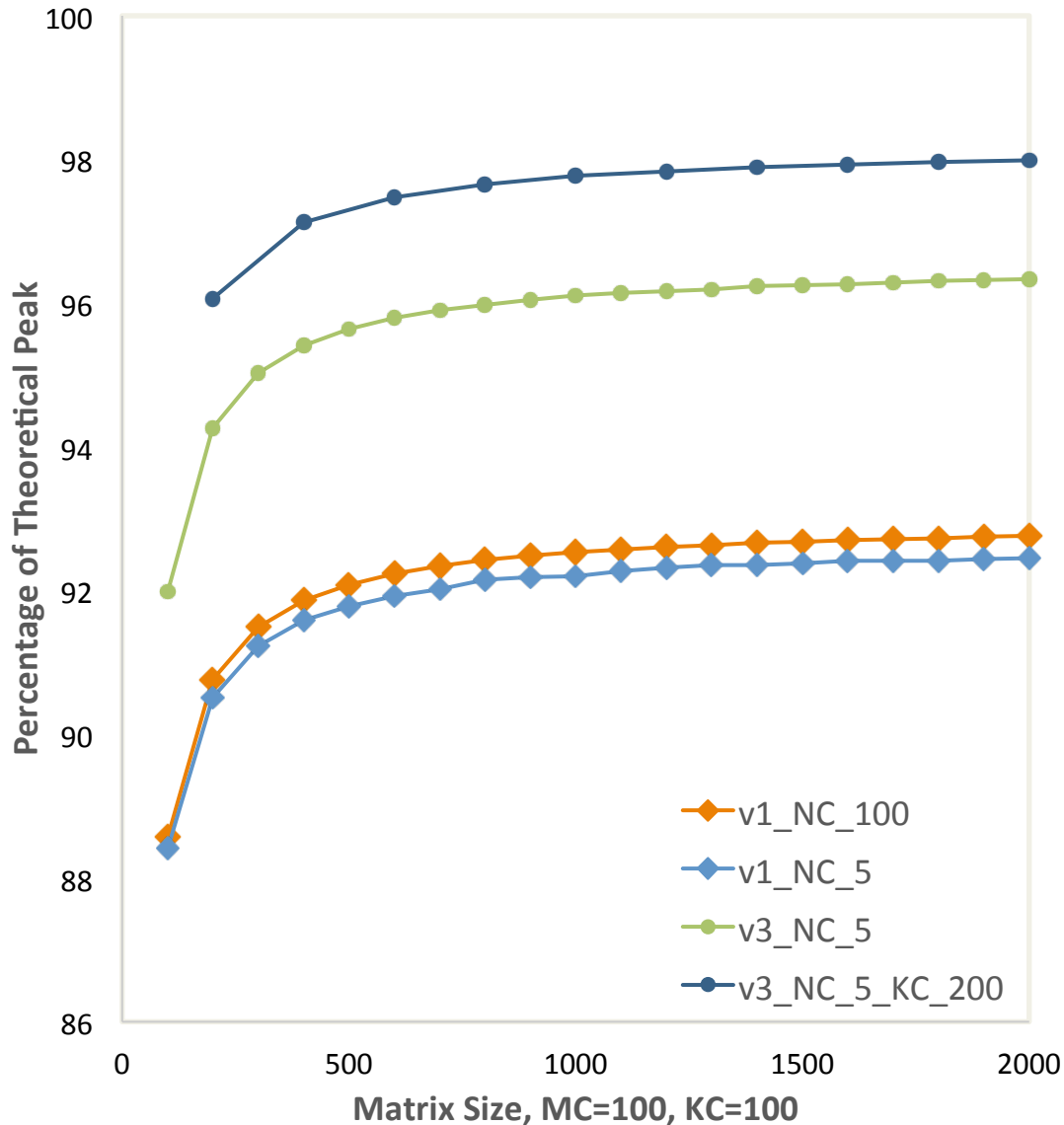
$$m_r = 4$$

$$n_r = 5$$

$$k_c = 100$$

$$m_c = 20$$

Percentage of peak as matrix size increases



Based on 4 FMA units

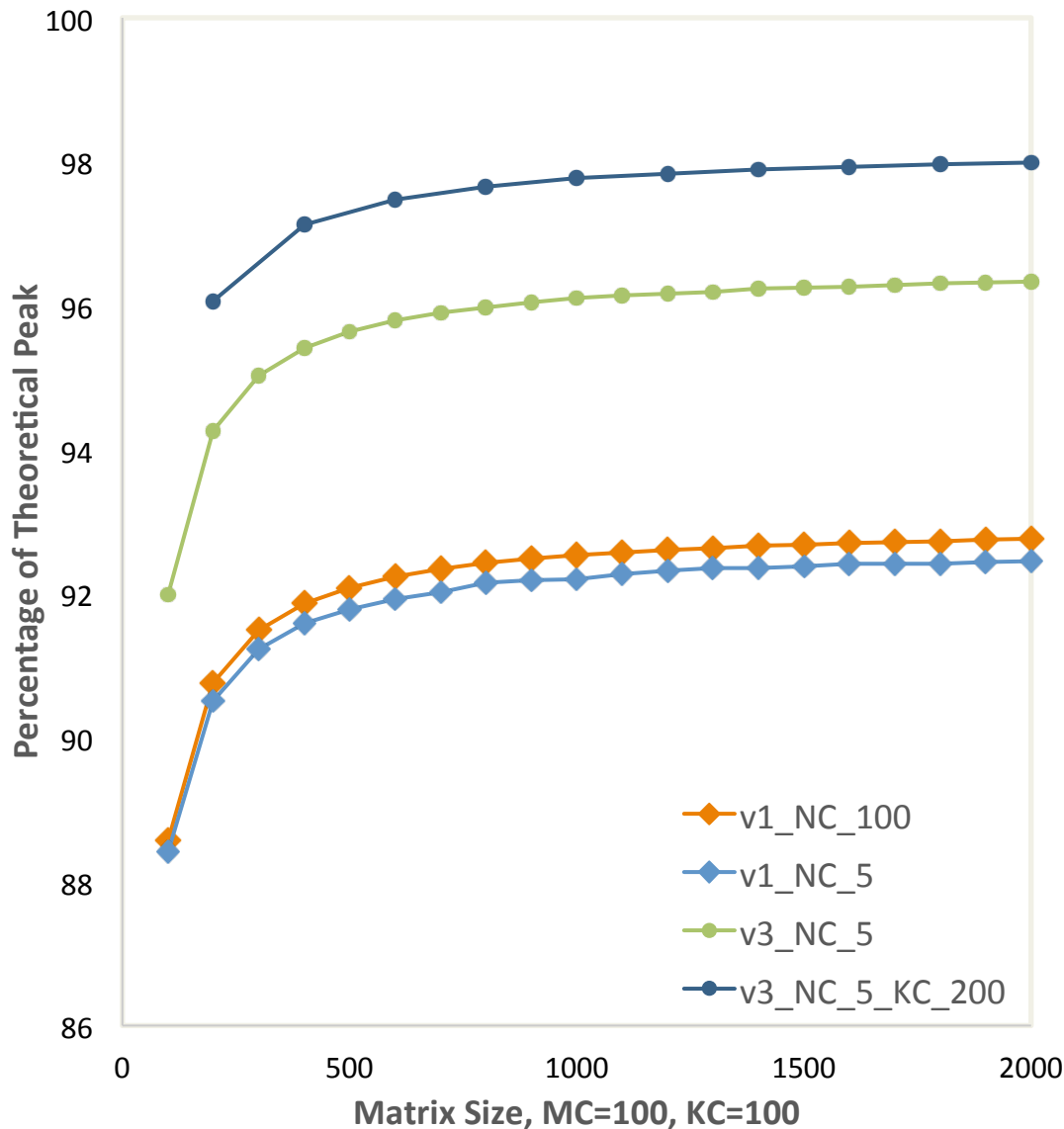
$$m_r = 4$$

$$n_r = 5$$

$$k_c = \cancel{100} 200$$

$$m_c = 20$$

## Percentage of peak as matrix size increases



Based on 4 FMA units

$$m_r = 4$$

$$n_r = 5$$

$$k_c = \cancel{100} 200$$

$$m_c = 20$$

Double buffer the movement of A

# Summary

- Analytical models for BLIS are good starting points for FPGAs
- Data movement requirements change how kernels are written
- Next, parallel BLIS implementations

# Questions?