

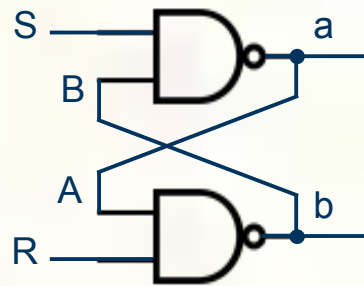


# Storage Elements and Memory





# R-S Latch

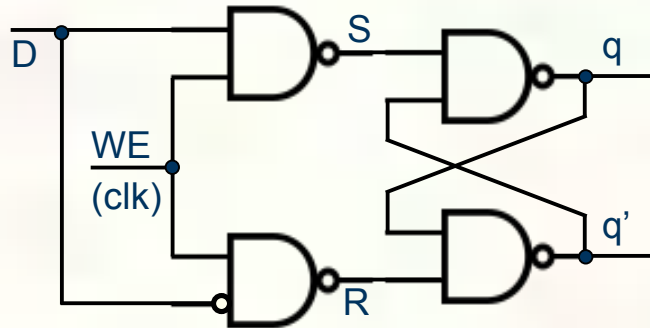


R	S	a	b
0	0	1	1
0	1	0	1
1	0	1	0
1	1	?	?

A	R	S	a	b	A	R	S	a	b
0	0	0	1	1	x	0	0	1	1
0	0	1	0	1	x	0	1	0	1
0	1	0	1	0	x	1	0	1	0
0	1	1	0	1	0	1	1	0	1
1	0	0	1	1	1	1	1	1	0
1	0	1	0	1					
1	1	0	1	0					
1	1	1	1	0					



# D Latch

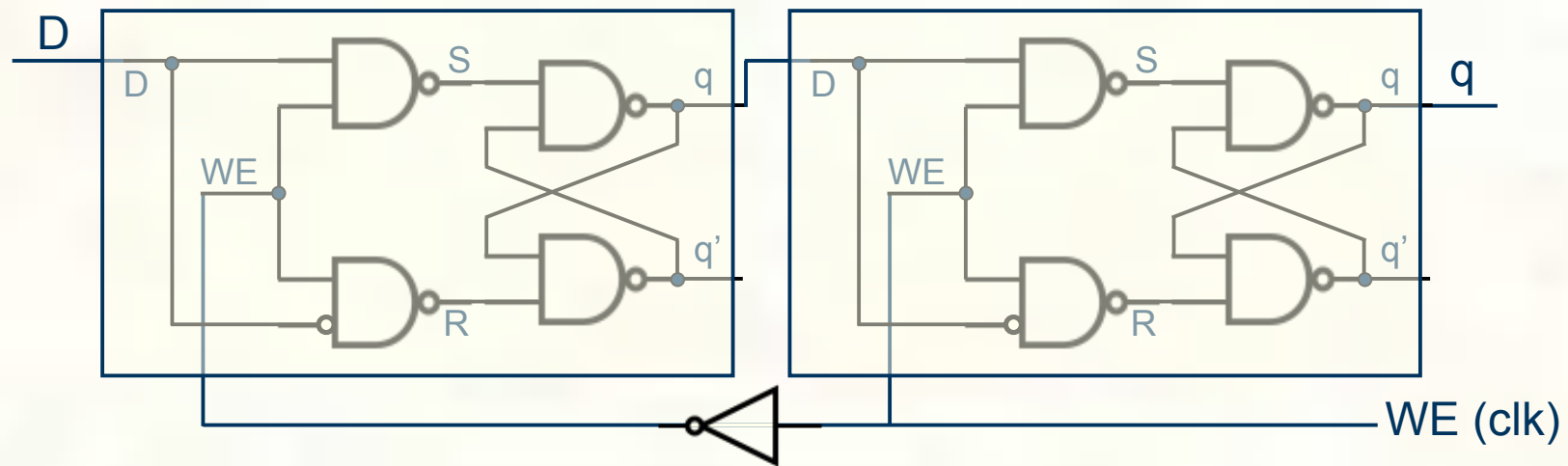


WE	q	D	q	q'
0	0	x	0	1
0	1	x	1	0
1	x	0	0	1
1	x	1	1	0

Note: a **latch** is a **level-triggered** storage element. Level-triggered means the stored data can be changed when the clock is at a specified voltage.



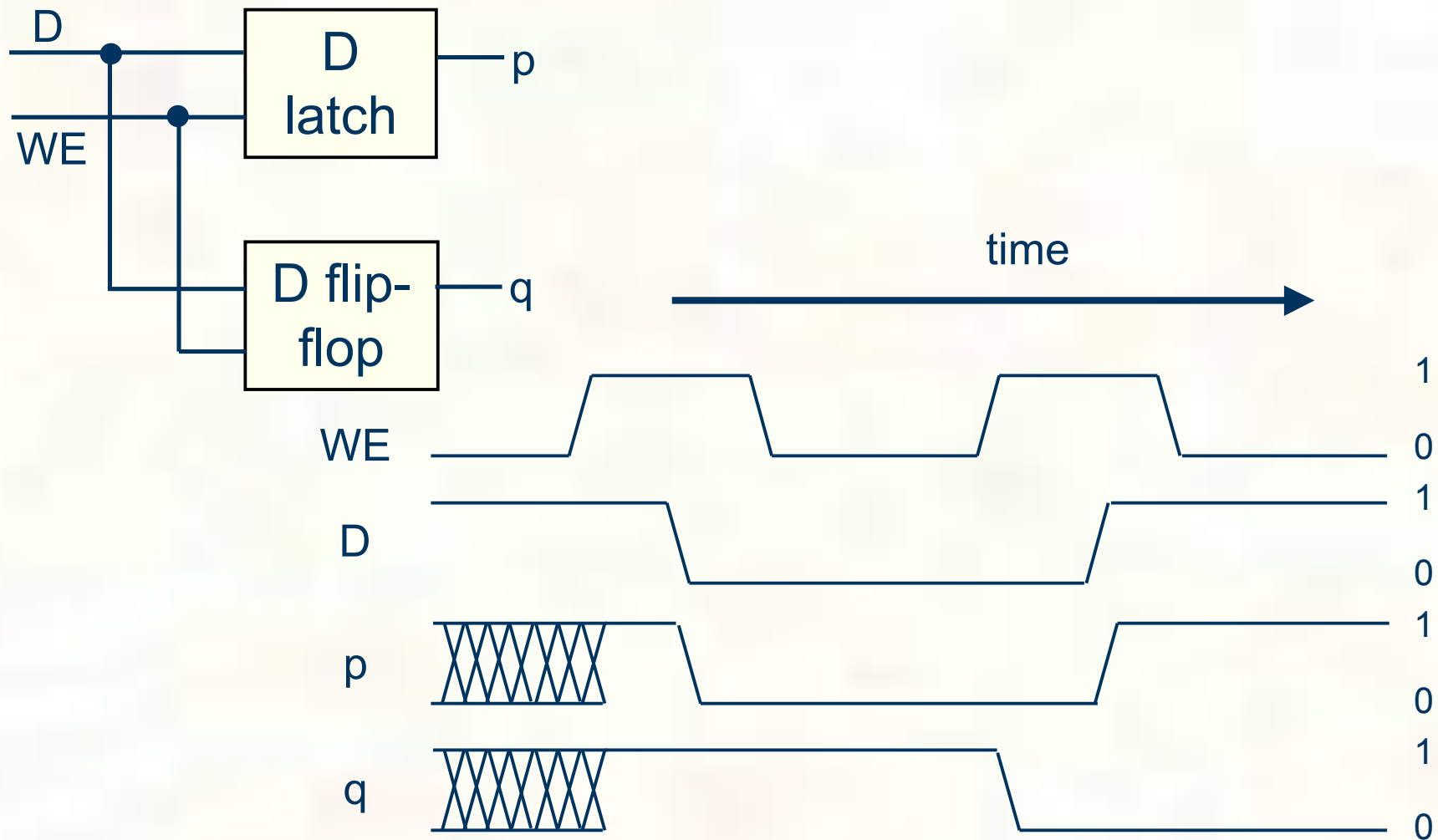
# D Flip-flop



Note: a **flip-flop** is an **edge-triggered** storage element. Edge-triggered means the stored data can be changed when the clock changes voltage, either from low to high (as here) or high to low.



# Edge vs. level triggering

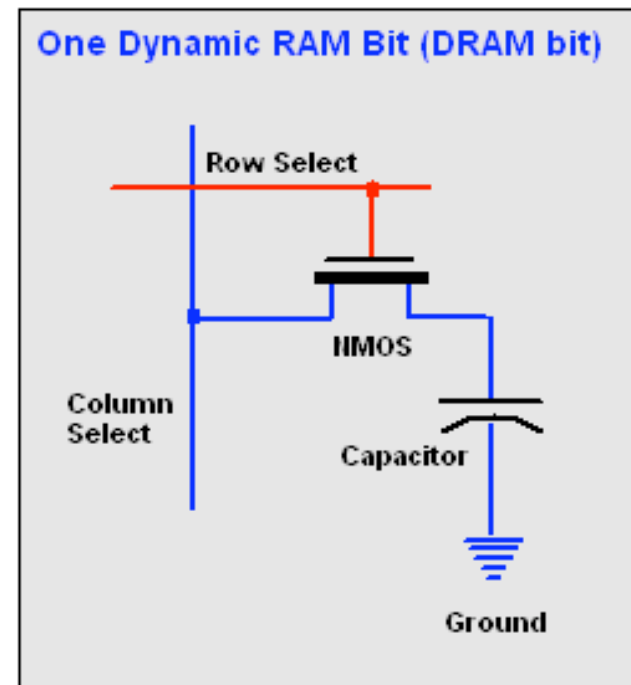




# Cheaper Memory

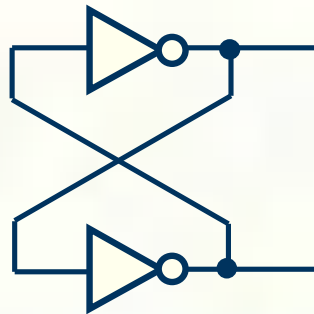
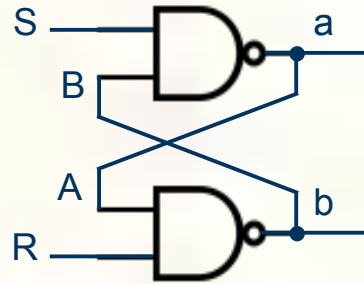
- 8+ CMOS transistors per bit is too much for large scale memory (okay for registers, although we can trim the transistor count just a bit)
- 1 transistor per bit DRAM uses a single transistor to trap charge on a capacitor (“dangling wire”), and then read out whether or not there’s charge there. The charge leaks out after a while, so it needs to be refreshed, and it’s pretty slow since it needs lots of amplification.
- Called dynamic memory since it needs to be refreshed (as opposed to self-amplifying, static memory).

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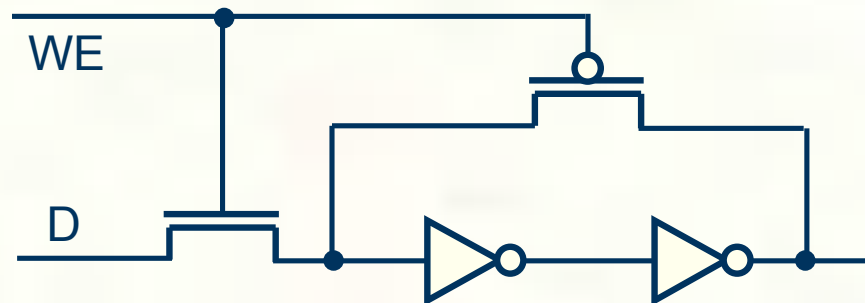




# Static bit in CMOS

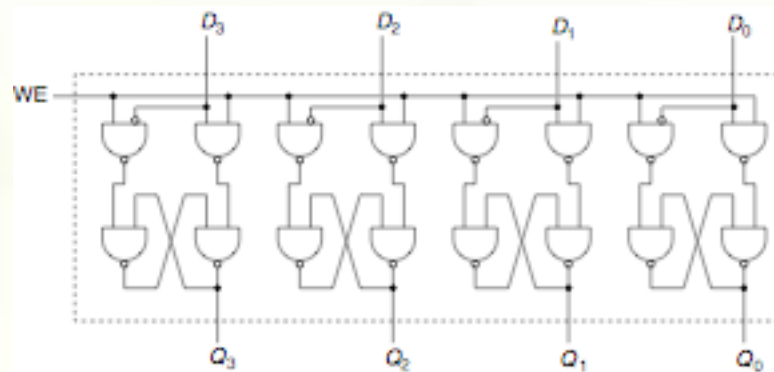


- This is 8 transistors (verify). Can we do better?
- Let's "cheat" and do our designs with transistors as well as Boolean logic
- Now we only need 6 transistors, and it gives us a D latch (which took 16 or 18 the Boolean way)
  - Actually, the 6 transistor design you'll see in normal use doesn't quite work like this, but it's close.





# Memory from bits

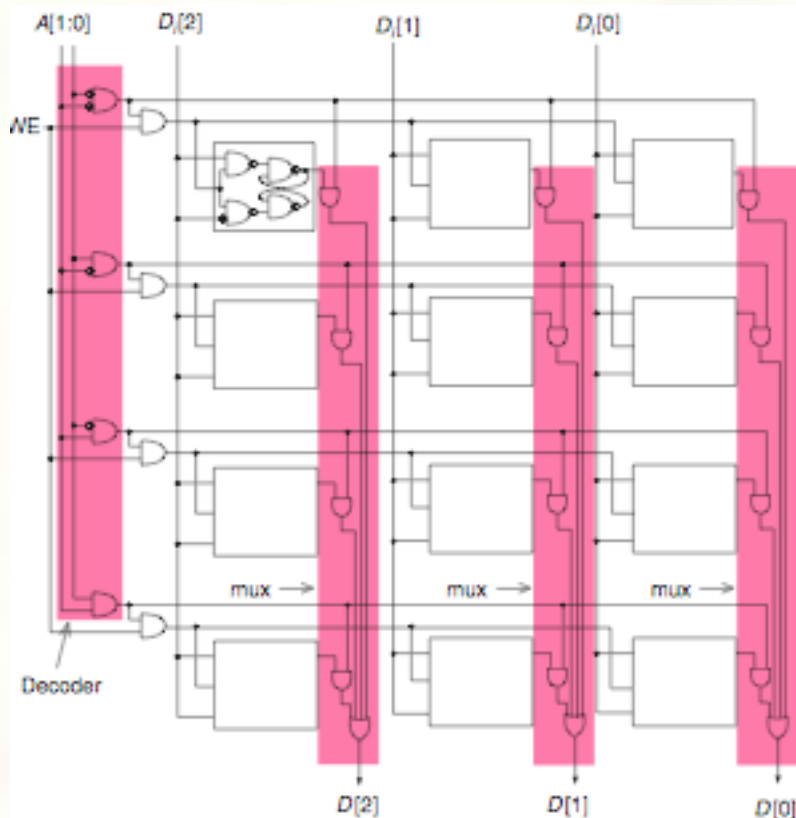


- A 4-bit register using D latches





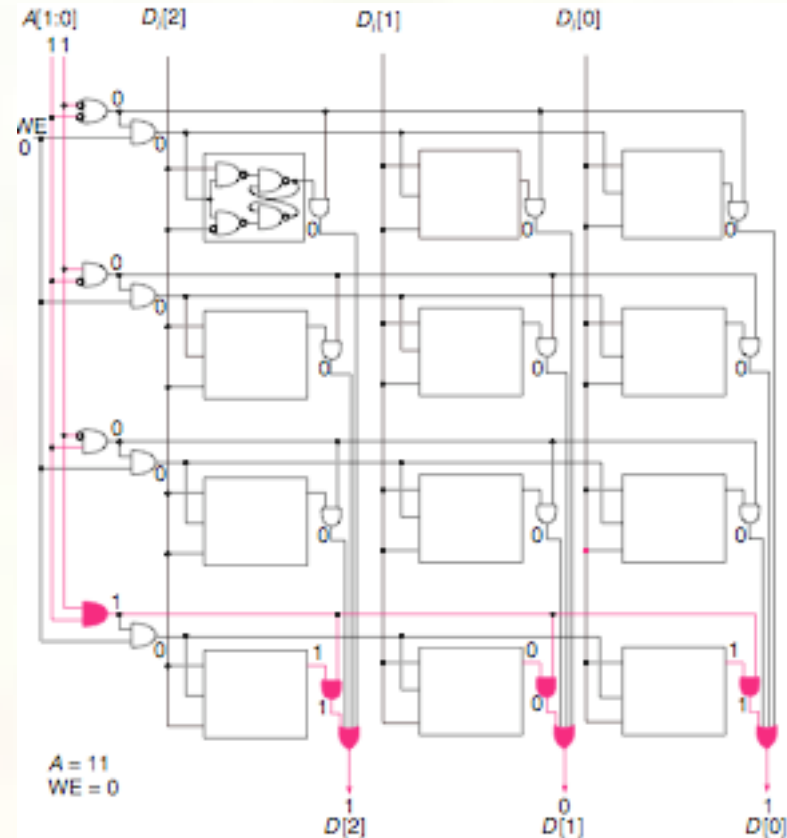
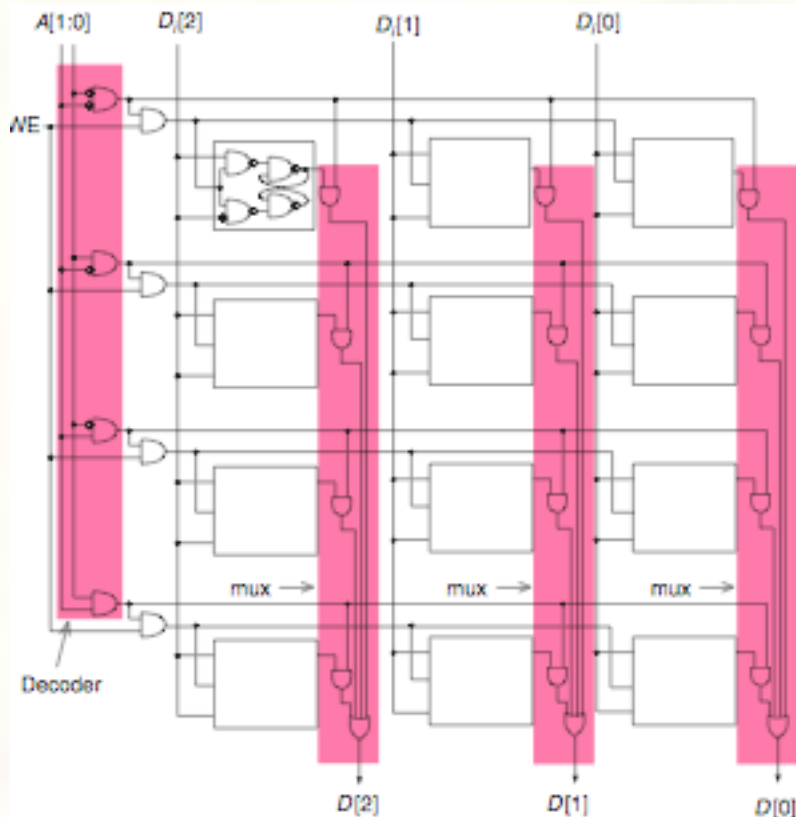
# Memory organization



- Address space = 4
- Addressability = 3 bits
- The leftmost pink box is a decoder
- What are the other 3 pink boxes?



# Memory organization



- Address space = 4
- Addressability = 3 bits
- The leftmost pink box is a decoder
- What are the other 3 pink boxes?

- Reading word 3