

Systems I

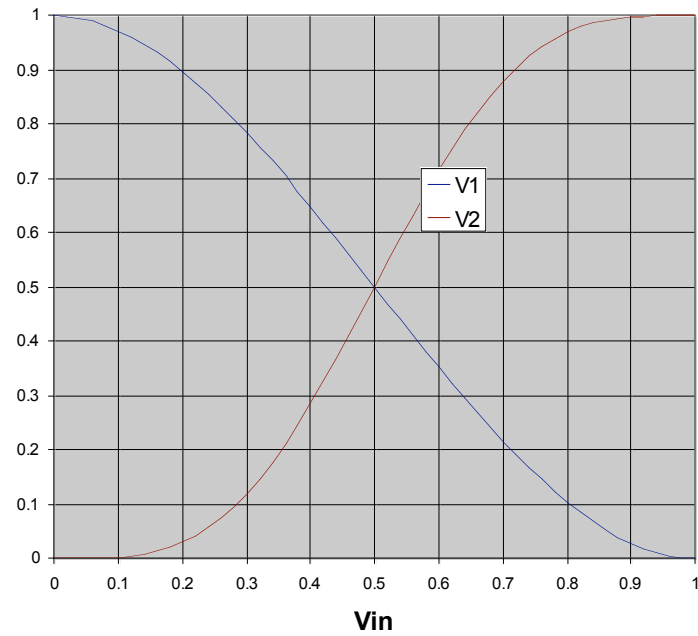
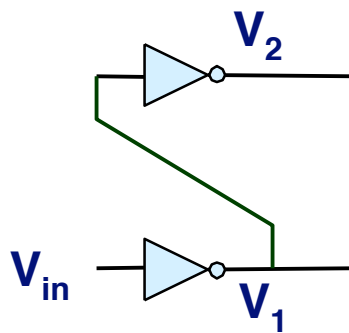
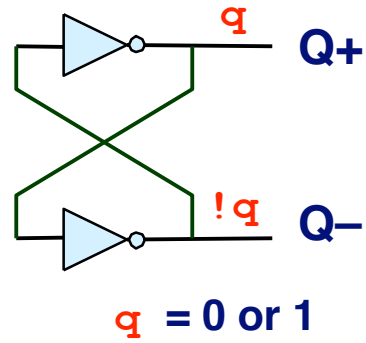
Logic Design II

Topics

- Storage technologies
- Capacity and latency trends
- The hierarchy

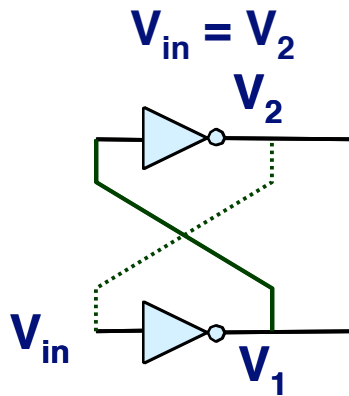
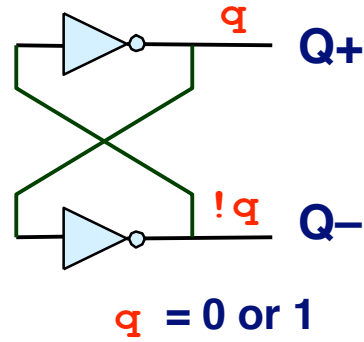
Storing 1 Bit

Bistable Element

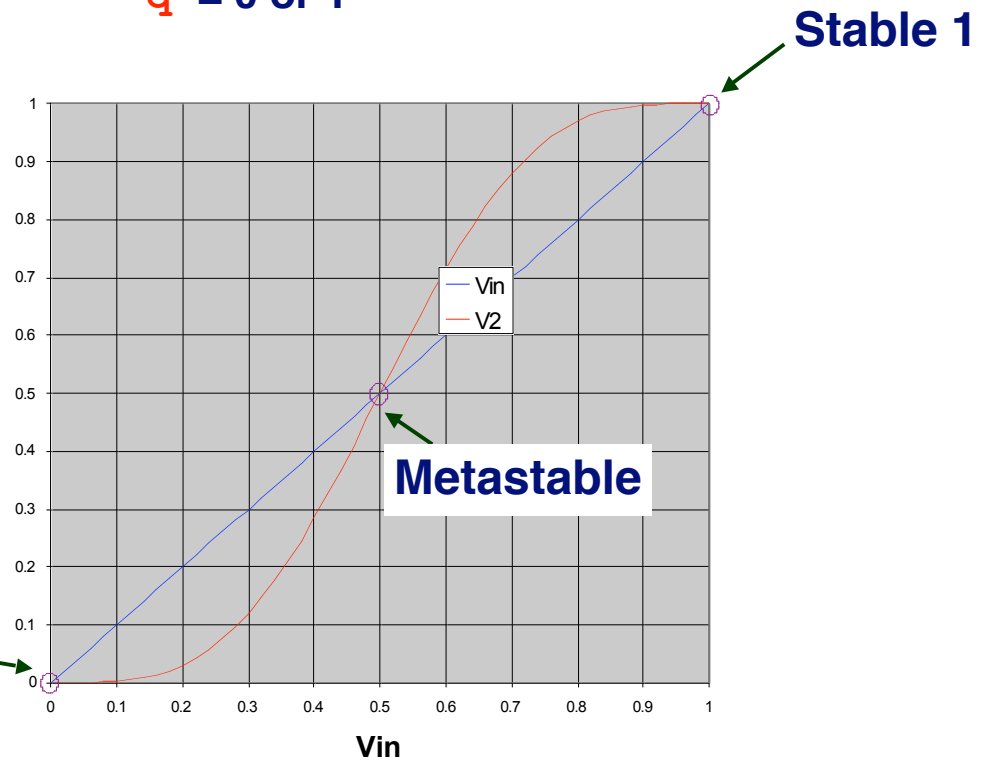


Storing 1 Bit (cont.)

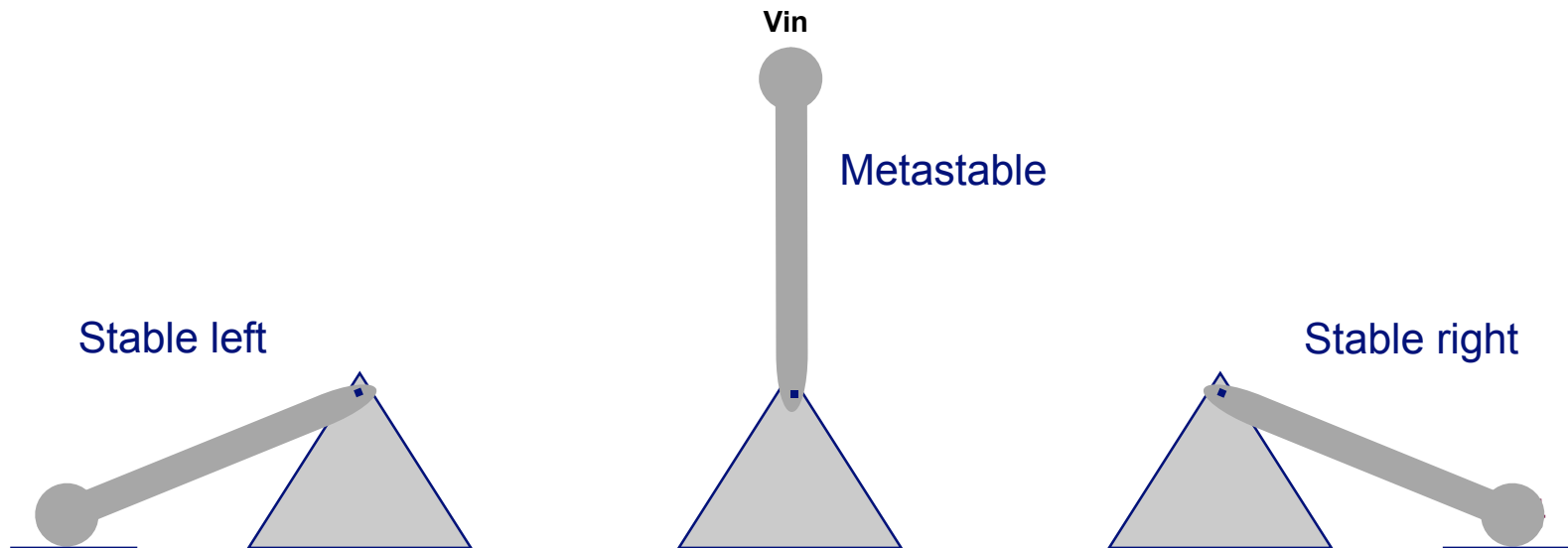
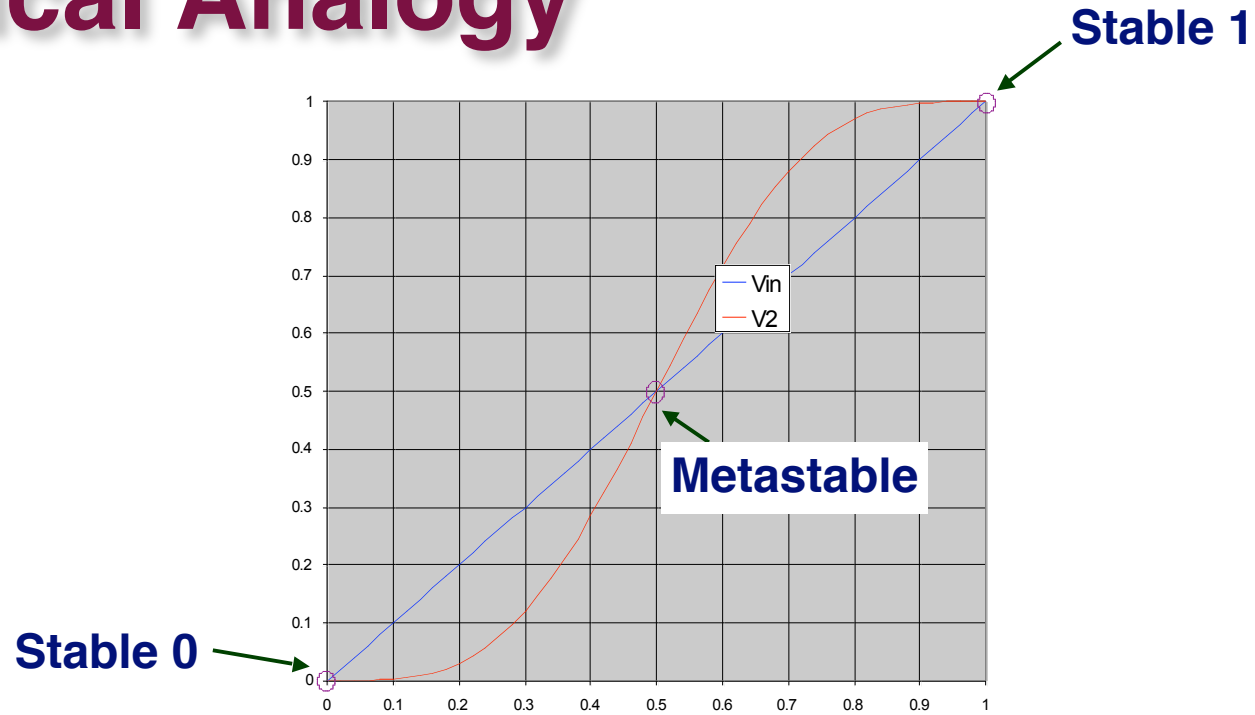
Bistable Element



Stable 0

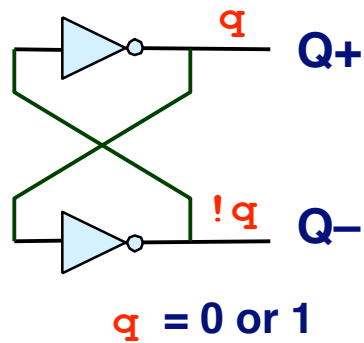


Physical Analogy

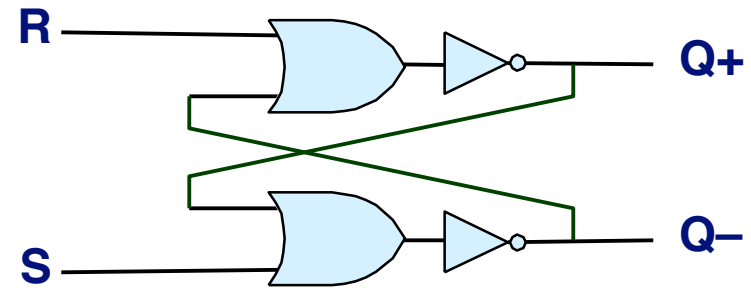


Storing and Accessing 1 Bit

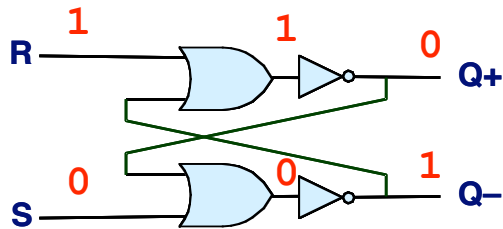
Bistable Element



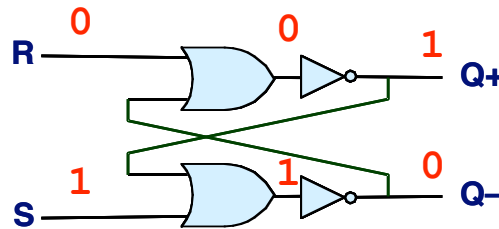
R-S Latch



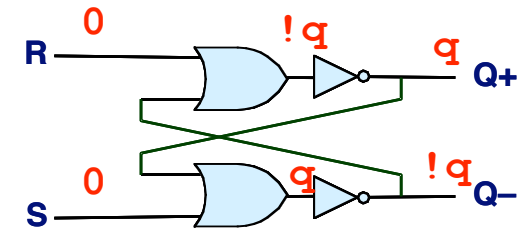
Resetting



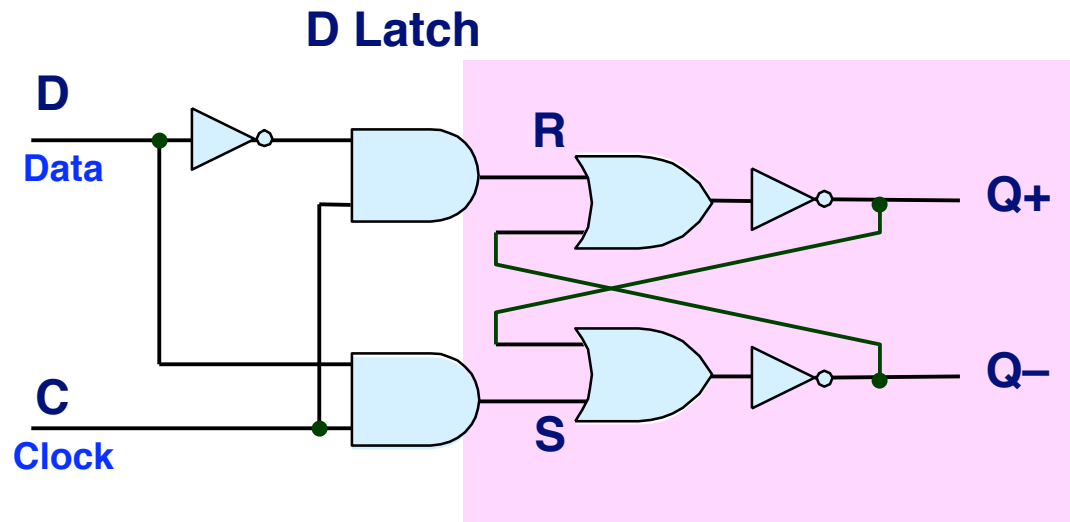
Setting



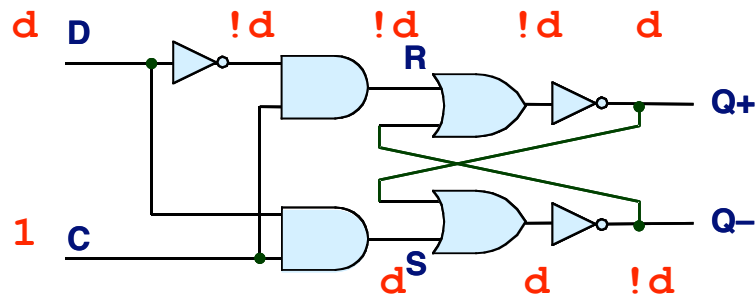
Storing



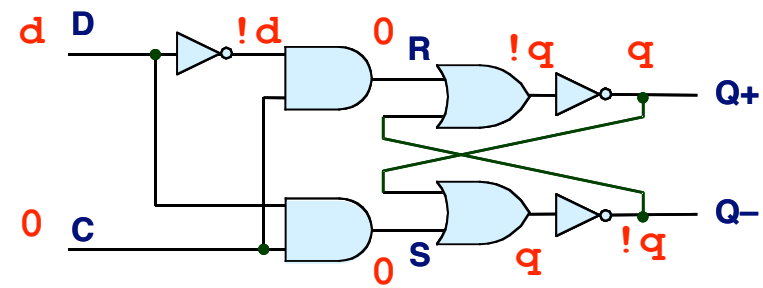
1-Bit Latch



Latching

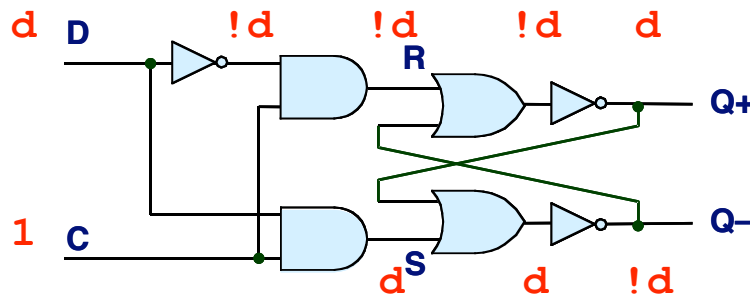


Storing

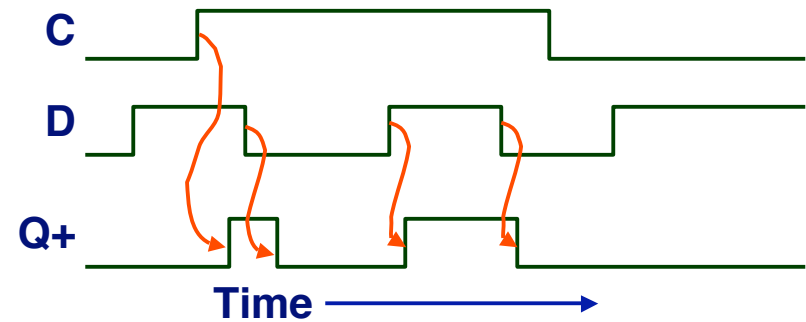


Transparent 1-Bit Latch

Latching

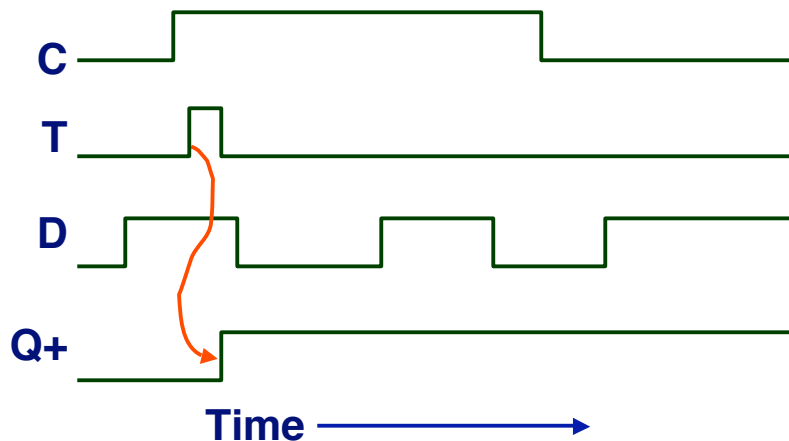
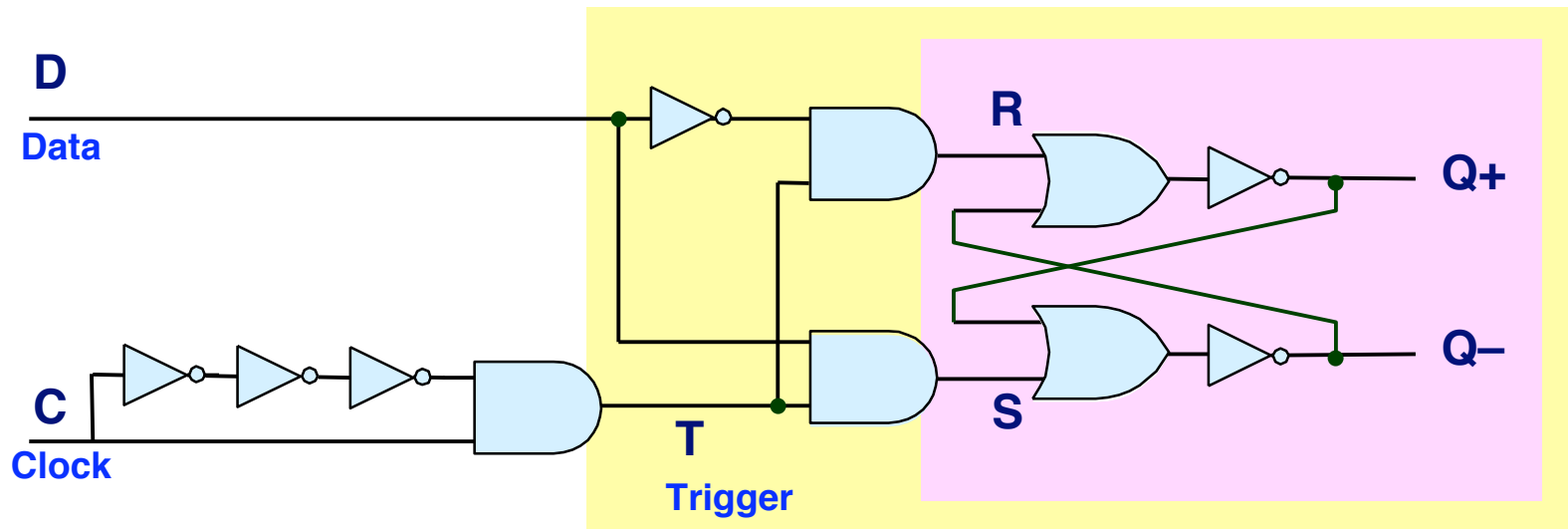


Changing D



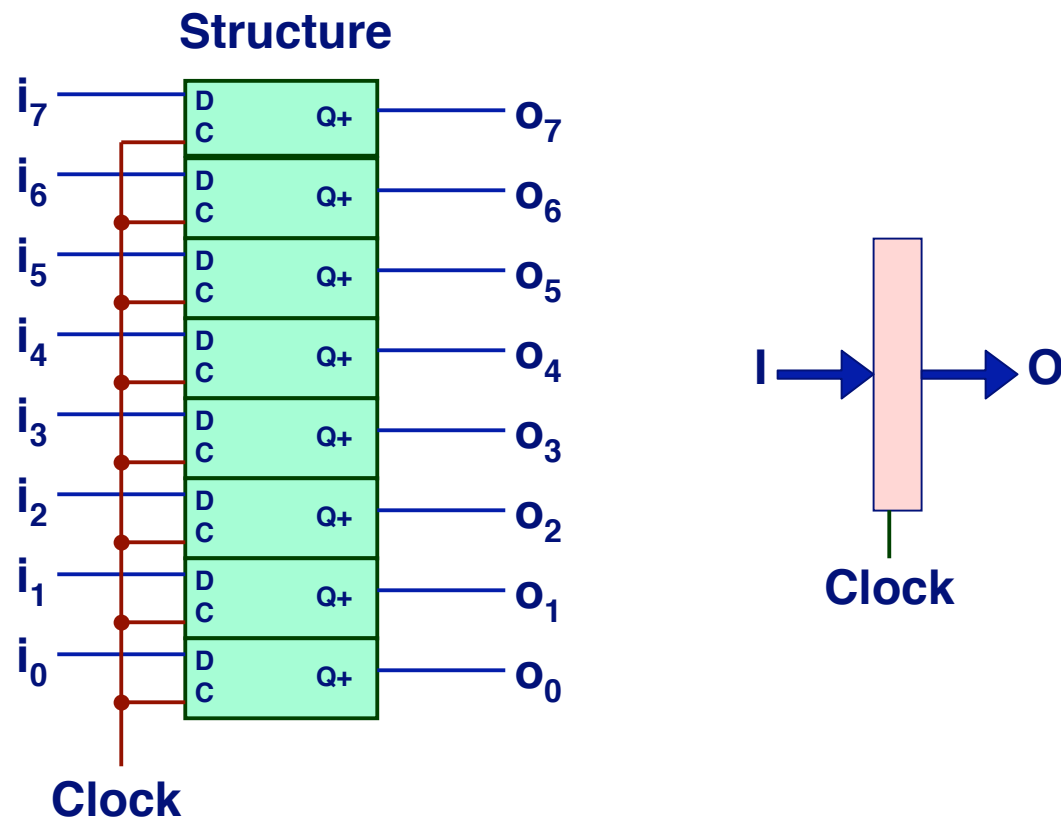
- When in latching mode, combinational propagation from D to $Q+$ and $Q-$
- Value latched depends on value of D as C falls

Edge-Triggered Latch



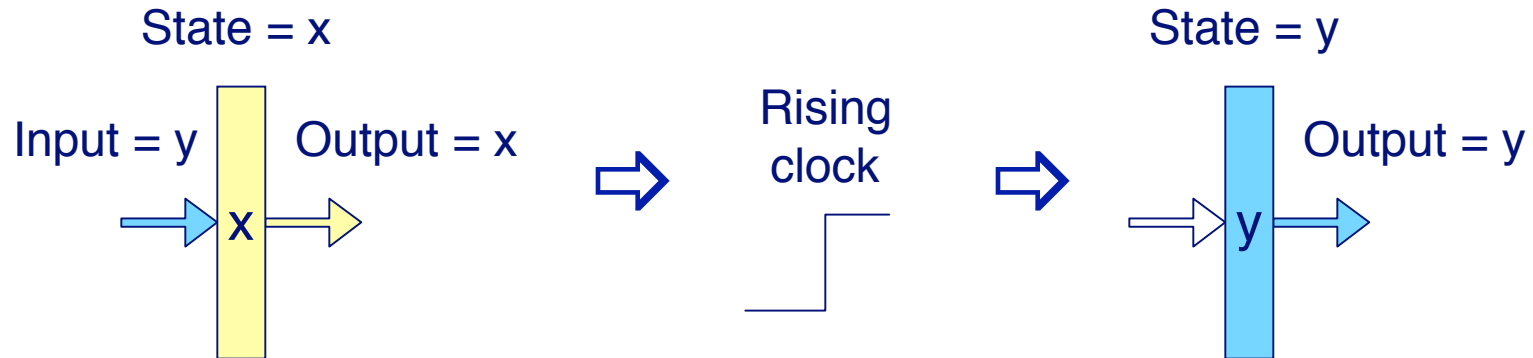
- Only in latching mode for brief period
 - Rising clock edge
- Value latched depends on data as clock rises
- Output remains stable at all other times

Registers



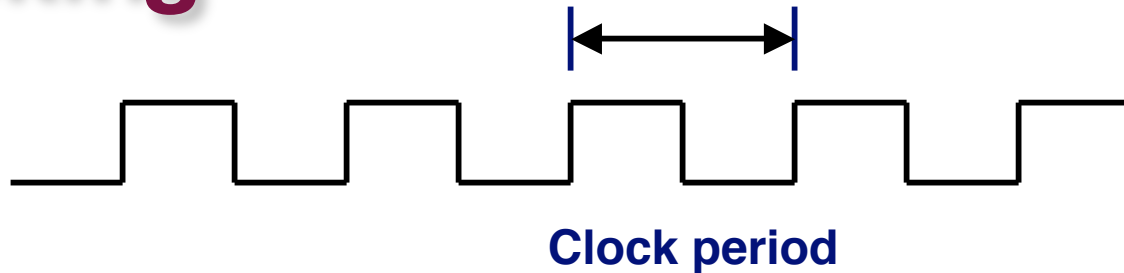
- Stores word of data
 - Different from *program registers* seen in assembly code
- Collection of edge-triggered latches
- Loads input on rising edge of clock

Register Operation



- Stores data bits
- For most of time acts as barrier between input and output
- As clock rises, loads input

Clocking



Need traffic control to make sure signals arrive in different places at the right time

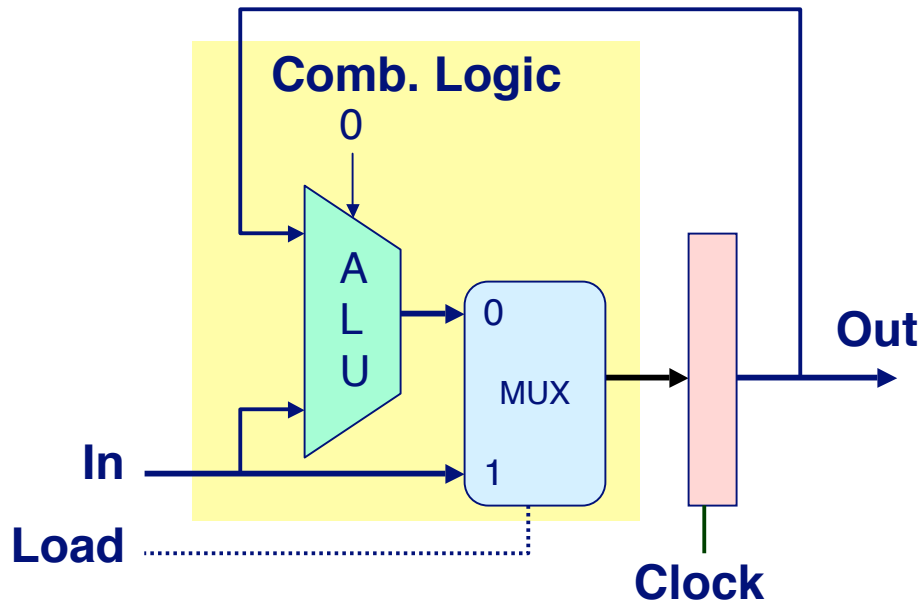
- Synchronous systems employ a clock
- Sometimes global
- Serves to enforce timing protocol across chip

Clock frequency = $1/\text{clock period}$

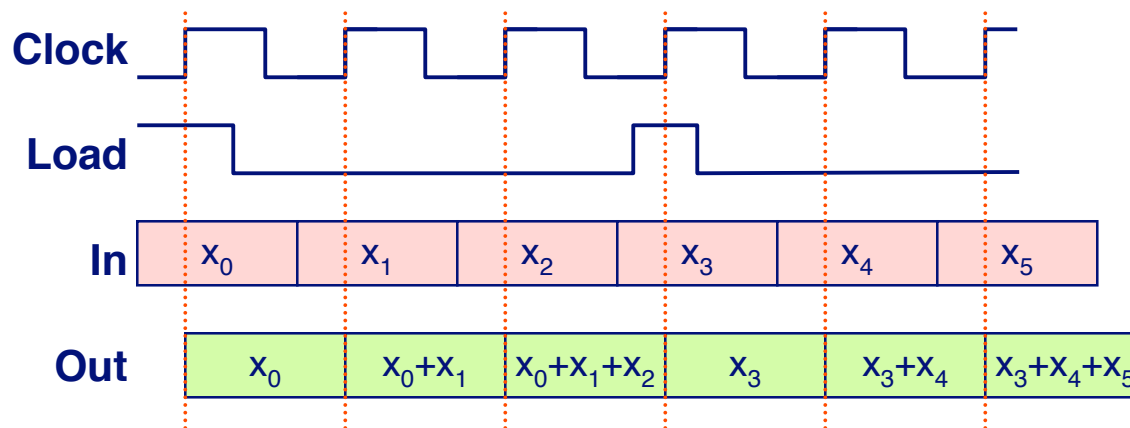
- Measured in cycles per second (Hertz)
- 1ns clock period \Rightarrow 1 GHz clock
- 200 picosecond period \Rightarrow 5 GHz clock

Historically - faster clock = faster computer (why?)

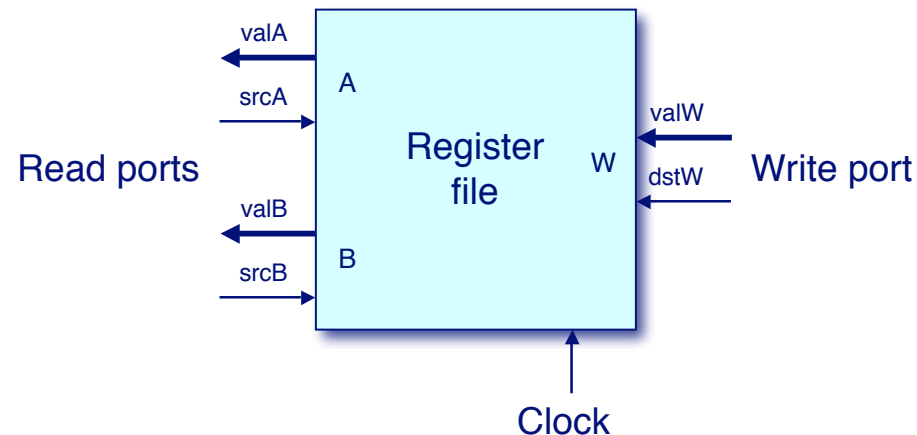
Simple State Machine Example



- Accumulator circuit
- Load or accumulate on each cycle

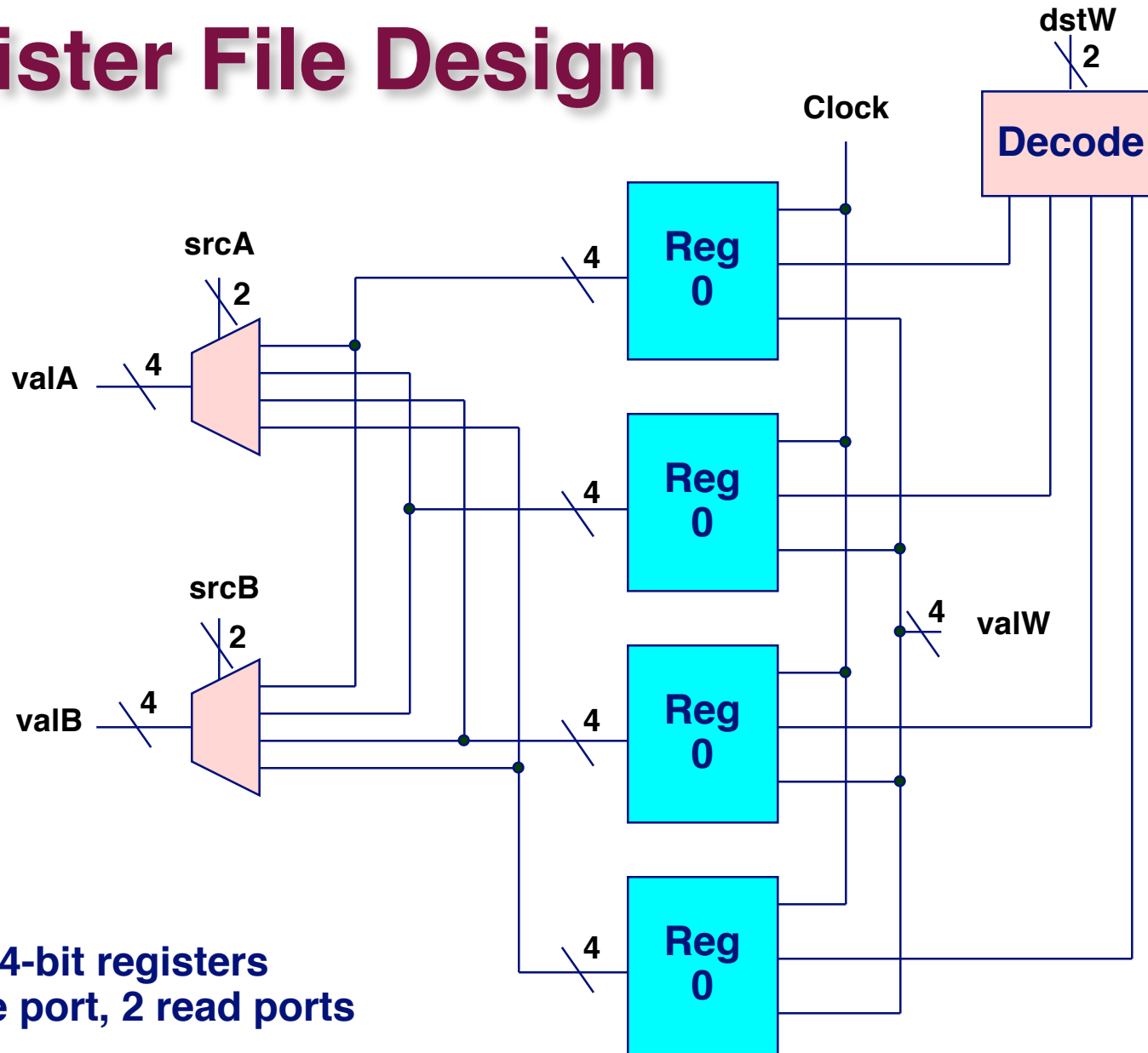


Random-Access Memory



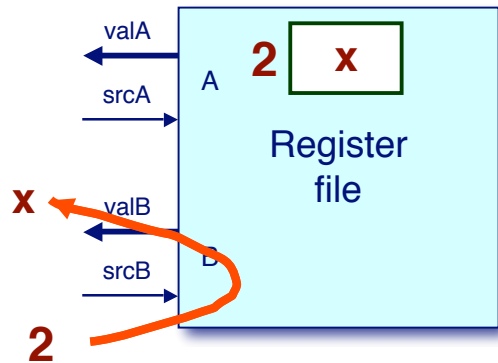
- **Stores multiple words of memory**
 - Address input specifies which word to read or write
- **Register file**
 - Holds values of program registers
 - `%eax`, `%esp`, etc.
 - Register identifier serves as address
 - » ID 8 implies no read or write performed
- **Multiple Ports**
 - Can read and/or write multiple words in one cycle
 - » Each has separate address and data input/output

Register File Design



4 4-bit registers
1 write port, 2 read ports

Register File Timing

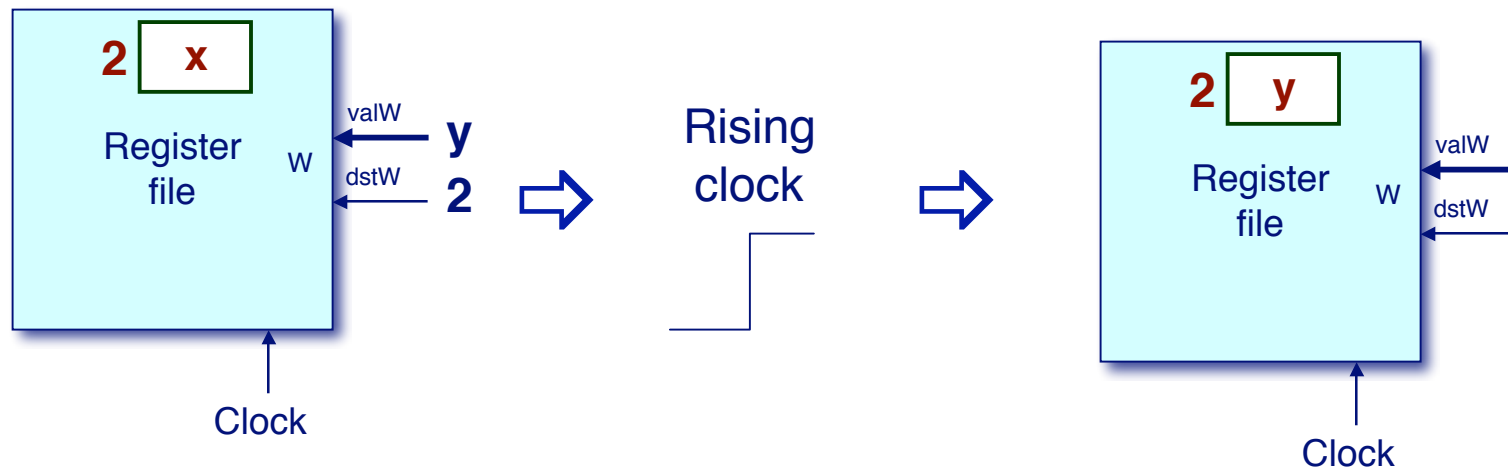


Reading

- Like combinational logic
- Output data generated based on input address
 - After some delay

Writing

- Like register
- Update only as clock rises



Register Files versus large RAM

Register files

- Small
- Multiported (sometimes 6-8 ports)
- Fast to access
- Addressed by word

Random Access Memory (SRAM, DRAM, etc.)

- Large
- Usually single-ported, sometime dual-ported
- Slower to access
- Addressed by byte (often accessed for many bytes)

Large RAM

How large is large?

- 2^{10} = Kilobyte
- 2^{20} = Megabyte
- 2^{30} = Gigabyte
- 2^{40} = Terabyte
- 2^{50} = Petabyte

Desktops today have a Gigabyte+ of DRAM, many clusters have a Terabyte+ of DRAM

SRAM: 6 transistors, data doesn't decay

DRAM: 1 capacitor/1 transistor, data must be refreshed

Memory organization

Logically a memory is a 2-D array

- Rows = number of addressible items
- Column width = # bits per entry in memory

“Addressability”

- Size of addressible item (column width)

“Address Space”

- Number of bits to specify number of entries (\log_2 Rows)

Reality

- Physical organization of memory on memory chips is much more complicated (multiple banks, chips, interleaving)
- Most memory access involve many bytes

Summary

Computation

- Performed by combinational logic
- Computes Boolean functions
- Continuously reacts to input changes

Storage

- Registers
 - Hold single words
 - Loaded as clock rises
- Random-access memories
 - Hold multiple words
 - Possible multiple read or write ports
 - Read word when address input changes
 - Write word as clock rises