Name: _____   **Score:** _____

(Please print)

EID: _____

In recognition of University regulations regarding academic dishonesty, I hereby certify that I have neither received nor given unpermitted aid on this examination.

Signed: _____

DIRECTIONS: Work on these sheets (both sides, if needed) only — **do not turn in any supplementary sheets of paper**. There is plenty of room for your answers.

1. (10 pts) True-False

_T_ (a) 1 bit of SRAM is larger than 1 bit of DRAM.

_F_ (b) DRAM is faster than SRAM.

_F_ (c) Registers are made out of DRAM.

_T_ (d) P-type transistors pass strong 1's and weak 0's.

_F_ (e) It is okay for the output of a logic gate to have an unknown value.

_F_ (f) Only a voltage that is exactly at VDD can be interpreted as logic 1.

_T_ (g) The threshold voltage of an N-type transistor is less than VDD and greater than 0.

_T_ (h) A 1-gigabit RAM chip with 4 data I/O pins needs fewer pins for addresses than a 1-gigabit RAM chip with 1 data I/O pin.

_F_ (i) A 1-gigabit RAM chip with 4 data I/O pins needs fewer pins overall than a 1-gigabit RAM chip with 1 data I/O pin (considering only address and data pins).

_T_ (j) A 32-bit word addressable machine with a 64-bit address space can store more data than an 8-bit byte addressable machine with a 64-bit address space.

2. (10 pts) Perform the following conversions:

    (a) 101101 unsigned base 2, to base 10

       45

    (b) 101101 1's complement, to base 10

       −18

    (c) 101101 2's complement, to base 10

       −19

    (d) 57 base 10, to base 16

       0x39

    (e) 57 base 10, to base 2

       111001

3. (10 pts) Perform each of the arithmetic operations given. In each case, indicate whether or not there is an overflow, and, if not, give the answer in decimal. All numbers are in 2's complement.

    (a) $1011 + 1111$

       $1010 = -6$

    (b) $1011 + 1000$

       overflow

    (c) $0011 + 1000$

       $1011 = -5$

    (d) $0011 + 0110$

       overflow

    (e) $1011 - 1000$

       overflow (but the answer is right, $0011 = 3$)

4. (10 pts) Consider a single-precision floating-point format in which 32 bits in a word are divided up as shown, with the high-order bit the sign bit, the next seven bits the exponent, and the final 24 bits the mantissa. The exponent is represented in excess 64 (no, I didn't mean excess 63). The binary point is at the left of the mantissa, so the mantissa is a fraction, and no leading digits are suppressed, unlike IEEE floating point. The entire number is signed-magnitude, just as in IEEE floating point. There are no special cases, unlike IEEE floating point.

Sign	Exponent 7 bits	Mantissa 24 bits
31		0
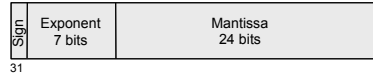
(a) (5 pts) Show the representation of the decimal number 15 in this format. Express your answer in hexadecimal.

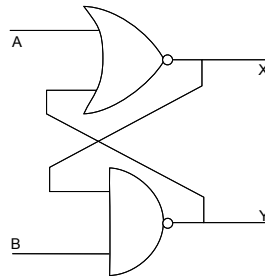$.1111 \times 2^4 \to$ **0100 0100 1111 0000 0000 0000 0000 0000 $\to$ 0x44F00000**

(b) (5 pts) What is the largest number that can be represented in this format? Use binary scientific notation to express this number.

0111 1111 1111 1111 1111 1111 1111 1111 1111 $\to$
$0.1111\ 1111\ 1111\ 1111\ 1111\ 1111 \times 2^{63} =$
$1.111\ 1111\ 1111\ 1111\ 1111\ 1111 \times 2^{62}$

5. (10 pts) Consider the following circuit:

(a) (5 pts) Analyze the dynamic behavior of the circuit. Summarize your results by filling in the truth table for the circuit.

| A	B	X	Y
0	0	0	1
0	1	X	Y
1	0	0	1
1	1	0	1

(b) (5 pts) Could this circuit be used as a memory circuit? Why or why not?

No. While it does have a stable state that retains a previously stored state (A=0, B=1), there is no way to set the circuit to any value other than X=0, Y=1.

6. (20 pts) Give a circuit diagram for a 4-bit shift register that can do 4 possible shifts. SHL shifts all bits to the left 1 position. The leftmost bit is lost, and a 0 is inserted at the right. ROL shifts all bits left 1 position, with the leftmost bit being "rotated" back to the rightmost position. SHR shifts all bits right 1 position. The new leftmost bit is a copy of the previous leftmost bit, and the rightmost bit is lost. ROR shifts all bits to the right 1 position, and the rightmost bit is "rotated" into the leftmost position. When the clock goes from low to high, the register should do one of these shifts if the control input SHIFT' is 0, otherwise it will do nothing. Which shift is done is determined by two other control inputs, L'/R which means shift right if 1, left if 0, and ROT, which means rotate if 1, otherwise not. You may use D flip-flops, multiplexors, decoders, and logic gates as the elements of your circuit diagram.
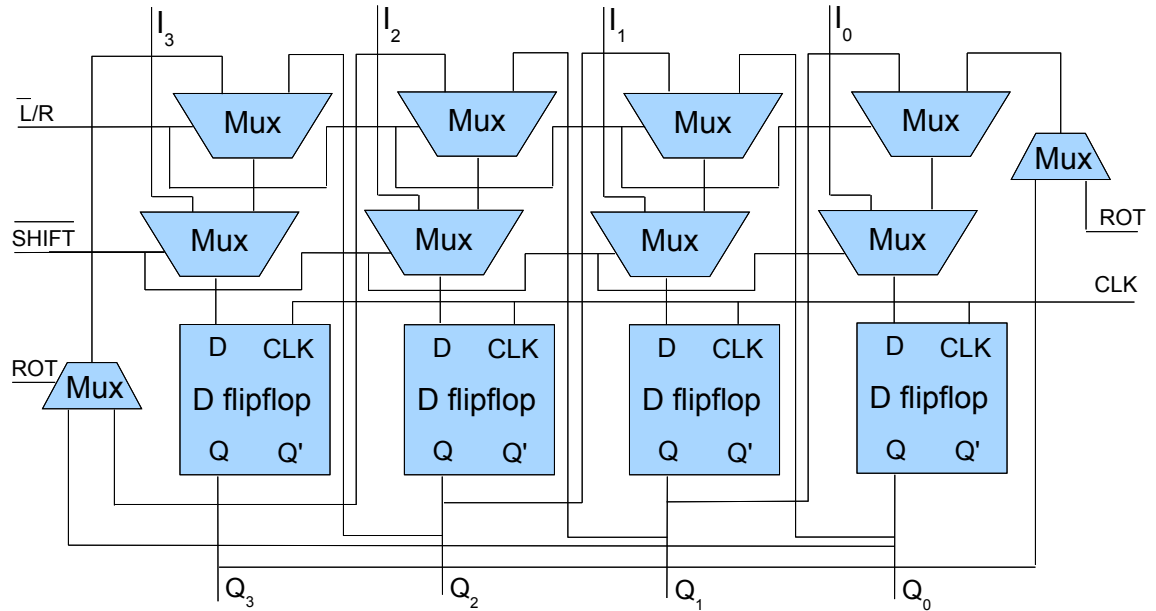
7. (30 pts) You are designing a controller for a factory-floor mail-delivery robot. The robot mail cart can pick up and deliver mail at any of the 4 stations on the floor, as shown. The numbers shown at each station are the addresses of the respective stations. From any station, a person can summon the robot to that station by entering the address of the station. When the robot arrives, the person can put mail in its basket and send it to another station, again by entering the address of that station. The robot will compare its current address to the destination address entered to decide whether to go N, S, E, or W. As long as the current address doesn't match the destination address, it will continue rereading the destination address as input at each step. If it finds that its current address matches the destination address, it will stay where it is and discard the destination address it had been reading in order to read the next one. So, the controller takes as input the destination address, and it produces as output four signals, which move itself N, S, E, or W when the respective output line is high (1). If the robot has two possible moves (the diagonal case), it should always take the horizontal (E or W) move. You may assume that it starts at location 0,0.
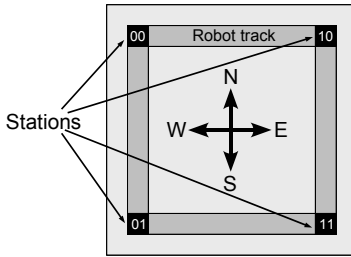
(a) (10 pts) Give a state diagram for a controller that operates this way. Use a Mealy machine, in which outputs are determined by the transition edges, rather than a Moore machine (as in the book), in which outputs are determined by the states. This will make your task considerably simpler.
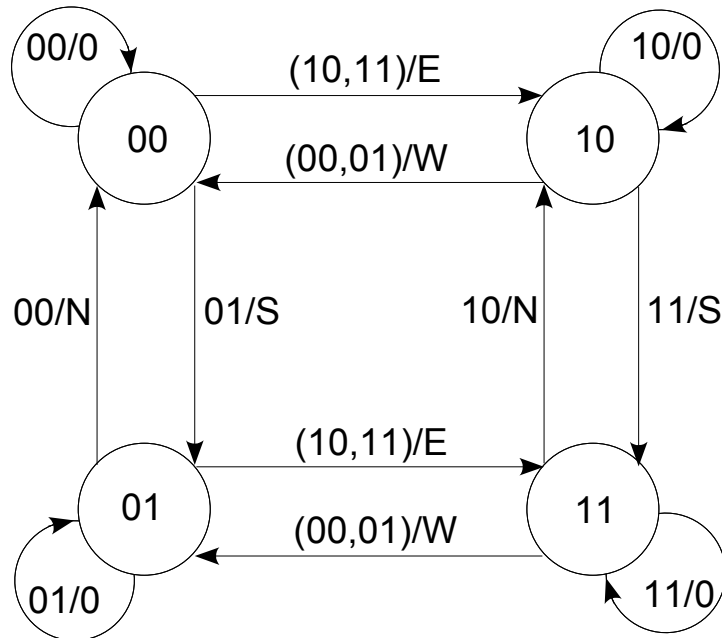
(b) (10 pts) Assign binary encodings to the states of this machine. Use the obvious scheme involving location addresses. How many bits are needed to implement the controller? Draw the table for the next state function for the current horizontal address bit and the W output.

D_h D_v C_h C_v	C_{hn} C_{vn}	N S E W
0 0 0 0	0 0	0 0 0 0
0 0 0 1	0 0	1 0 0 0
0 0 1 0	0 0	0 0 0 1
0 0 1 1	0 1	0 0 0 1
0 1 0 0	0 1	0 1 0 0
0 1 0 1	0 1	0 0 0 0
0 1 1 0	0 0	0 0 0 1
0 1 1 1	0 1	0 0 0 1
1 0 0 0	1 0	0 0 1 0
1 0 0 1	1 1	0 0 1 0
1 0 1 0	1 0	0 0 0 0
1 0 1 1	1 0	1 0 0 0
1 1 0 0	1 0	0 0 1 0
1 1 0 1	1 1	0 0 1 0
1 1 1 0	1 1	0 1 0 0
1 1 1 1	1 1	0 0 0 0

(c) (10 pts) Give minimal sum of products expressions for the next state function for the current horizontal address bit and for the W output. Use Karnaugh maps if necessary.

$$\mathbf{C_{hn} = D_h}$$

$$\mathbf{W = C_h \overline{D_h}}$$