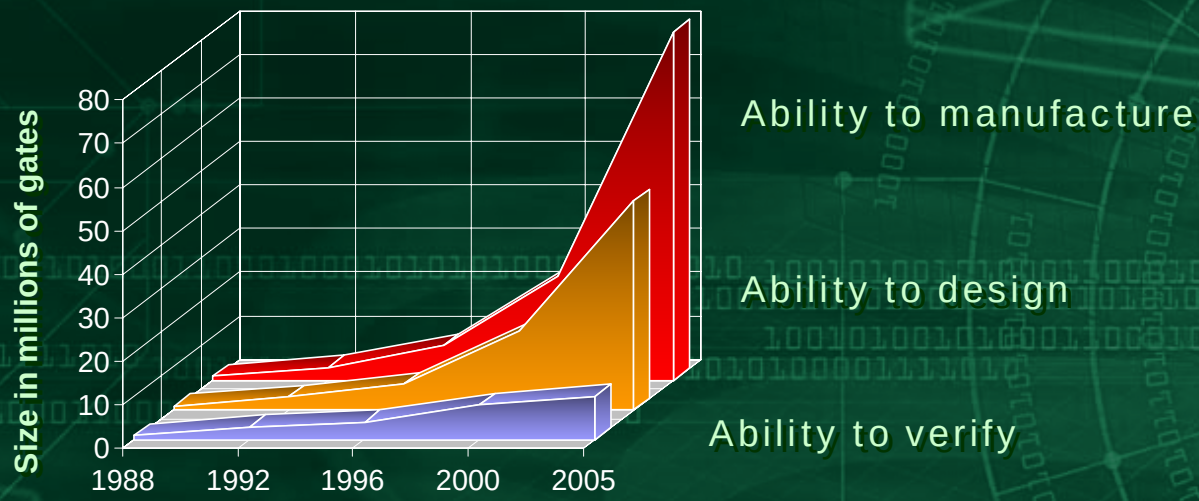
Formal Verification: *A Business Perspective*

The industry is lacking the equivalent of a design synthesis breakthrough in the area of functional verification



[Collett International 2004]

Harry Foster

Chief Technologist

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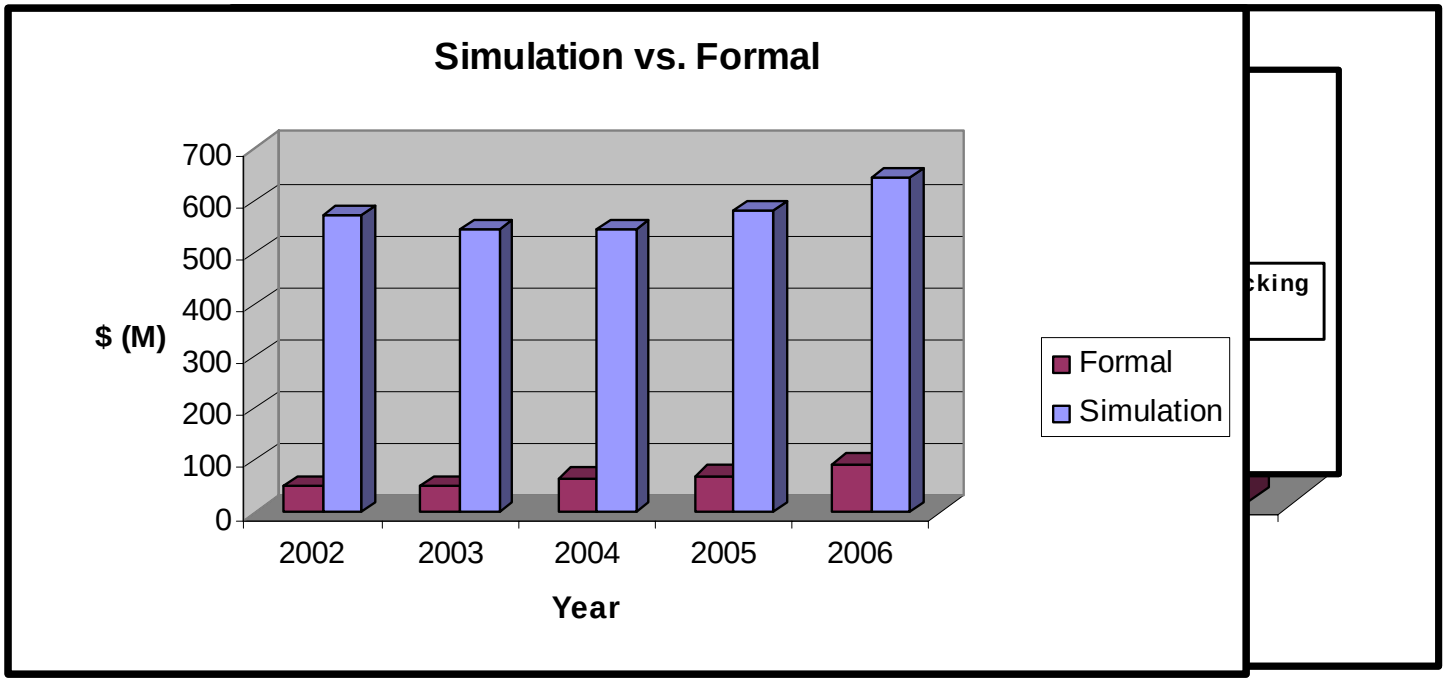
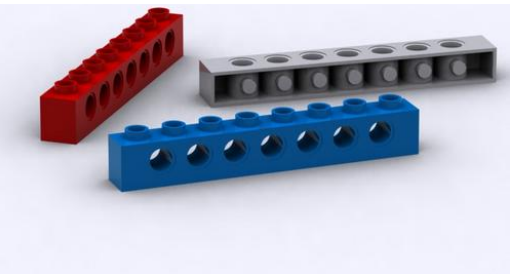
Show Me The Money. . . .



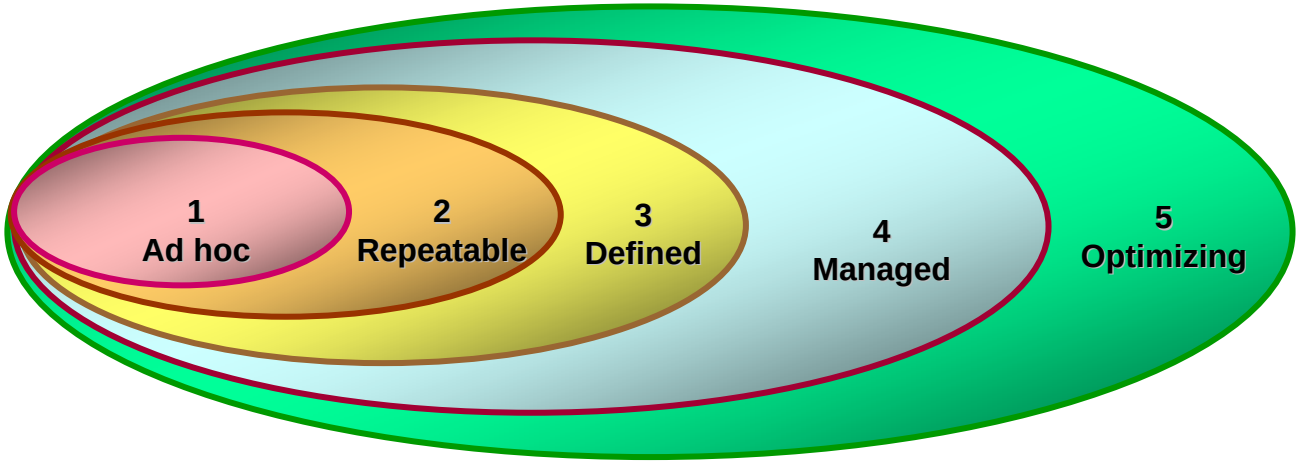
Question

Could an organization with ad hoc methodologies successfully build a reusable object-oriented constrained-random coverage-driven testbench. . . .repeatedly?

Could an organization lacking sufficient skills formally prove a cache controller?



Capability Maturity Model



Level 1

- Ad-hoc processes and testplans
- Directed test
- Few or no metrics to measure success

Level 2

- Testplans and reviews
- Directed & random simulation
- Linting
- **Simulation ABV**
- Metrics: code coverage
- ***Improved predictability***

Level 3

- Processes defined
- Constrain-random coverage driven simulation
- Clock-Domain Checks
- **Simple formal**
- Functional coverage
- ***Improved productivity and quality***

Level 4

- Processes tracked
- Transaction-level testbenches (OVM)
- Advanced formal
- Internal and external IP use
- **Advanced formal**
- Requirement to verification traceability
- Metrics tracking system in place
- ***Improved quality***

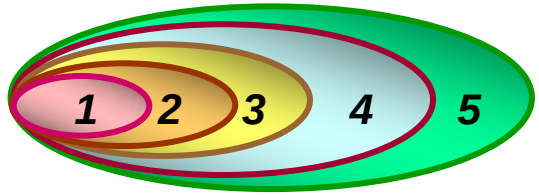
Level 5

- Optimizing
- Higher-level assertions proved on blocks
- Identify missing metrics required for optimization
- Continual review and refine processes
- ***Reduce cost***

- **Value**
- **Infrastructure**
- **Skills**
- **Resources**

Levels of maturity

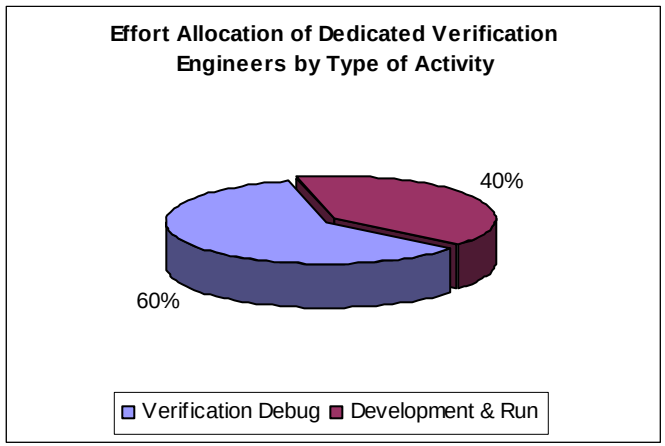
What's easy and hard

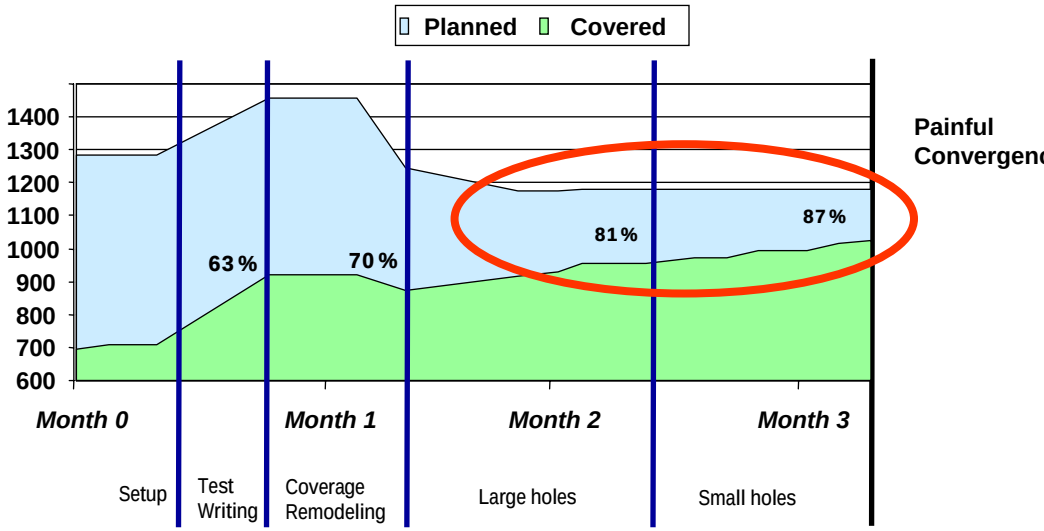


Design Block	Level of Maturity	Difficulty
Arbiter	3	Easy
Timing Controller	3	Easy
AHB Bus Bridge	3	Easy
SRAM Controller	3	Easy
AXI Bus Bridge	3	OK
SDRAM Controller	3	OK (more difficult with data integrity)
DDR Controller	3-4	Medium (more difficult with data integrity)
DDR2 Controller	3-4	Medium
USB Controller	4	Difficult (long latency)
Cache Controller	4	More Difficult
PCI-Express	4	Hard (complex & long latency)
JPEG/MPEG	-	NO-GOOD-FOR-MODEL-CHECKING
DSP	-	NO-GOOD-FOR-MODEL-CHECKING
Ecription	-	NO-GOOD-FOR-MODEL-CHECKING
Floating-Point Unit	-	NO-GOOD-FOR-MODEL-CHECKING

Research Opportunities

Debug and Coverage Closure Are Big Problems!



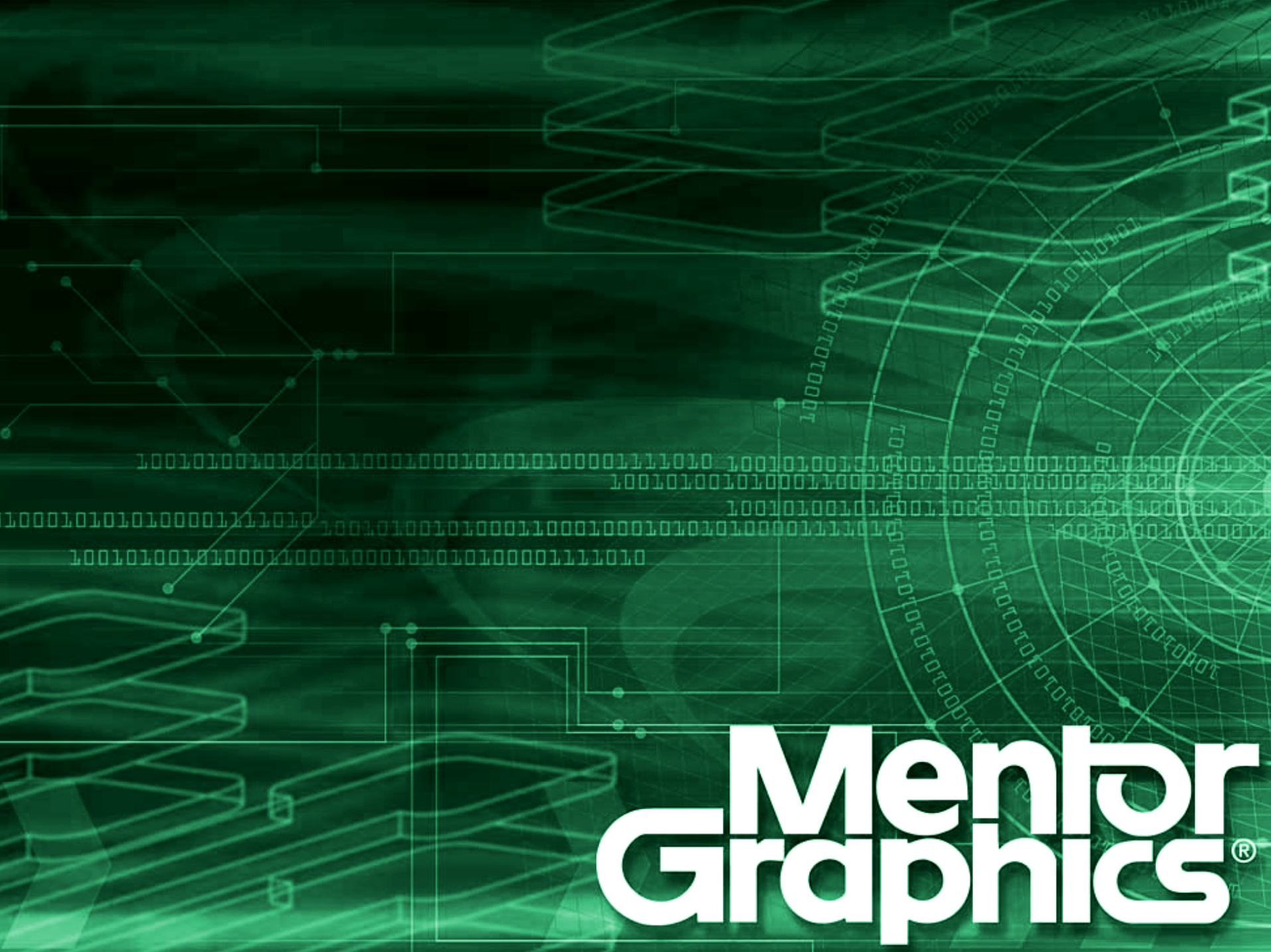


[SystemVerilog Constrained Random Environment]

Source: 2004/2002 IC/ASIC Functional Verification Study, Collett International Research, Used with Permission

Position Statement

- Formal Business Today
  - Automatic Applications
    - Clock-Domain Checking, Equivalence Checking, Timing, Power
    - Does not require mature skills, easy adoption (*Level 3*)
  - Property Checking
    - Assurance, high ROI, mature skills required (*Level 4*)
    - Bug hunting, hot spots, low effort (*Level 3*)
- Formal Tomorrow
  - Reduce barrier to adoption, more automatic applications, more to a verification appliance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