FMCAD 2007 Panel

Formal Verification:
A Business Perspective

November 11, 2007

Aarti Gupta
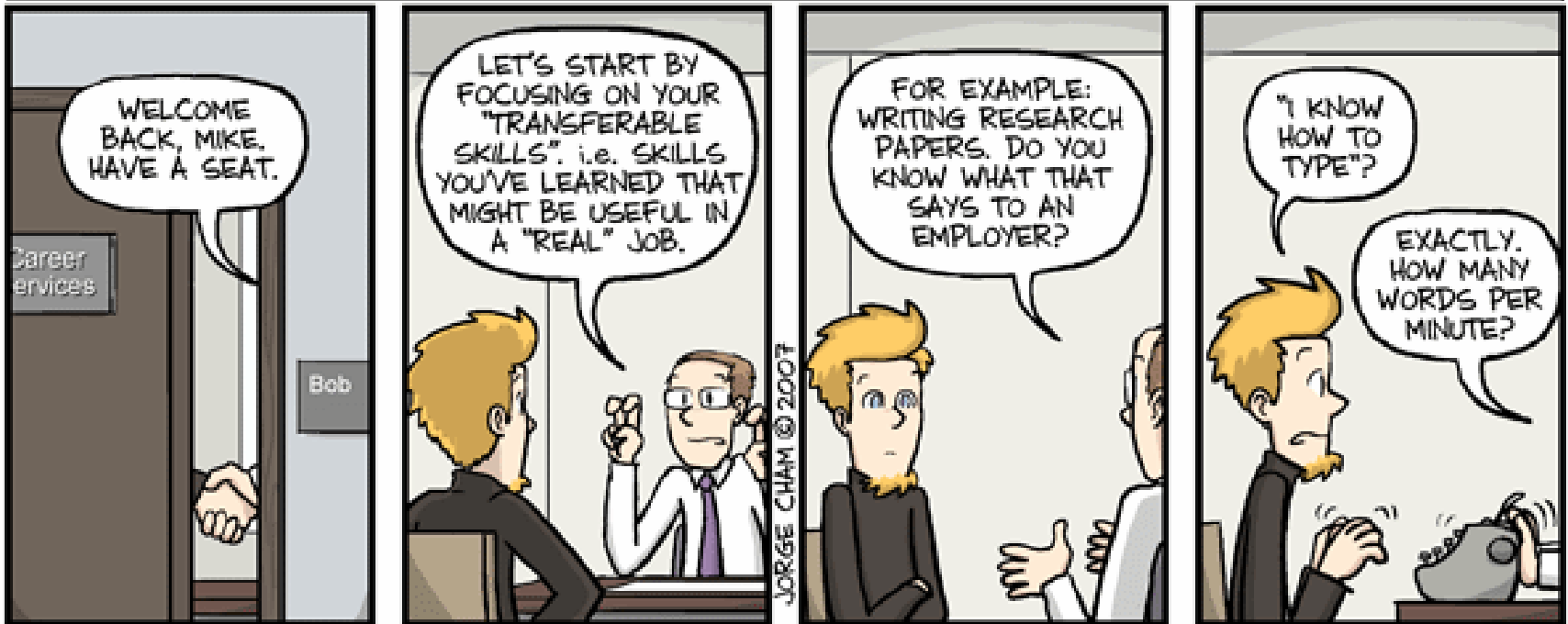NEC Labs America

FV Business Timeline
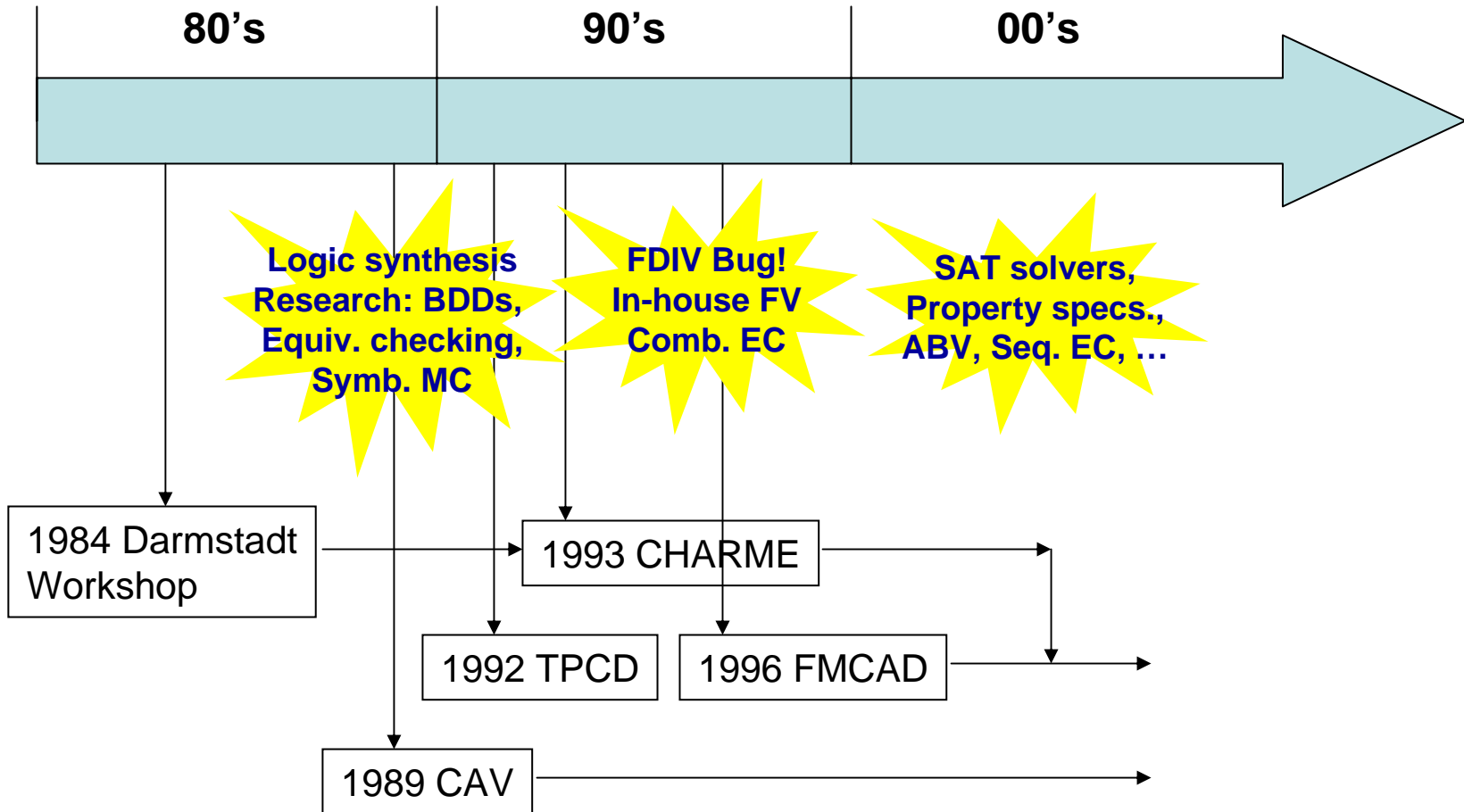
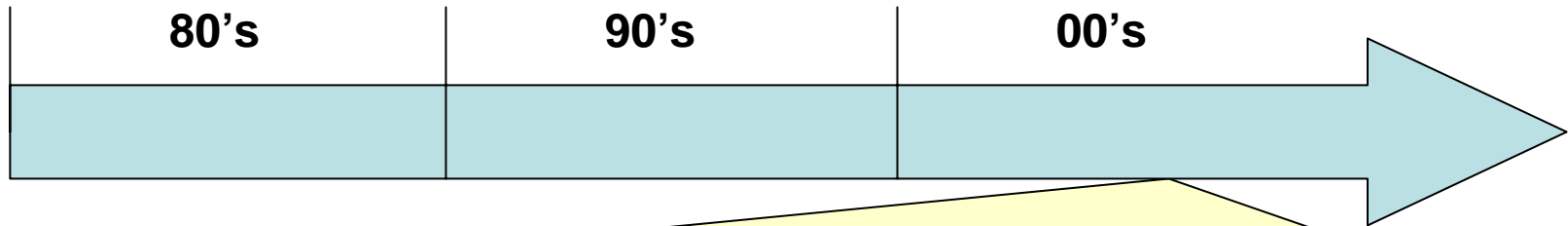# FV Business Timeline

80's	90's	00's

**Logic synthesis
Research: BDDs,
Equiv. checking,
Symb. MC**

**FDIV Bug!
In-house FV
Comb. EC**

**SAT solvers,
Property specs.,
ABV, Seq. EC, …**

1984 Darmstadt
Workshop

1993 CHARME

1992 TPCD

1996 FMCAD

1989 CAV

FV Business Timeline

80's	90's	00's

Here we are today …

http://shemesh.larc.nasa.gov/fm/fm-humor.html
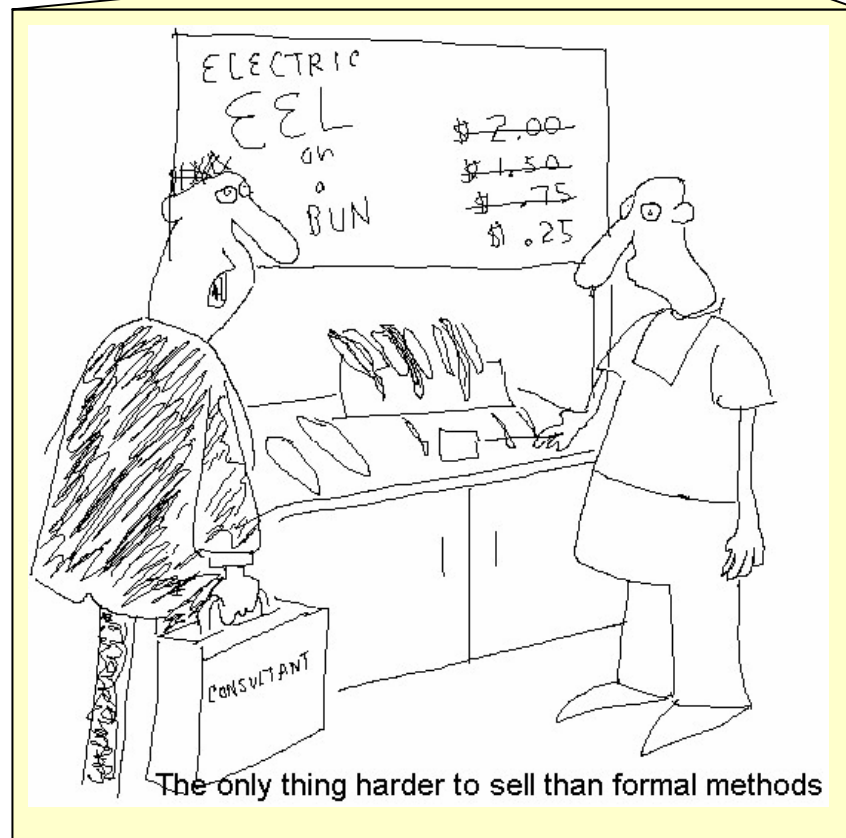
FV Business Timeline
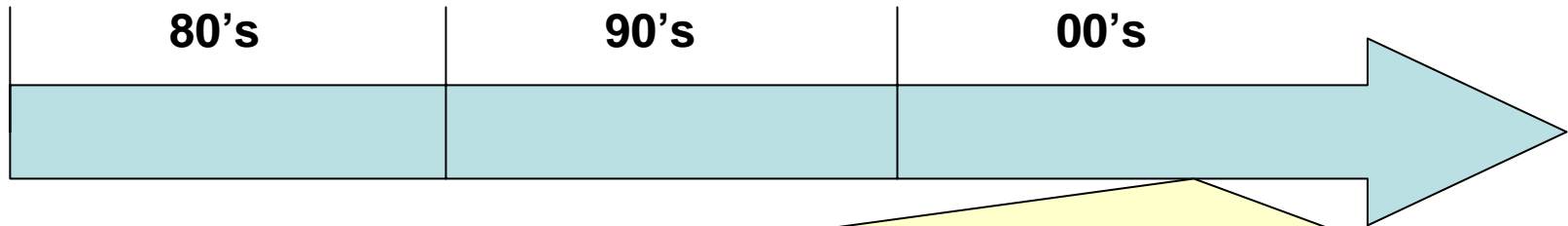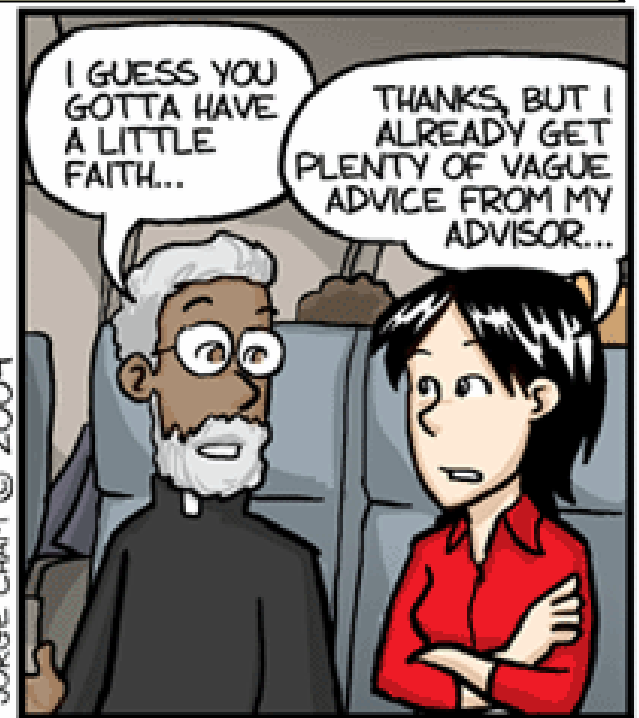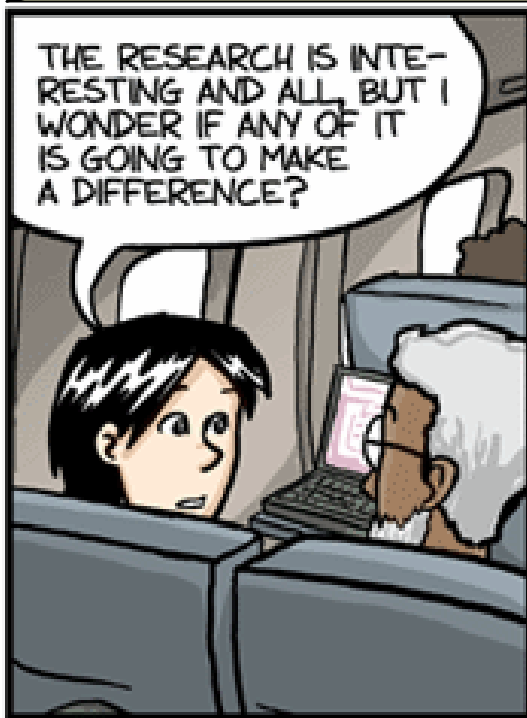
Panelists

- Husam Abu-Haimed, Nvidia
- Harry Foster, Mentor Graphics
- Robert Kurshan, Cadence
- Hillel Miller, Freescale Semiconductor
- Prakash Narain, Real Intent
- Rajeev Ranjan, Jasper Design Automation

- Initial Idea: Rajeev Ranjan
- Organizers: Mary Sheeran, Jason Baumgartner
- Moderator: Aarti Gupta

Questions for Panelists

- **1. The current status of acceptance of FV technology**

- **2. Who are the users of FV technology (designers, DV engineers, expert FV folks), and how does FV fit in their primary job responsibility?**

- **3. What are the key roadblocks/barriers faced by the users of FV?**

- **4. What are the challenges in building an FV market (how do management folks determine the ROI)?**

- **5. Are there other novel applications of formal technology on the business horizon?**

- **6. What are the key areas of research that are most relevant from a business stand point?**