

Call For Participation



FMCAD'08

Eighth International Conference on Formal Methods in Computer-Aided Design Portland, Oregon, United States, November 17-20, 2008

http://fmcad.org/2008/

FMCAD'08 Chairs:

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Tutorials:

Anna Slobodova (Intel)

Panels:

Carl Pixley (Synopsys)

Local Arrangements:

Annette Bunker (Intel)

Publicity:

Lee Pike (Galois)

Steering Committee:

Jason Baumgartner (IBM) Aarti Gupta (NEC) Warren Hunt (UT Austin, chair) Pete Manolios (Northeastern U.) Mary Sheeran (Chalmers)

Important Dates:

Early Registration Deadline: October 14, 2008 Hotel Registration Deadline: October 18, 2008

Conference Overview:

FMCAD 2008 is the eighth in a series of conferences on the theory and application of formal methods in hardware and system design and verification. In 2005, the bi-annual FMCAD and sister conference CHARME decided to merge to form an annual conference with a unified community. The resulting unified FMCAD provides a leading international forum to researchers and practitioners in academia and industry for presenting and discussing groundbreaking methods, technologies, theoretical results, and tools for formally reasoning about computing systems, as well as open challenges therein.

Local Information:

The Conference will be held at the Embassy Suites (Downtown) in Portland, Oregon. We have negotiated a special rate with the hotel for conference attendees. Please book early to secure the reduced rate. For details, please see the conference web page. A dinner cruise on the Willamette River is planned.

Technical Program:

The technical program is available at the conference web page. It includes 2 invited keynotes, 4 invited tutorials, 24 regular papers, 4 short papers, and 2 panels.

• Keynotes:

- Ken McMillan (Cadence): Interpolation Theory and Applications
- Carl Seger (Intel): Formal Methods and Physical Design: Match Made in Heaven or Fools' Paradise?
- Tutorials:
 - Kevin Jones (Rambus): Analog and Mixed Signal Verification: The State of the Art and some Open Problems
 - Moshe Levinger (IBM): Building a Bridge: From Pre-Silicon Verification to Post-Silicon Validation
 - Byron Cook (Microsoft): Computing Bounds on Space and Time for Hardware Compilation
 - David Hardin (Rockwell Collins): Considerations in the Design and Verification of Microprocessors for Safety-Critical and Security-Critical Applications

• Panels:

- High Level Design and ESL: Who Cares?
- The Future of Formal: Academic, IC, EDA, and Software Perspectives

Sponsors:

- Sponsored by: IEEE CEDA
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