Skipping Refinement

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Example of a Reactive System: Microprocessor

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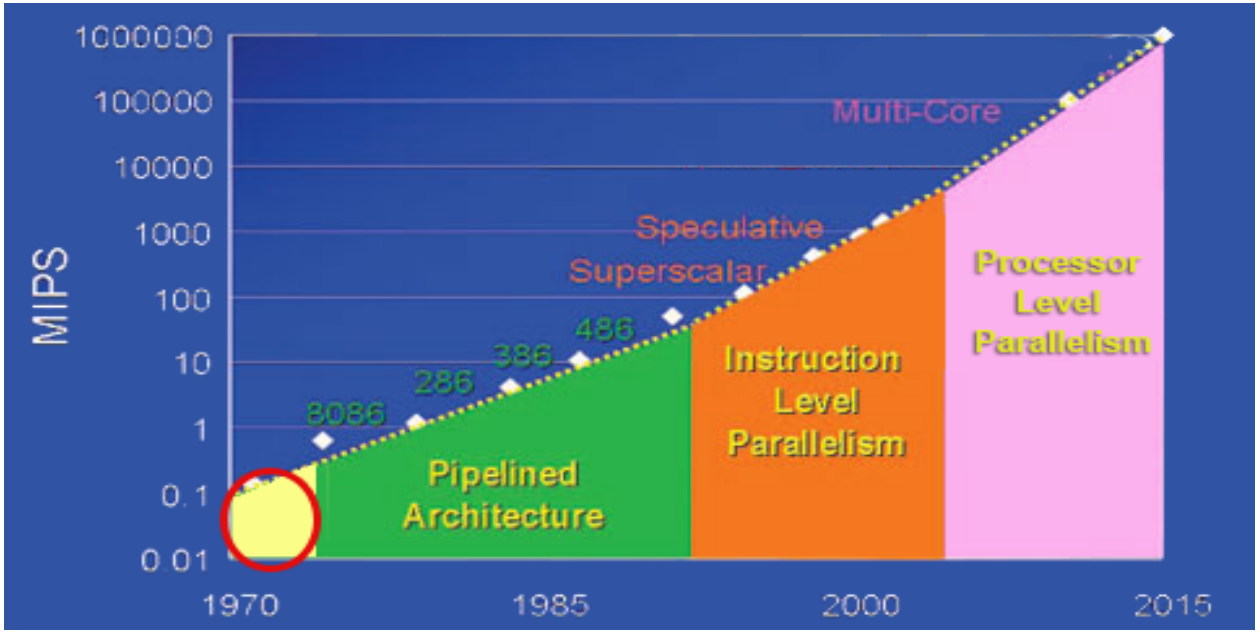
Instruction Set Architecture (ISA)

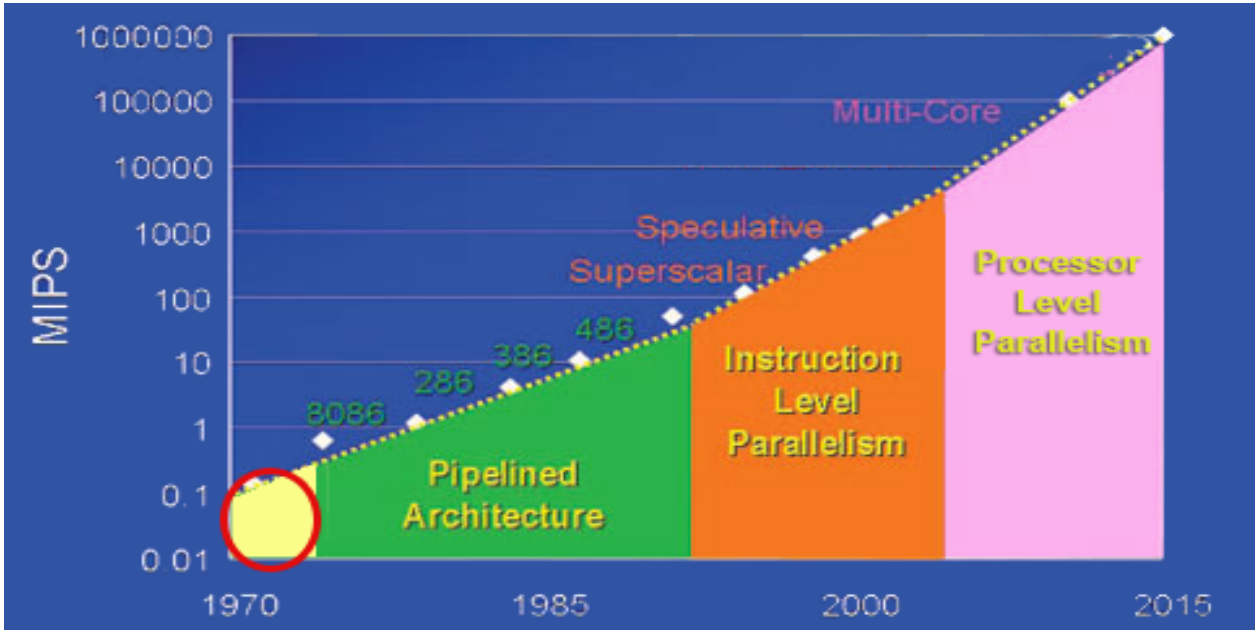
Natural Specification

- *add rd,ra,rb*
- *sub rd,ra,rb*
- *jnz imm*
- ...

First Generation Microprocessor

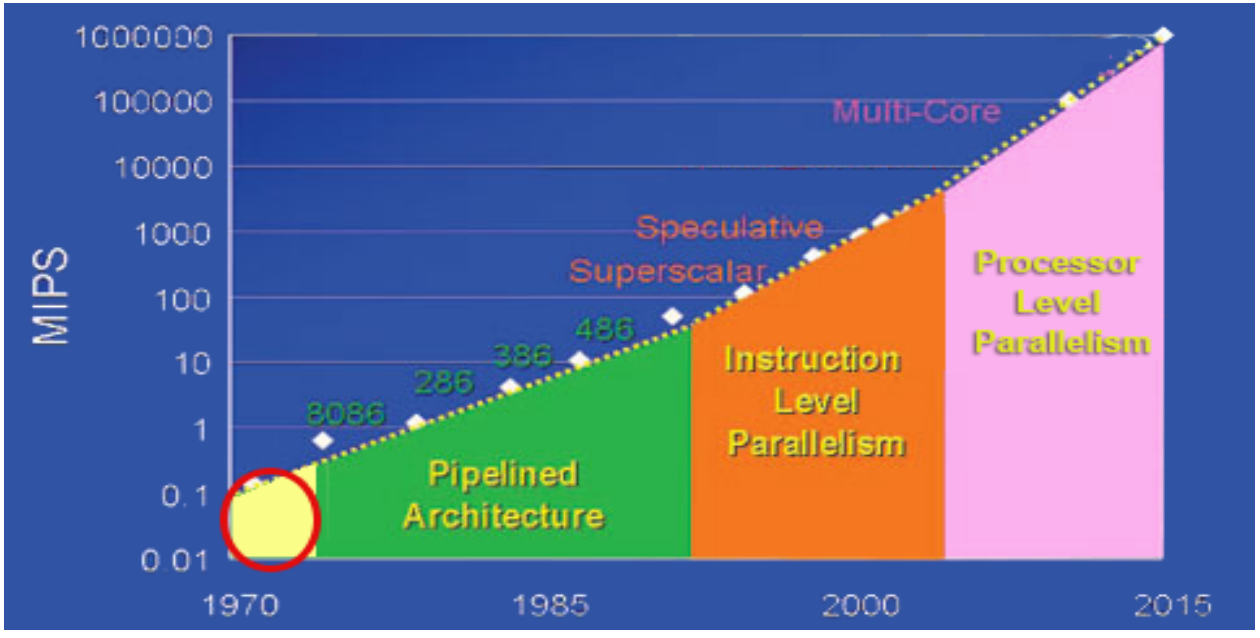


First Generation Microprocessor



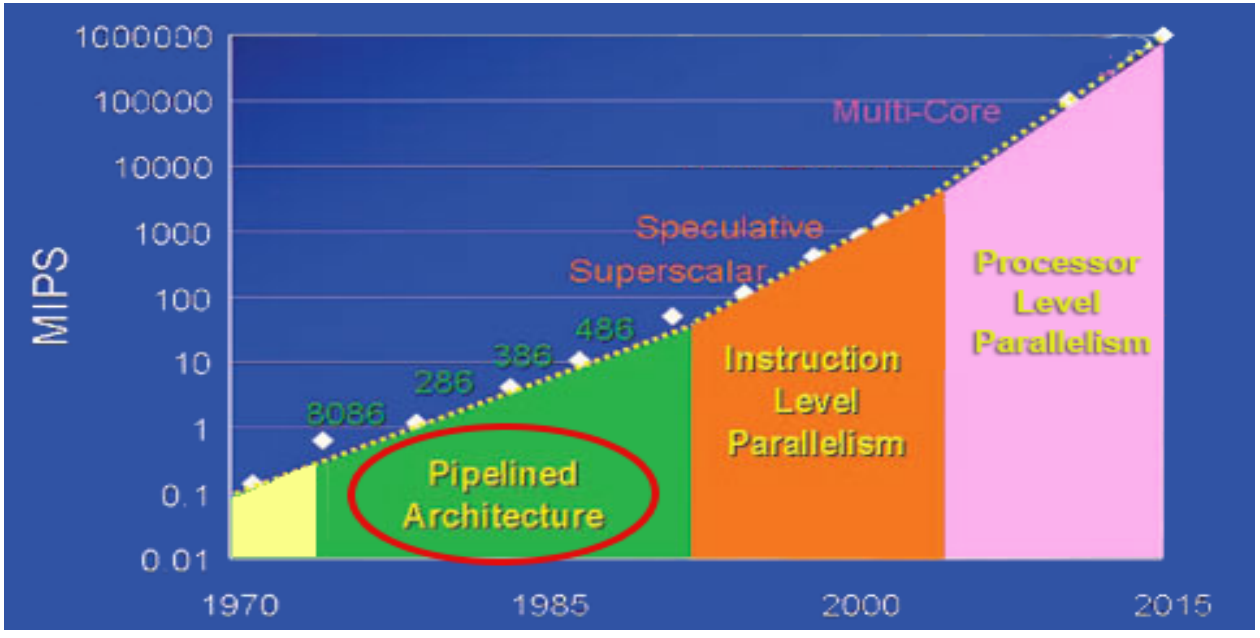
- Show that all behaviors of the implementation are behaviors of the specification.

First Generation Microprocessor



- Show that all behaviors of the implementation are behaviors of the specification.
- Simulation Refinement [Milner and Park 1981]

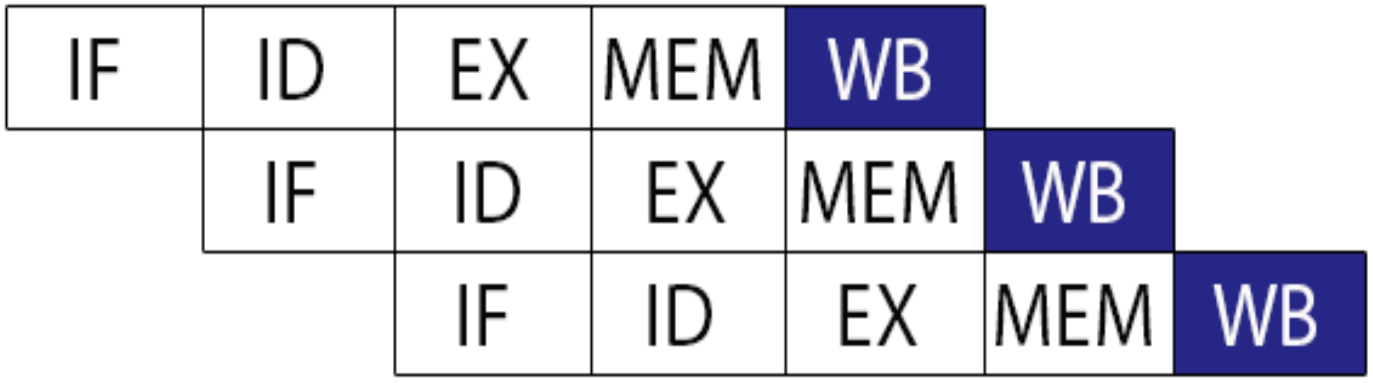
Pipelined Microprocessor



Optimizations

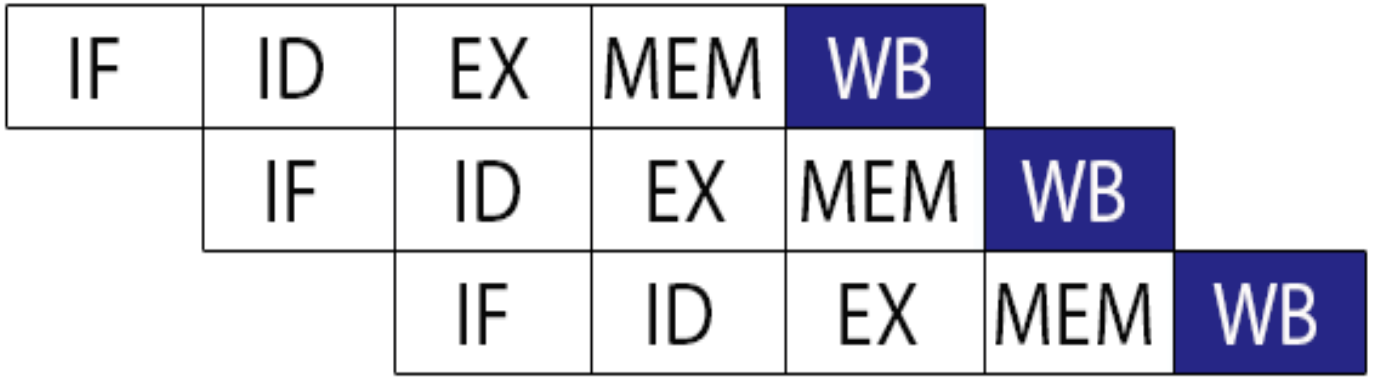
- **Pipelined Architecture:** increase the throughput

Pipelined Microprocessor



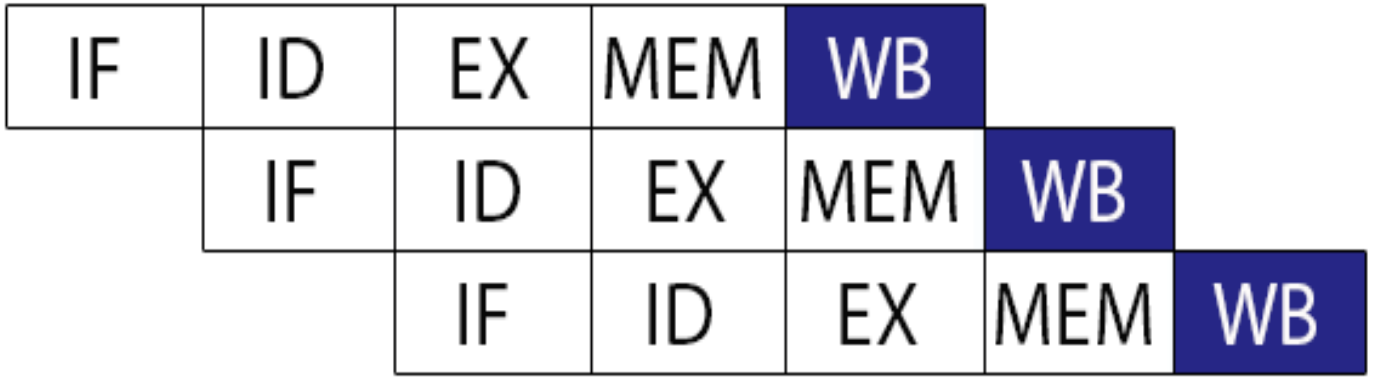
- Simulation refinement does not account for unobservable steps (stuttering)

Pipelined Microprocessor



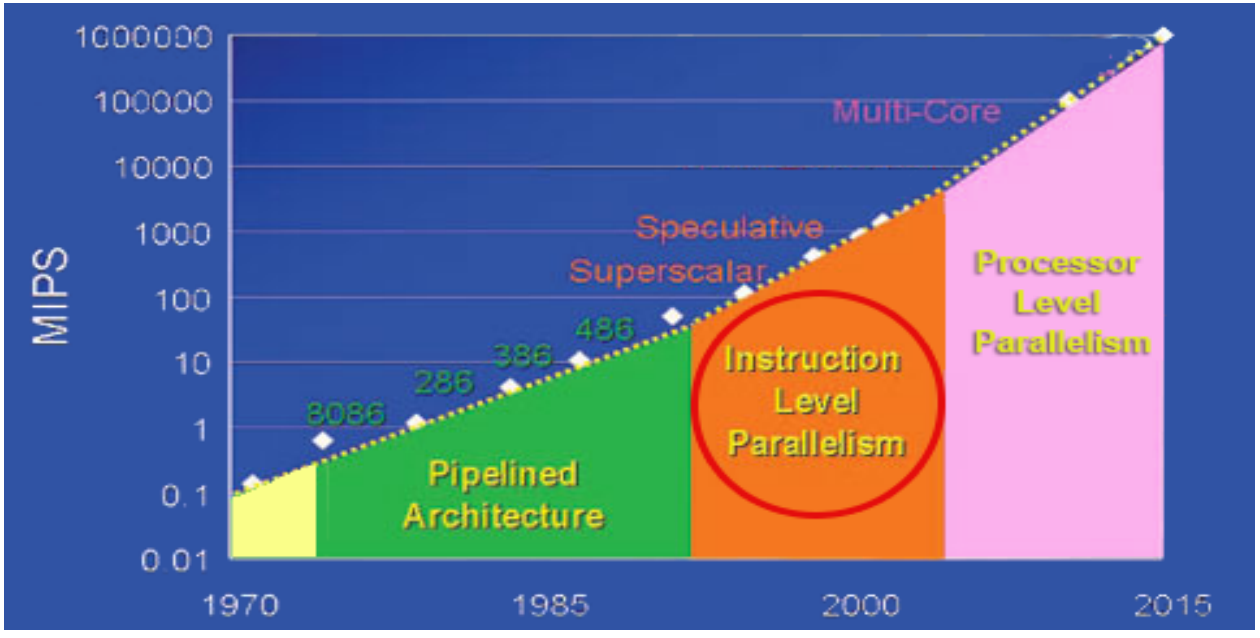
- Simulation refinement does not account for unobservable steps (stuttering)
- Show that all behaviors of the implementation are behaviors of the specification upto stuttering

Pipelined Microprocessor



- Simulation refinement does not account for unobservable steps (stuttering)
- Show that all behaviors of the implementation are behaviors of the specification upto stuttering
- Well-founded Stuttering Simulation [Manolios 2001]

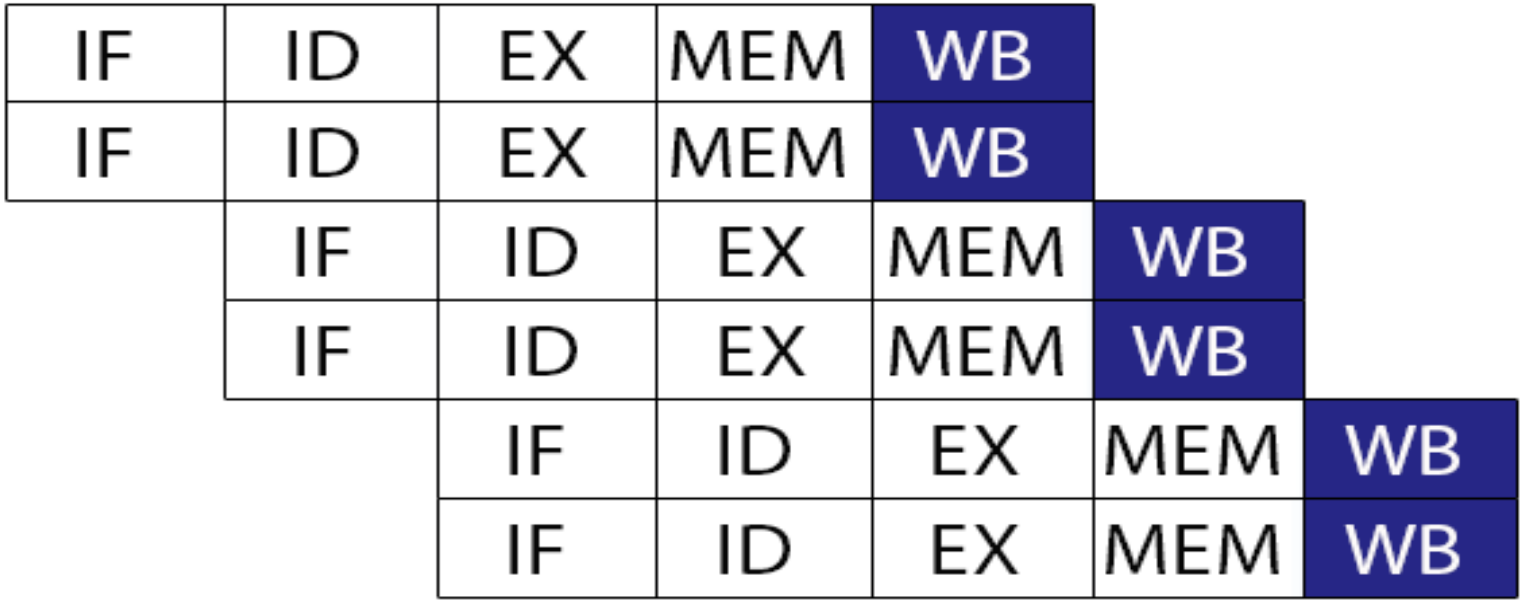
Superscalar Microprocessor



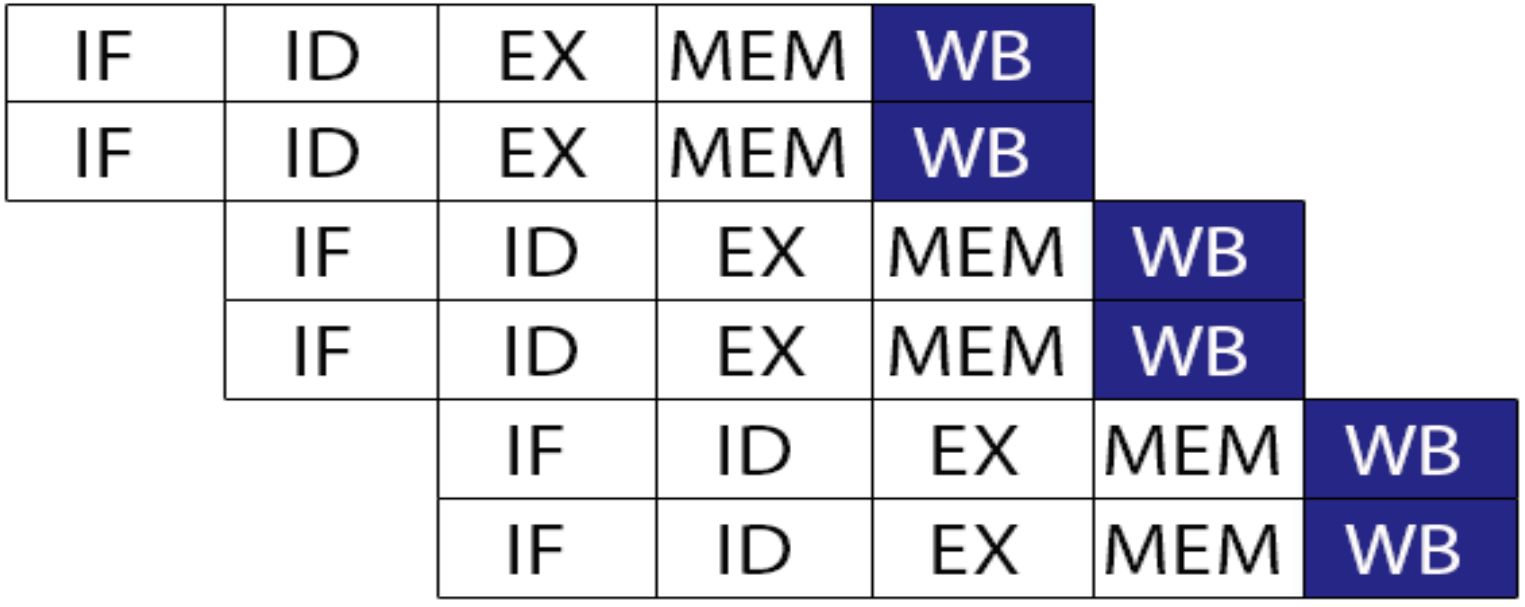
Optimizations

- Pipelined Architecture
- **Superscalar**: increase number of instructions retired per cycle

Superscalar Microprocessor

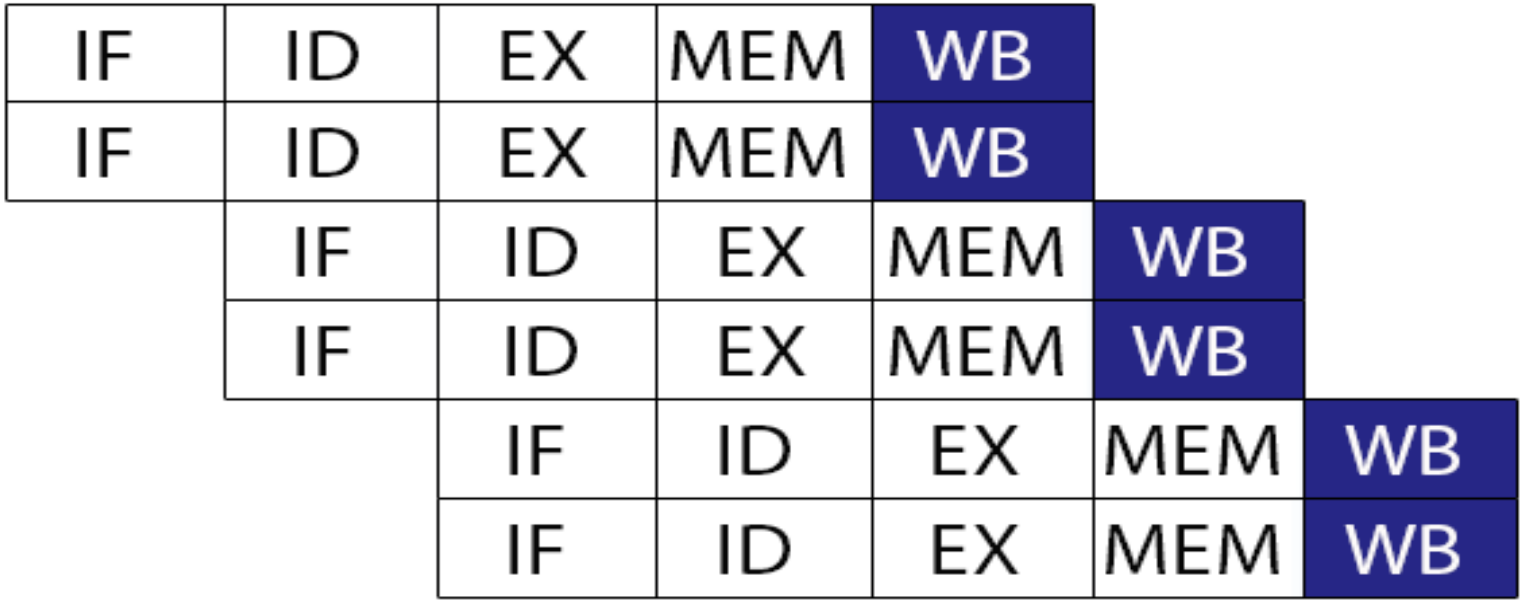


Superscalar Microprocessor



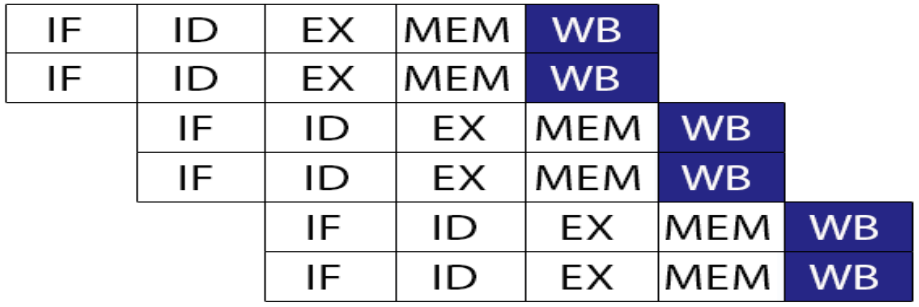
- Can retire multiple instructions in a single step.

Superscalar Microprocessor



- Can retire multiple instructions in a single step.
- Existing notions do not account for "skipping" observable steps.

Notion of Correctness for Superscalar Microprocessor



Skipping Refinement

- Show that all behaviors of the implementation are behaviors of the specification upto stuttering and finite skipping

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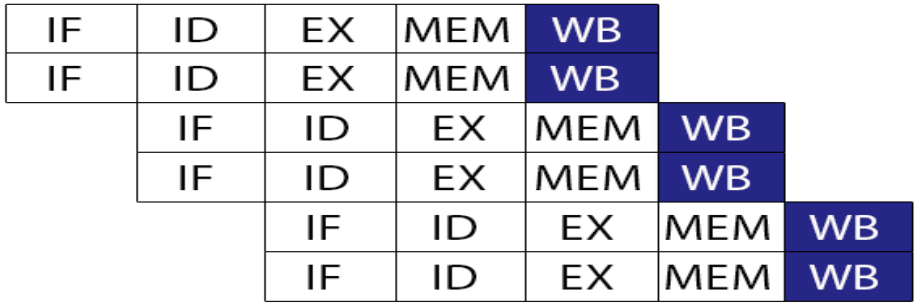

Skipping Refinement

- Show that all behaviors of the implementation are behaviors of the specification upto stuttering and finite skipping
- Well-founded Skipping

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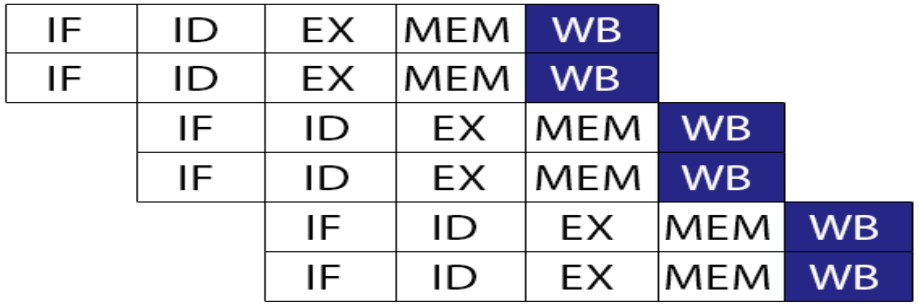
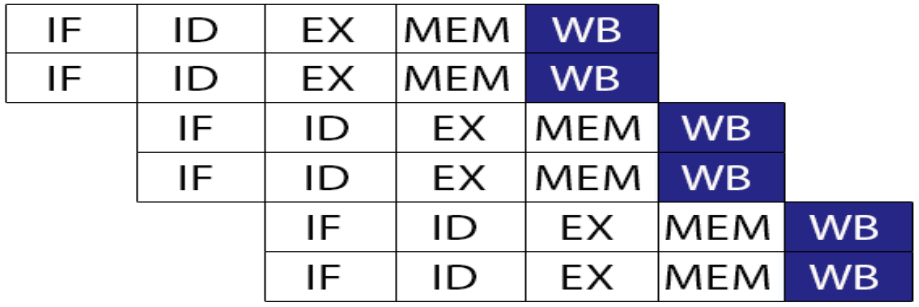


Skipping Refinement

- Show that all behaviors of the implementation are behaviors of the specification upto stuttering and finite skipping
- Well-founded Skipping
  - Local Reasoning

Notion of Correctness for Superscalar Microprocessor



Skipping Refinement

- Show that all behaviors of the implementation are behaviors of the specification upto stuttering and finite skipping
- Well-founded Skipping
  - Local Reasoning
  - Compositional

Case Studies

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- Vectorizing compiler transformation

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  - Transform a sequence of scalar instructions into vector instructions

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- Memory Controller

Case Studies

- Vectorizing compiler transformation
  - Transform a sequence of scalar instructions into vector instructions
- Memory Controller
  - Buffer reads/writes to the memory and update multiple locations in a page simultaneously.

Thank You