Challenging Problems in Industrial Formal Verification

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ABSTRACT OF TUTORIAL TALK

The electronic design industry has emerged in the recent years to adopt the system-on-chip (SoC) design methodology, where systems become a smart and complex integration of many configurable and reusable intellectual properties (IP) designs such as CPU, GPU, DSP, etc. SoC design methodologies have become common to a wide range of systems, starting from high-end servers, down to tablets, smartphones, Internet-of-things and wearable devices. The aggressive time-to-market and the hard competition add a major challenge to the electronic design companies to deliver high volume, and high quality products. Integration and validation of such designs has become the major challenge. The EDA industry and the academia has continued the innovation pipeline trying to cope with the complexity of such systems however major challenges are still ahead. Formal verification has emerged in the recent years to become a mainstream technology in SoC/IP design and verification methodologies. In the past, the usage of formal verification was limited to a small range of applications and it was mainly for verifying complex protocols, or some tricky logic functionality by formal experts. However in the recent years,we see a rapid adoption of formal, and we see a widespread of formal verification applications for low power design, security, SoC connectivity, configuration status register, and many more. In this talk, we provide an overview of the challenges that we see in designing SoC systems and configurable IPs, and provide some ideas to stimulate the academic research, aiming at increasing the research and innovation in such areas for keeping bridging the emerging gap that the electronic design industry is facing now and will face in the future.

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