Bayesian Networks based Probabilistic Approach for Digital Circuits' Reliability

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Abstract

Bayesian Networks technique is widely used in artificial intelligence and image processing. The application of applying Bayesian Networks in circuit design by leveraging its exact inference schemes in order to evaluate the reliability of digital circuit. The reliability of integrated circuits degrades as MOSFET dimensions continue to scale down to nanometer dimension. The measurement of reliability of nano-scale circuits is becoming an important issue for the circuit designers. The existing reliability computation schemes can only evaluate the cumulative reliability values of circuits. The cumulative or overall reliability value does not provide the enough information to the circuit designer to apply the fault tolerant solutions unless they are aware of the reliability degradation at circuit's internal stages and cell level. This research work shows how to transform the circuits into Bayesian networks and then to evaluate the reliability of each stage of the circuit. The simulations have been done on same functionality Full Adder circuits and different functionality circuits such as Decoder and a benchmark C17 circuit. The analysis on internal stages show that the larger number of gates' stages are giving lowest reliability compare to the rest of the stages.

Bayesian Networks Background Definitions

- Bayesian networks (BN) is a kind of graphical model whose basic constituents are nodes and set of directed links between multiple nodes make directed acyclic graph [1] .
- The directed acyclic links are used to show joint probabilities between the nodes. Every Bayesian network node has a conditional probability table except their parent nodes and each parent node has an earlier probability
- We compute the error probability by assuming that our original network is error-free and making a copy of it to represent an error prone network. Error at the ith output can be represented mathematically in (1) and (2).

$$E_i = Y_i^e \otimes Y_i \quad (1)$$

$$P(E_i = 1) = P(Y_i^e \otimes Y_i = 1) \quad (2)$$

- where; Y_i and Y_i^e are the outputs of the ideal and error prone circuits respectively. The probability of the ith output can be calculated if both error free output Y_i and error prone Y_i^e are equal to logic 1. The XOR gate is used as a comparator to compare both the original and error prone network which gives the correct output error probability.

Bayesian Networks in Circuit Design

- Bayesian networks scheme can be used in circuit design by transforming circuit individual gates into nodes and finally compute the reliability of circuit by using BN algorithms.

- We consider a Full Adder (XOR/NAND) circuit as a case study and following are the steps in terms of diagrams showing all graphical transformations.

Methodology

Test Circuit (e.g. Full Adder) → BN Transformations in Nodes → BN Moral Graph Transformation → BN Triangulated Graph Transformation → Junction Tree Graph Transformation → Initialization and Message Passing → Marginalization (Marginal Probability) → Compute Reliability of Entire Circuit → Compute Reliability of sub-circuit → Compute Reliability of each Gate

Soft Errors Effects → Reliability of Nano-scale Circuits → Techniques of Estimation Reliability → Digital-Logic Level: Bayesian Networks (BN), Probabilistic Transfer Matrix (PTM), Probabilistic Gate Model (PGM), Booelan Difference Error Calculator

Overall Circuit Reliability

This Work → Sub-Circuit or stage wise Reliability of Circuits

Future Work → Gate-wise i.e. individual Gate's Reliability

Fig. Full Adder (XOR/NAND) Circuit

Fig. Full Adder (XOR/NAND) Circuit Divided into sub-circuit

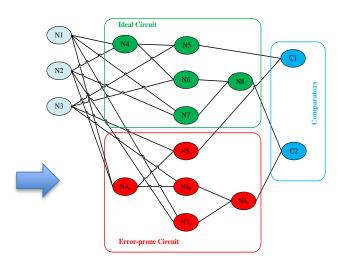## Graphical Transformations and Methodology
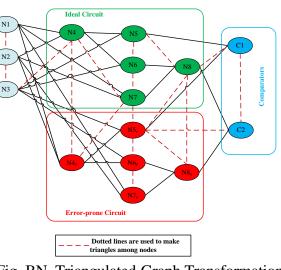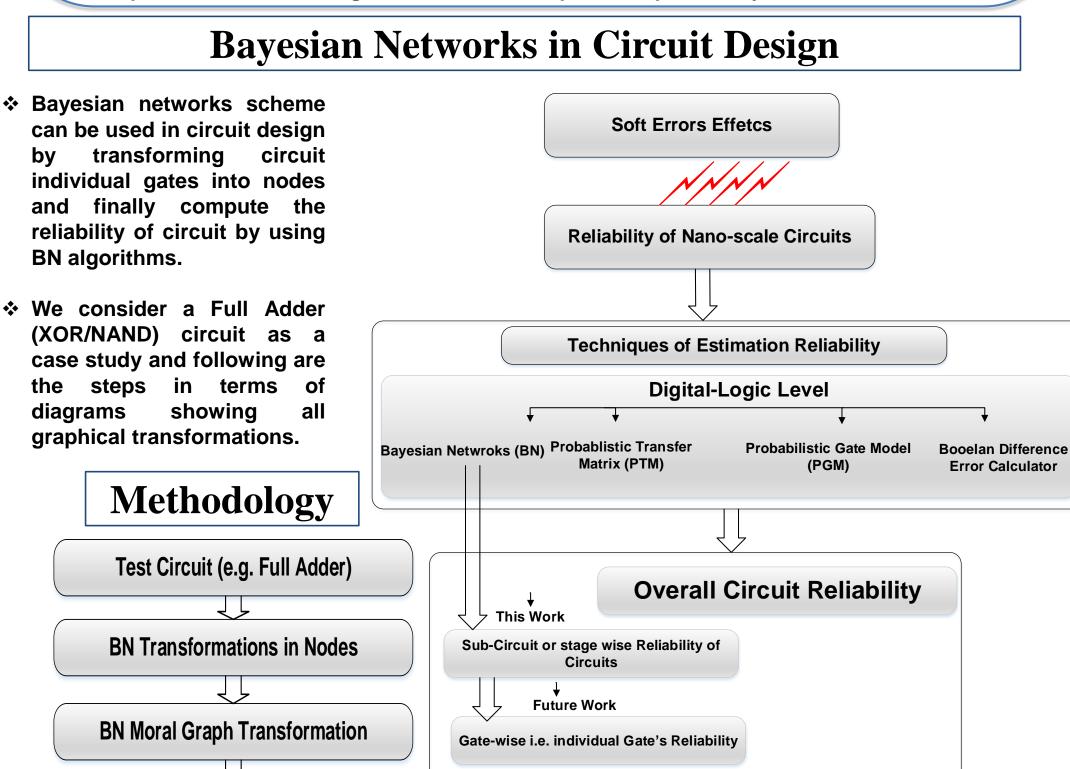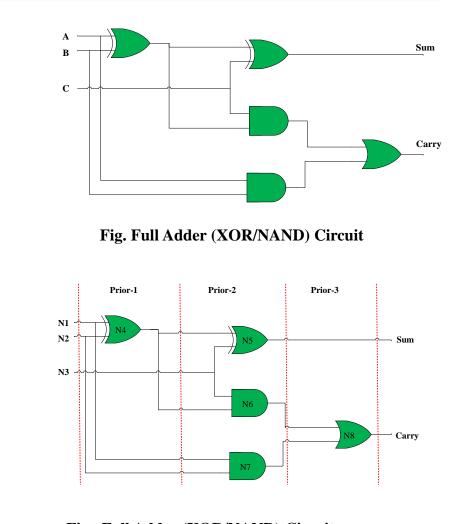

Fig. BN Conceptual Diagram

Fig. BN Gates to Nodes Transformation

Fig. BN Moral Graph Transformation

Fig. BN Triangulated Graph Transformation

Fig. Junction Tree Transformation

Conditional Probability Tables

Table I Digital Signal Values for Full Adder (XOR /NAND) Circuit

Input Name	Input values
N1	0 or 1
N2	0 or 1
N3	0 or 1
N4 (N1=0,N2=0)	0
N4 (N1=0,N2=1)	1
N4 (N1=1,N2=0)	1
N4 (N1=1,N2=1)	0

Table II CPT for Ideal Full Adder (XOR /NAND) Circuit

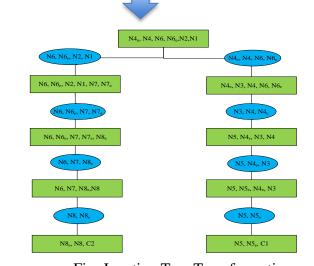| Input Name	Probability of Input being 0	Probability of Input being 1
N1	P(N1=0) = 0.5	P(N1=1) = 0.5
N2	P(N2=0) = 0.5	P(N2=1) = 0.5
N3	P(N3=0) = 0.5	P(N3=1) = 0.5
N4	P(N4=0|N1,N2)	P(N4=1|N1,N2)
N4 (N1=0,N2=0)	0	1
N4 (N1=0,N2=1)	1	0
N4 (N1=1,N2=0)	1	0
N4 (N1=1,N2=1)	0	1

Table III CPT for Error-prone Full Adder (XOR /NAND) Circuit

Input Name	Probability of Input being 0	Probability of Input being 1
N1	P(N1=0) = 0.5	P(N1=1) = 0.5
N2	P(N2=0) = 0.5	P(N2=1) = 0.5
N3	P(N3=0) = 0.5	P(N3=1) = 0.5
N4	P(N4$_e$=0|N1,N2)	P(N4$_e$=1|N1,N2)
N4$_e$ (N1=0,N2=0)	ε_g	1- ε_g
N4$_e$ (N1=0,N2=1)	1- ε_g	ε_g
N4$_e$ (N1=1,N2=0)	1- ε_g	ε_g
N4$_e$ (N1=1,N2=1)	ε_g	1- ε_g

Results

Table Reliability of Each Stage for Same Functionality Digital Circuits

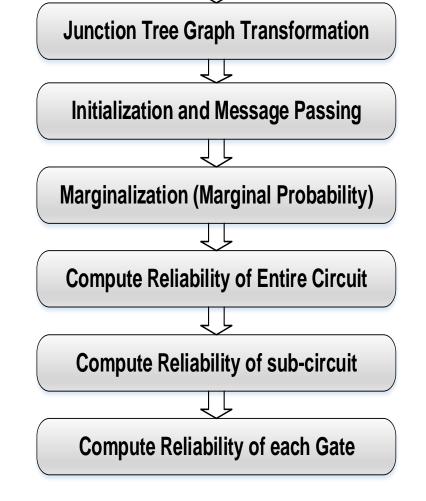| Circuit Name	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7
Full Adder (XOR/NAND)	0.8693	0.8687	0.8723	-	-	-	-
Full Adder (NAND)	0.7576	0.7813	0.7634	0.7651	0.7746	0.7702	0.7656
Full Adder (Majority)	0.8071	0.7305	0.8178	-	-	-	-

Table Reliability of Each Stage for Different Functionality Digital Circuits

Circuit Name	Stage-1	Stage-2	Stage-3
2-4 Decoder	0.9500	0.9392	-
C17	0.8627	0.8575	0.8445

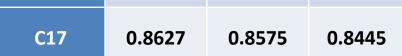- The result show that the circuits having similar Boolean functionality does not have similar location of lowest reliability stage. It depends on the number of gates in the respective stage.
- The second category different functionality circuit results lead us to the same dependency as well. But the lower reliability is also dependent on the circuit structure which has been analyzed in different functionality circuits where the error-effect is propagating from primary inputs to the internal circuitry gates and affecting the reliability of final stage.
- So overall, the affected stages (having lower reliability values) are dependent on the larger number of gates in the respective stage.

Conclusion

- The graphical transformation in stage analysis using Bayesian networks gives the circuit designer an opportunity to take an in depth analysis of internal architecture of the circuit.
- The Bayesian network not only evaluates the overall reliability of a circuit but also evaluates its reliability with respect to stage location.
- This analysis shows that the affected stages are dependent on the number of gates in the respective stage and the circuit structure.
- The identification of most error-prone stage is helpful for the circuit designer who can possibly introduce fault-tolerance solutions to stages having reliability below a certain threshold. The stage analysis helps the circuit designer to take extra measures to ensure the reliability of stages having reliability below a certain threshold.

Future Work

- In future work BN will be applied in order to compute the Reliability for a Gate-wise Reliability evaluation.
- The work is already in progress for Transistor level CMOS and FinFETs based circuits Reliability Evaluation.

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