Dynamic Random Access Memory:

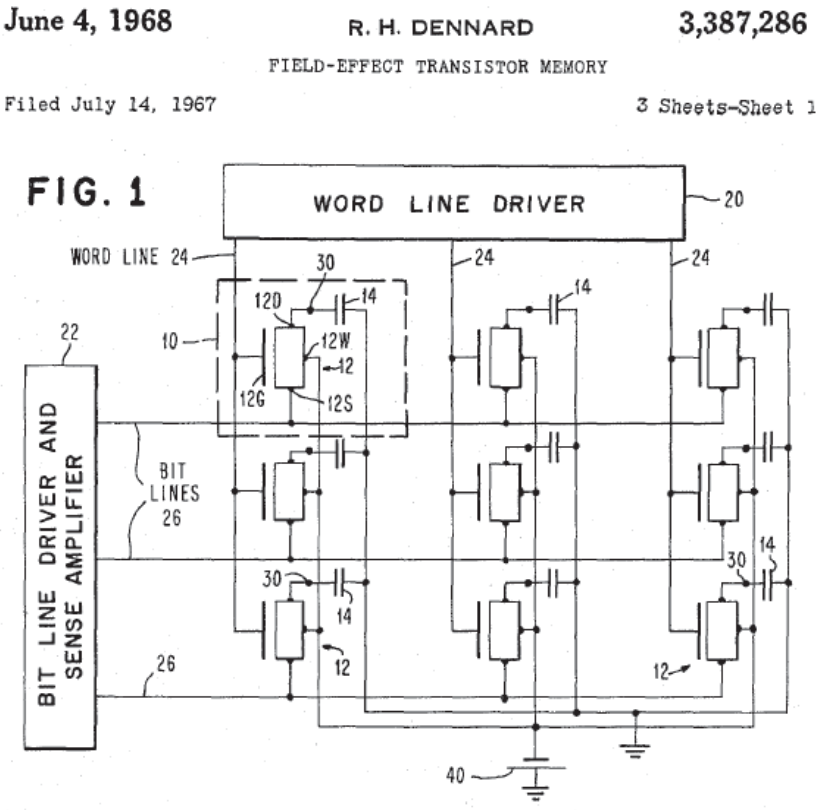
Dynamic random access memory (DRAM) is a type of random access memory that stores each bit of data in a separate capacitor within an integrated circuit. Since real capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory.

The main memory (the "RAM") in personal computers is Dynamic RAM (DRAM), as is the "RAM" of home game consoles (PlayStation, Xbox 360 and Wii), laptop, notebook and workstation computers.

The advantage of DRAM is its structural simplicity: only one transistor and a capacitor are required per bit, compared to six transistors in SRAM. This allows DRAM to reach very high density. Unlike flash memory, it is volatile memory (cf. non-volatile memory), since it loses its data when power is removed. The transistors and capacitors used are extremely small—millions can fit on a single memory chip.

From http://en.wikipedia.org/wiki/DRAM

The modern DRAM patent:


June 4, 1968 R. H. DENNARD 3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

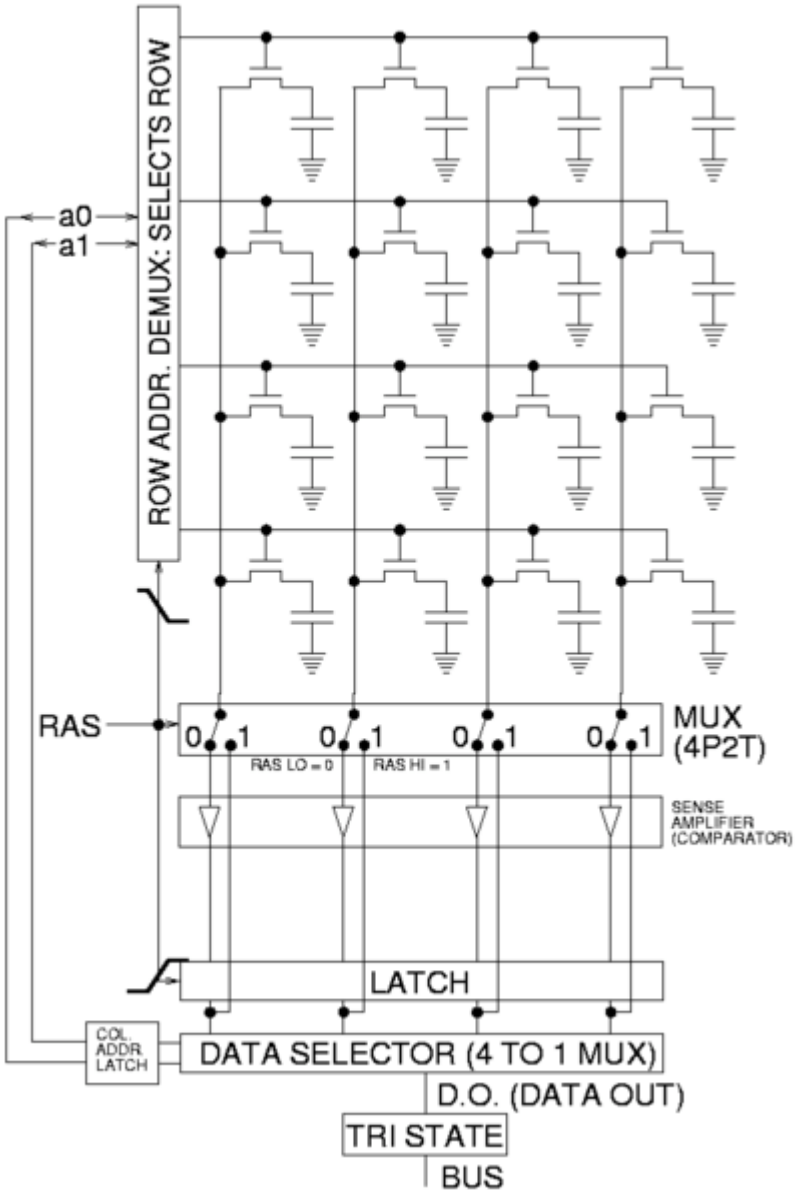
Filed July 14, 1967 3 Sheets-Sheet 1

FIG. 1

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

DRAM Internal Storage Architecture

An alternate drawing from Wikipedia uses row and column numernclature instead of word and bit lines.



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The Row Address Strobe (RAS) connects a row of capacitive memory cells to the column lines. To read, a sense amplifier is used. To write, the column lines are driven high or low.

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

When an external Column Address Strobe (CAS) follows the RAS, the sense amplifier value is captured. Then, when the CAS remains low, the output of the sense amp is fed back to the columns to "refresh" the row being read.

Therefore, RAS followd by CAS or RAS before CAS leads to a read function (or write if desired).

If no access is performed, an external refresh cycle musted be initiated. The normal way of doing a refresh is to present CAS before RAS, a sequence not associated with a normal read or write cycle.

DRAM Flavors

DRAM

Fast Page Mode DRAM

Extended Data Output DRAM

Burst EDO DRAM

Multibank DRAM

Synchronous DRAM (SDRAM)

Pseudo Statc DRAM (PSDRAM)

Double Data Rate (DDR)

Comments

Historically, DRAMs can come and go in as little as 6 months … first released to obsolete.

DRAMs often have "extra bits" for parity error detection or full error detection and correction.

DRAM data storage can be effected by temperature and electro magnetic effects.

Dr. Grantmer's DRAM Notes P. 137-159.

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

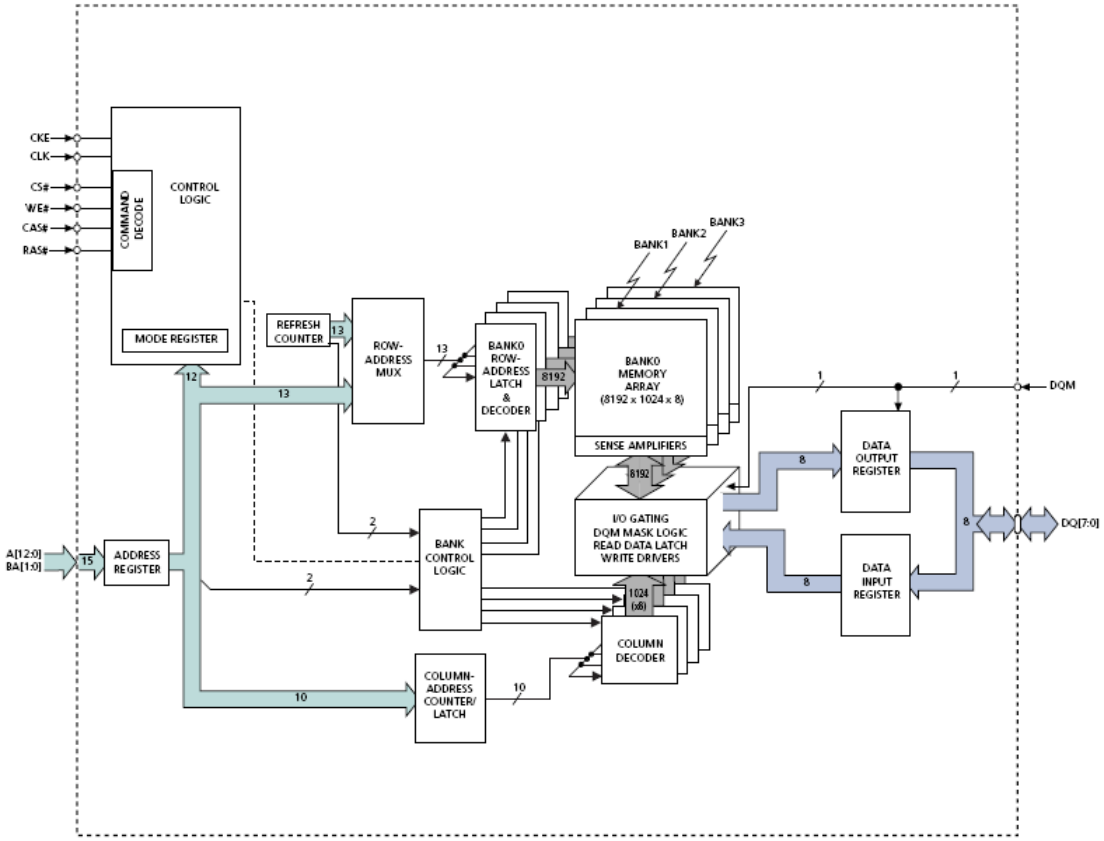
Micron MT48LC32M8A2TG-6A: 8 Meg x 8 x 4 banks, 256 Mbit

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode (not available on AT devices)
- Auto refresh
  - 64ms, 8192-cycle (commercial and industrial)
  - 16ms, 8192-cycle (automotive)
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

Block Diagram

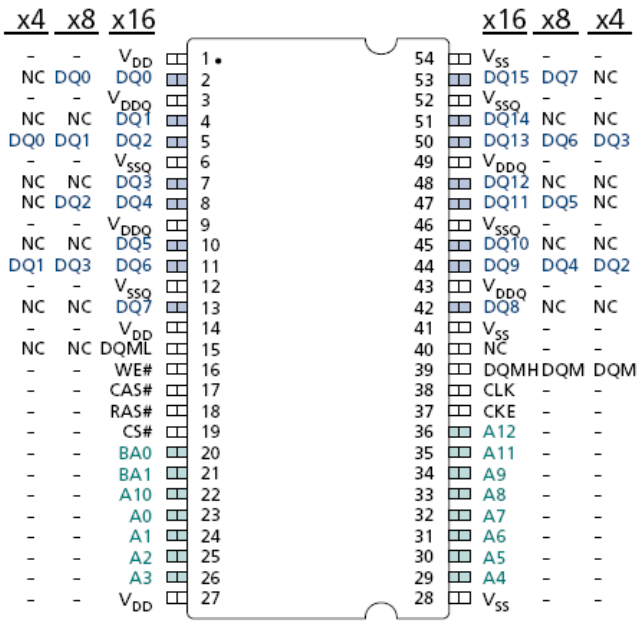
Figure 2: 32 Meg x 8 Functional Block Diagram



Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

Pinout

Figure 4: 54-Pin TSOP (Top View)



Note: 1. The # symbol indicates that the signal is active LOW. A dash (-) indicates that the x8 and x4 pin function is the same as the x16 pin function.

Functional Description

In general, 256Mb SDRAM devices (16 Meg x 4 x 4 banks, 8 Meg x 8 x 4 banks, and 4 Meg x 16 x 4 banks) are quad-bank DRAM that operate at 3.3V and include a synchronous interface. All signals are registered on the positive edge of the clock signal, CLK. Each of the x4's 67,108,864-bit banks is organized as 8192 rows by 2048 columns by 4 bits. ***Each of the x8's 67,108,864-bit banks is organized as 8192 rows by 1024 columns by 8 bits***. Each of the x16's 67,108,864-bit banks is organized as 8192 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A[12:0] select the row). The address bits (x4: A[9:0], A11; x8: A[9:0]; x16: A[8:0]) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

Pin Descriptions

Table 4: Pin and Ball Descriptions

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while CS# is HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
x4, x8: DQM x16: DQML, DQMH LDQM, UDQM (54-ball)	Input	Input/output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are High-Z (two-clock latency) during a READ cycle. LDQM corresponds to DQ[7:0], and UDQM corresponds to DQ[15:8]. LDQM and UDQM are considered same-state when referenced as DQM.
BA[1:0]	Input	Bank address input(s): BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A[12:0]	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0] and A11 for x4; A[9:0] for x8; A[8:0] for x16; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA[1:0] (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
x16: DQ[15:0]	I/O	Data input/output: Data bus for x16 (pins 4, 7, 10, 13, 42, 45, 48, and 51 are NC for x8; and pins 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, and 53 are NC for x4).
x8: DQ[7:0]	I/O	Data input/output: Data bus for x8 (pins 2, 8, 47, 53 are NC for x4).
x4: DQ[3:0]	I/O	Data input/output: Data bus for x4.
V_{DDQ}	Supply	DQ power: DQ power to the die for improved noise immunity.
V_{SSQ}	Supply	DQ ground: DQ power to the die for improved noise immunity.
V_{DD}	Supply	Power supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground.
NC	–	These should be left unconnected. For x4 and x8 parts, G1 is a no connect, but may be used as A12 in future designs.

Addressing

Each of the x8's 67,108,864-bit banks is organized as
8192 rows by 1024 columns by 8 bits.

- Initial A[12:0] (RAS period) addresses one of the 8192 rows
- Initial BA[1:0] (RAS period) addresses one of the four banks
- Later A[9:0] (CAS period) addresses one of the 1024 columns

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

Device Commands

Table 16: Truth Table – Commands and DQM Operation

Note 1 applies to all parameters and conditions

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	8
Write enable/output enable	X	X	X	X	L	X	Active	9
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	9

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A[0:*n*] provide row address (where A*n* is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:*i*] provide column address (where *i* = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQ column reads a "Don't Care" state to illustrate that the BURST TERMINATE command can occur when there is no data present.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. A[11:0] define the op-code written to the mode register.
9. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

Initialization

SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

See data sheet page 43-45.

Mode Register

The mode register defines the specific mode of operation, including burst length (BL), burst type, CAS latency (CL), operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and retains the stored information until it is programmed again or the device loses power.

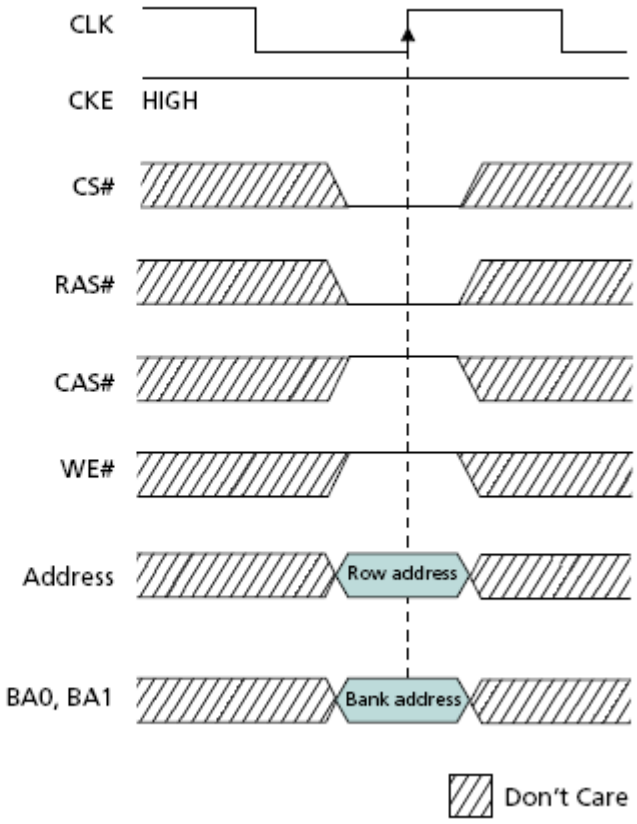
Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

Simple Execution

ACTIVE

The ACTIVE command is used to activate a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

Figure 13: ACTIVE Command

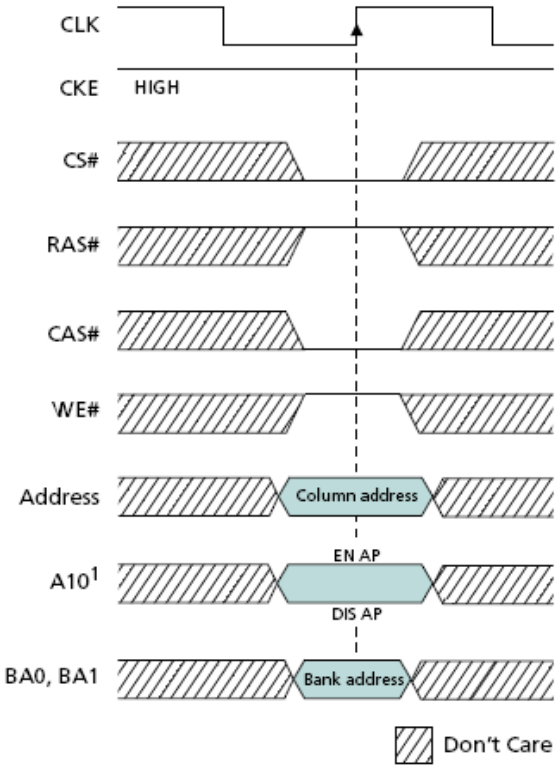


Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

READ

The READ command is used to initiate a burst read access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the READ burst; if auto precharge is not selected, the row remains open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

Figure 14: READ Command



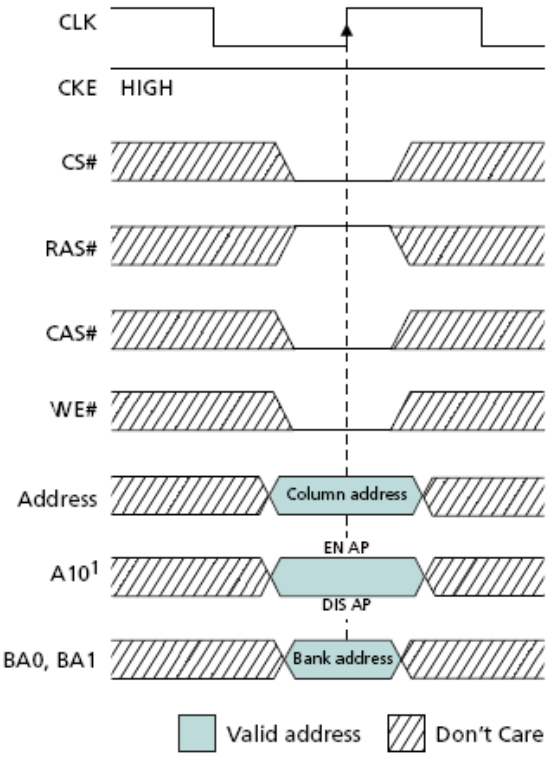
Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the write burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQ is written to the memory array, subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data is written to memory; if the DQM signal is registered HIGH, the corresponding data inputs are ignored and a WRITE is not executed to that byte/column location.

Figure 15: WRITE Command



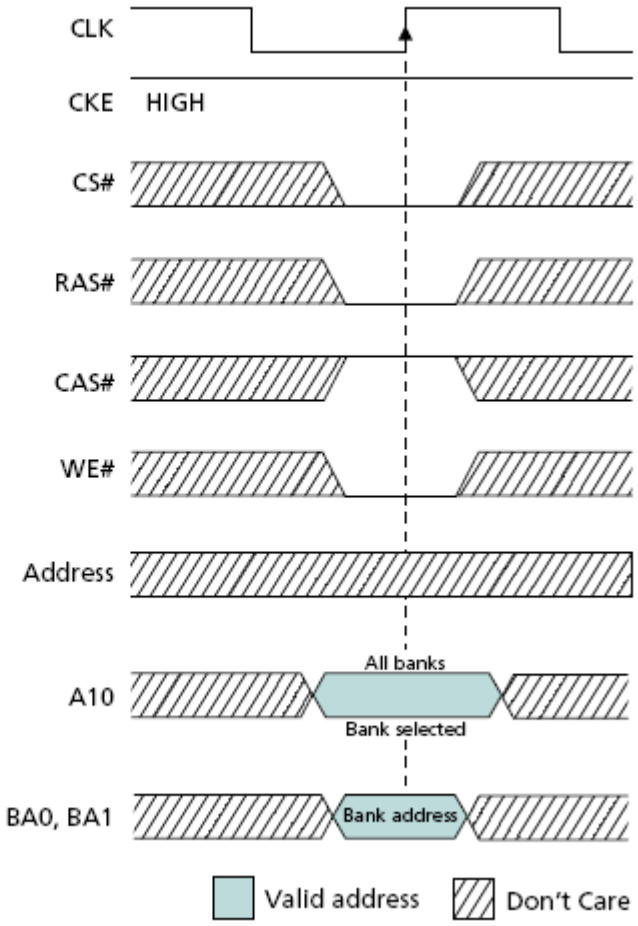
Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is precharged, inputs BA0 and BA1 select the bank. Otherwise BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands are issued to that bank.

Figure 16: PRECHARGE Command



Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

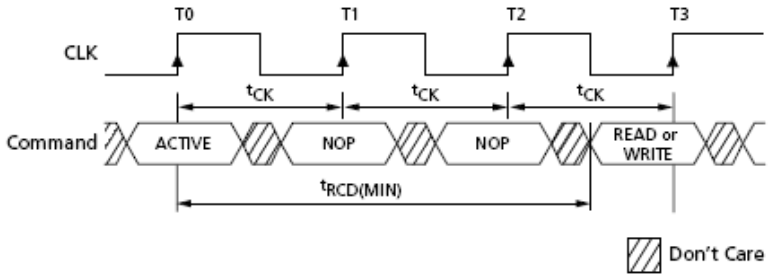
AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be precharged prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum t_{RP} has been met after the PRECHARGE command, as shown in Bank/Row Activation (page 51 of the data sheet). The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command.

Regardless of device width, the 256Mb SDRAM requires 8192 AUTO REFRESH cycles every 64ms (commercial and industrial) or 16ms (automotive). Providing a distributed AUTO REFRESH command every 7.813µs (commercial and industrial) or 1.953µs (automotive) will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (t_{RFC}), once every 64ms (commercial and industrial) or 16ms (automotive).

Activation Timing

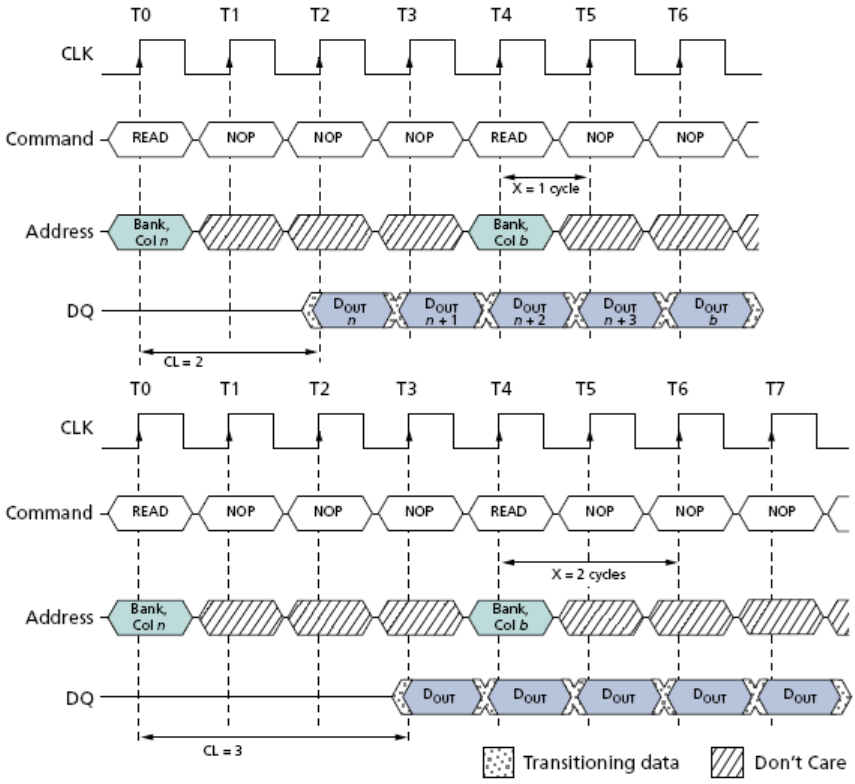
Figure 20: Example: Meeting ^{t}RCD (MIN) When 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3



Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

Read Timing

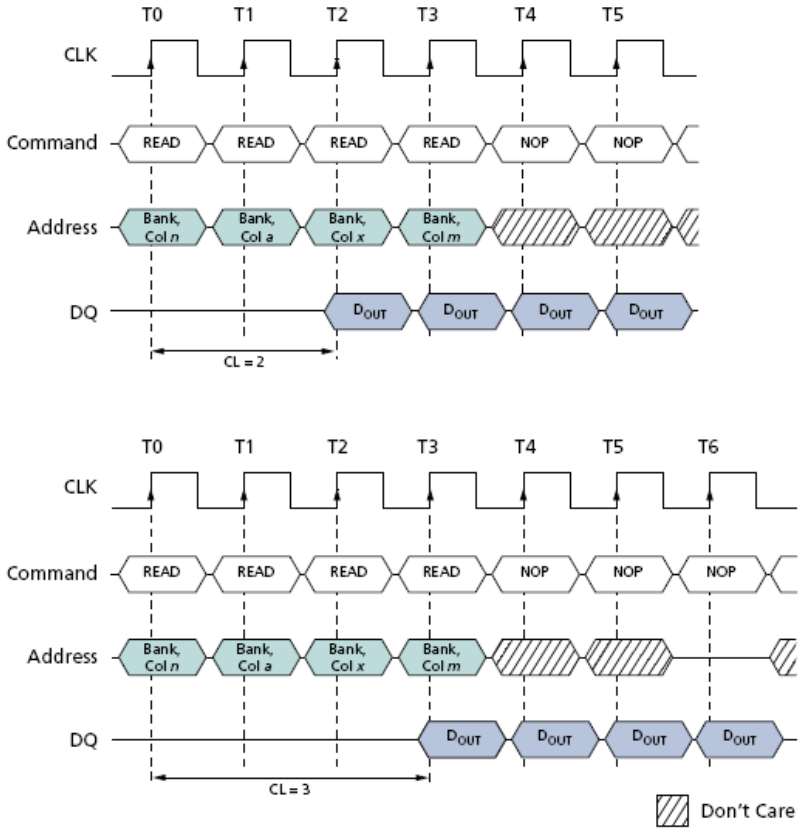
Figure 21: Consecutive READ Bursts



Note: 1. Each READ command can be issued to any bank. DQM is LOW.

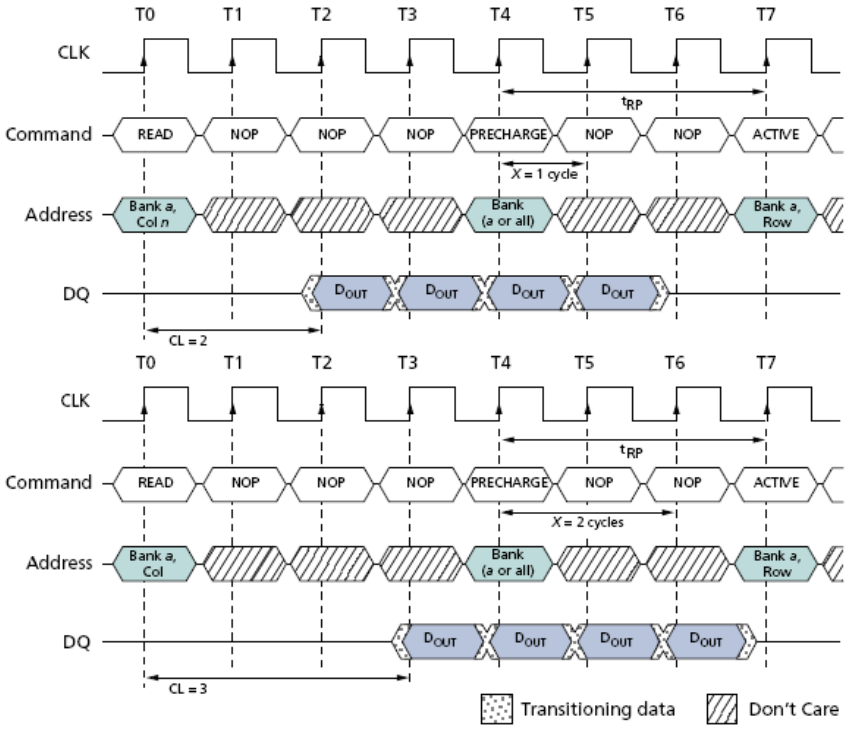
Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

Figure 22: Random READ Accesses



Note: 1. Each READ command can be issued to any bank. DQM is LOW.

Figure 25: READ-to-PRECHARGE

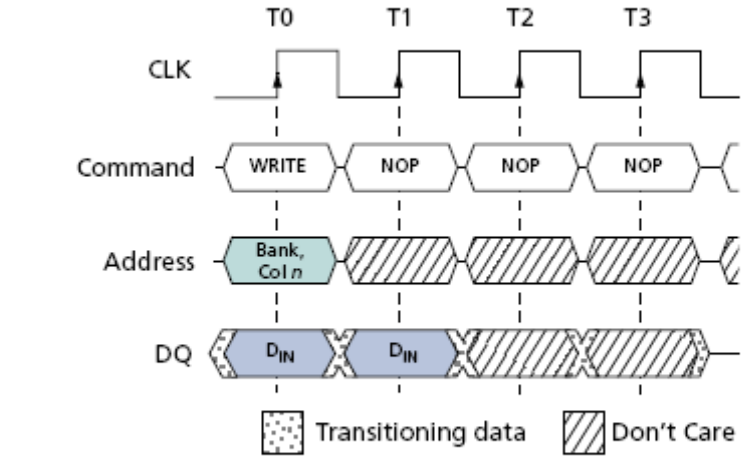


Note: 1. DQM is LOW.

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

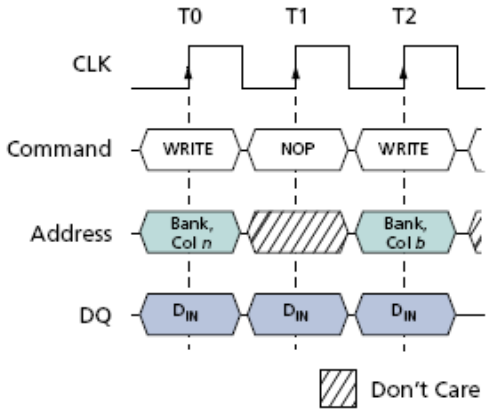
Write Timing

Figure 30: WRITE Burst



Note: 1. BL = 2. DQM is LOW.

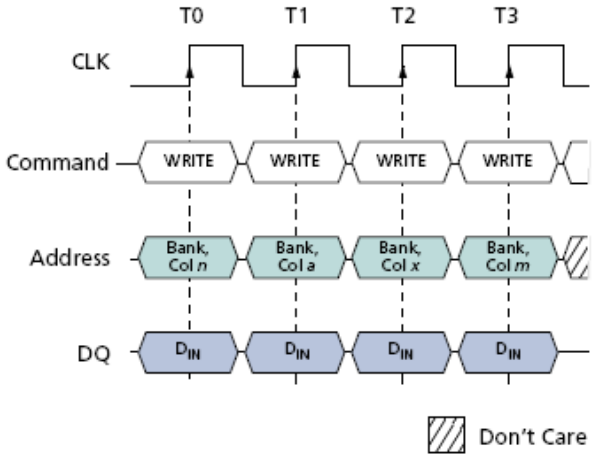
Figure 31: WRITE-to-WRITE



Note: 1. DQM is LOW. Each WRITE command may be issued to any bank.

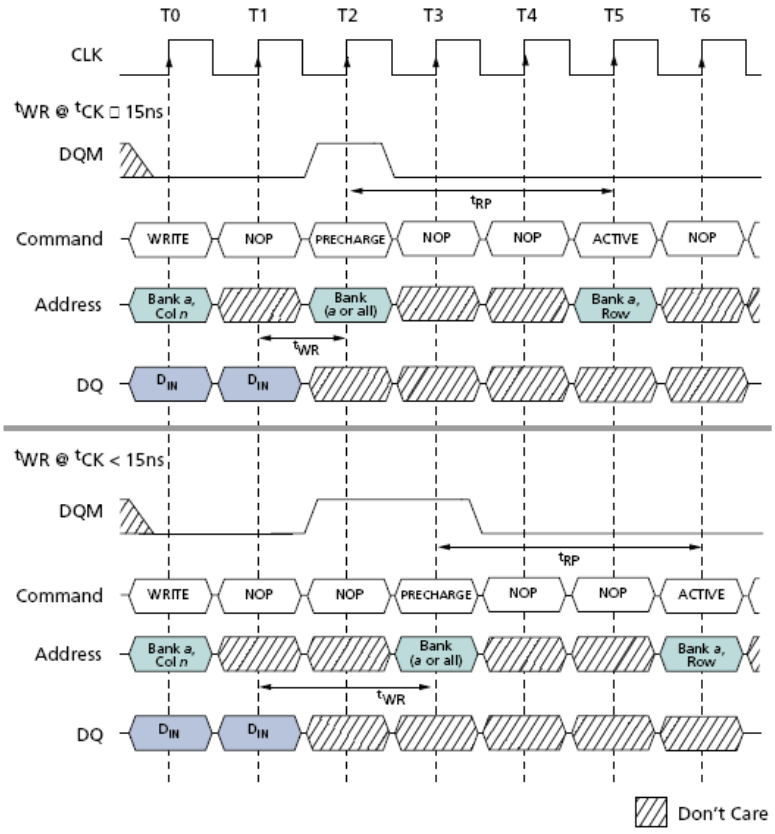
Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.

Figure 32: Random WRITE Cycles



Note: 1. Each WRITE command can be issued to any bank. DQM is LOW.

Figure 34: WRITE-to-PRECHARGE



Note: 1. In this example DQM could remain LOW if the WRITE burst is a fixed length of two.

Material derived from http://en.wikipedia.org/wiki/DRAM and Micron Technology, Inc. Data Sheet for the MT48LC32M8A2 – 8 Meg x 8 x 4 banks, PDF: 09005aef8091e6d1, 256Mb_sdr.pdf - Rev. N 1/10 EN, 1999.