Lecture 19: Exam 2 Review

- Administration
  - Homework 7 due today
  - Exam II in class Tuesday April
- Last time
  - Page table organization
  - Page table may not be in memory!?
  - TLB to speed up VM address translation
- Today
  - Exam Review

Format

- Open book and open notes
  - including homework, notes, printed lectures, etc.
  - Helpful table: http://www.vaughns-1-pagers.com/computer/powers-of-2.htm
- Calculator (No other electronic devices)
- 75 minutes
- 4 Sections
  - Section 1: multiple choice, true/false, short answer
    - Topics will range over all the material
  - Section 2 through 4: multiple parts on a single topic
    - Topics: Pipelining, Caches, Virtual Memory

Things you should know

- Pipelining
  - Instruction fetch logic, decode logic, hazards, hazard detection, hazard solutions
  - Multi-issue pipelining
  - Basics of out-of-order execution
  - Performance analysis of pipelining IPC, CPI
- Cache & Memory Hierarchy Design
  - AMAT, program properties it exploits, miss rate, miss types
  - cache design tradeoffs (size, ports, associativity, etc.)
  - address translation, mapping/replacement
- Virtual Memory Design
  - Paging, pages, page frames
  - address translation, mapping/replacement
  - Page table logic, TLB hardware to speed up paging

Things you should be able to do

- Analyze a pipeline
- Modify or design a pipeline
- Analyze and design hazard logic
- Compute AMAT
- Analyze cache and virtual memory behavior given a design and for a particular address stream
- Design address translation hardware for particular cache and virtual memory configurations

Questions & Answer