An ACL2 Mechanization of an Axiomatic Weak Memory Model

Ben Selfridge

February 28, 2014

Outline

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Multiprocessor Reasoning

Goal: **Analysis of programs** written for **multiple processors** with a shared memory

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Both approaches have certain advantages and disadvantages

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- **Axiomatic** models can be **easier to reason about**; fully modeling an MP architecture can be messy from a theorem-proving perspective

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2. Demonstrate, for all programs and oracles, **any object** produced by such an execution **satisfies certain structural properties**
3. To prove a program has property P, show that **any execution** of that program that **fails to satisfy** P will produce an **invalid object**

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- Instead, they satisfy some weaker properties
- **Axiomatic Memory Models** attempt to capture the weaker consistency guarantees of most modern architectures as axioms

Goal of this talk

What this talk is about:

[1] [2] Jade Alglave, Luc Maranget, and Michael Tautschnig. *Herding Cats - Modelling, simulation, testing, and data-mining for weak memory.* To appear in TOPLAS 2014. http://arxiv.org/abs/1308.6810

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- A partial description of one particular axiomatic memory framework[1]

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- A partial description of one particular axiomatic memory framework[1]
- An ACL2 mechanization of this framework
- A new proof of a nice equivalence result for this framework, and a mechanization of this proof

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How does this translate to concurrent programs?

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Instead, we represent it as a graph, consisting of a collection of **events** with various kinds of directed edges.

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Definition

An *event* is a read or a write.

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Components of an event:

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- Memory location
- Value read or written
- Process number

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An *execution* is a tuple $(\mathbb{E}, \mathsf{po}, \mathsf{rf}, \mathsf{co})$, where $\mathbb{E}$ is a set of events and po, rf, and co are relations on $\mathbb{E}$ satisfying

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po is "program order", co is "coherence order", rf is "read-from"

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co, rf, and fr are *per-location* dependencies; they relate events which occur at the same memory location only

Sequential consistency (SC)

Sequential consistency[2]: "The result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program."

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In our framework, we interpret this as the condition

$$\mathsf{acyclic}(\mathsf{po} \cup \mathsf{co} \cup \mathsf{rf} \cup \mathsf{fr})$$

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Modern architectures do not satisfy this constraint.

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SC-Per-Location

Although we don't usually have full sequential consistency, we do have an analogous notion that is enforced by most modern architectures:

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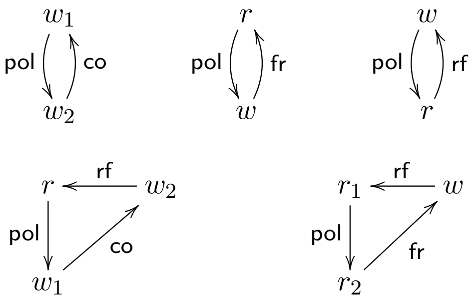
where pol is po restricted to events at the same memory location.

We refer to this condition as *SC-Per-Location*.

SC-Per-Location

SC-Per-Location is equivalent to prohibiting the following five patterns:



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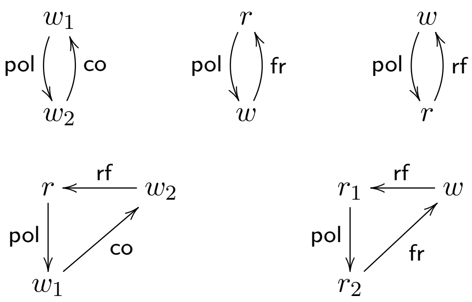

We formalized SC-Per-Location in ACL2 and proved this equivalence.

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- This included a new proof of an equivalence theorem
- I plan to investigate how this model (or a similar one) can be used practically for MP code proofs

References

1. Jade Alglave. *A Shared Memory Poetics.* Ph.D. Dissertation. Université Paris 7, 2010.

2. Jade Alglave, Luc Maranget, and Michael Tautschnig. *Herding Cats - Modelling, simulation, testing, and data-mining for weak memory.* To appear in TOPLAS 2014. http://arxiv.org/abs/1308.6810

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