

# Modeling Asynchronous Circuits in ACL2 Using the Link-Joint Interface

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# Introduction

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Why asynchronous?

- Low power consumption.
- High operating speed.
- Better composability and modularity.
- ...

# Introduction

Formal verification in asynchronous systems is an active research area.

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# Approach

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Dealing with:

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⇒ Every [state-holding device](#) in the DE primitive database must be governed by its own clock signal.
- local handshake protocols,  
⇒ Modeling the [link-joint interface](#) introduced by Roncken et al. [M. Roncken et al., 2015] in DE.



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Each occurrence consists of four elements: a module-unique occurrence name, outputs, a reference to a primitive or defined module, and inputs.

# DE Language Example

```
(defconst *half-adder*  
  '(half-adder      ;; module name  
    (a b)           ;; module inputs  
    (sum carry)    ;; module outputs  
    ()              ;; internal states  
    ;; occurrences  
    ((g0           ;; occurrence name  
      (sum)        ;; occurrence outputs  
      f-xor        ;; a primitive reference  
      (a b))       ;; occurrence inputs  
      (g1 (carry) f-and (a b))))))
```

# DE Language Example

```
(defconst *full-adder*
  (cons
    '(full-adder
      (a b c)
      (sum carry)
      ())
      ((t0 (sum1 carry1) half-adder      (a b))
       (t1 (sum  carry2) half-adder      (sum1 c))
       (t2 (carry)      f-or      (carry1 carry2))))
  *half-adder*))
```



# DE Language Example

```
(defconst *one-bit-counter*  
  (cons  
    '(one-bit-counter  
      (clk carry-in reset-)  
      (out carry)  
      (g0)  
      ((g0 (out)          ff          (clk sum-reset-))  
        (g1 (sum carry) half-adder  (carry-in out))  
        (g2 (sum-reset-) f-and      (sum reset-))))  
    *half-adder*))
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Demo.

# An Example DE Proof

Prove the correctness of a parameterized ripple-carry adder.

```
(defun ripple-adder (c a b)
  (declare (xargs :guard (and (booleanp c)
                               (boolean-listp a)
                               (boolean-listp b))))
  ;; c is a bit, a and b are bit-vectors of some length n;
  ;; this function returns a bit vector of length n+1.
  (if (endp a)
      (list c)
      (cons (xor c (xor (car a) (car b)))
            (ripple-adder (or (and (car a) (car b))
                              (and (car a) c)
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                          (cdr a)
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# Link and Joint

The dataflow in self-timed systems can be viewed as a directed graph with **links as edges** and **joints as nodes** [M. Roncken et al., 2015], where:

- Links are **communication channels**, with data flowing in the direction of the edges representing the links.
- Joints are modules that implement **flow control** and **data operations**.

The dataflow in self-timed systems can be viewed as a directed graph with **links as edges** and **joints as nodes** [M. Roncken et al., 2015], where:

- Links are **communication channels**, with data flowing in the direction of the edges representing the links.
- Joints are modules that implement **flow control** and **data operations**.

Data are stored in links, not in joints. Data flow from one end of the link to the other end, and are captured in-between.

# Link and Joint

A **link** receives `fill` or `drain` commands from and reports its `full/empty` state to its corresponding joints. When a link receives a `fill` command, it changes its state to `full`. A link will change to the `empty` state if it receives a `drain` command.

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A **joint** receives the `full/empty` states of its links and issues the `fill` and `drain` commands when the `handshake condition` is satisfied. In particular, whenever its `incoming links are full` and its `outgoing links are empty`, it will perform the following three actions in parallel:

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- hand-over data computed from the incoming links to the corresponding outgoing links,
- make the incoming links empty,
- make the outgoing links full.

# Handshake Protocol Using the Link-Joint Interface

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Demo: Modeling a simple while-loop circuit in an asynchronous manner using the link-joint interface.



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Develop more efficient decomposition-proof methods in asynchronous circuits.

Extend the DE system to modeling non-deterministic behavior in asynchronous circuits.

Implement tools and techniques for building and analyzing asynchronous circuits in a more automated manner.



W. Hunt (2000)

The DE Language

*Computer-Aided Reasoning: ACL2 Case Studies*, Kluwer Academic Publishers  
Norwell, MA, USA, 151 – 166.



M. Roncken, S. Gilla, H. Park, N. Jamadagni, C. Cowan, I. Sutherland (2015)

Naturalized Communication and Testing

*ASYNC 2015*, 77 – 84.

# Thank You!