A DE Verification Framework for Asynchronous Circuit Verification

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Outline

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Introduction

Synchronous circuits (Clocked circuits): changes in the state of storage elements are synchronized by **a global clock signal**.

Asynchronous circuits (Self-timed circuits): there is no global clock signal distributed in asynchronous circuits. The communication between components is performed via **local communication protocols**.

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Why asynchronous?

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Why asynchronous?

- Low power consumption,
- High operating speed,
- Better composability and modularity,
- ...

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  - no global clock signal,
  - local communication protocols,
  - non-deterministic behavior due to *variable delays* in wires and gates.

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DE is a formal occurrence-oriented hardware description language for describing Mealy machines. It allows **hierarchical module definition**, and multiple copies of a module are identified by reference (their appearance in an occurrence).

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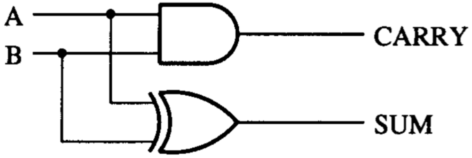
Each occurrence consists of four elements: a module-unique occurrence name, outputs, **a reference to a primitive or defined module**, and inputs.

Half-Adder



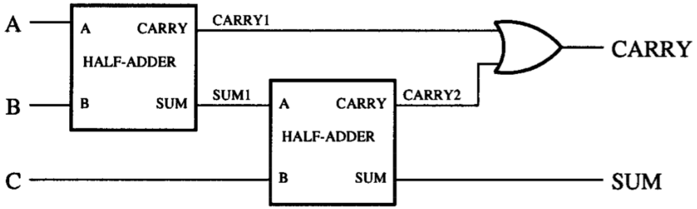
```
(defconst *half-adder*
  '((half-adder    ;; module name
     (a b)         ;; module inputs
     (sum carry)   ;; module outputs
     ()            ;; internal states
      ;; occurrences
     ((g0       ;; occurrence name
       (sum)    ;; occurrence outputs
       b-xor    ;; a primitive reference
       (a b))   ;; occurrence inputs
      (g1 (carry) b-and (a b))))))
```

The DE Primitive Database

The evaluation of a DE netlist eventually results in the interpretation of **primitives**, which are specified in the DE primitive database.

- Logic gates: AND, OR, NOT, XOR,...
- State-holding primitives: latches, flip-flops,...

Full-Adder

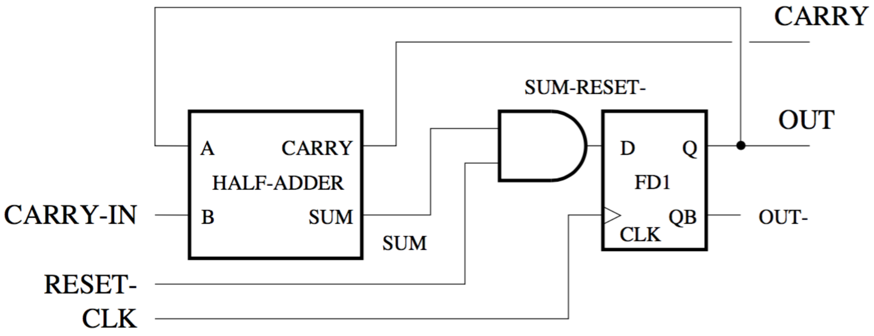

A
B
C
A
CARRY
HALF-ADDER
B
SUM
CARRY1
SUM1
A
CARRY
HALF-ADDER
B
SUM
CARRY2
CARRY
SUM

Full-Adder

```
(defconst *full-adder*
  (cons
   '(full-adder
     (a b c)
     (sum carry)
     ()
     ((t0 (sum1 carry1) half-adder           (a b))
      (t1 (sum  carry2) half-adder        (sum1 c))
      (t2 (carry)       b-or       (carry1 carry2))))

   *half-adder*))
```

One-Bit Counter



One-Bit Counter

```
(defconst *one-bit-counter*
  (cons
   '(one-bit-counter
     (clk carry-in reset-)
     (out carry)
     (g0)
     ((g0 (out out~)   fd1         (clk sum-reset-))
      (g1 (sum carry)  half-adder   (carry-in out))
      (g2 (sum-reset-) b-and          (sum reset-))))

   *half-adder*))
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- The `de` function computes the **next state** of a module being evaluated given its inputs and its current state.

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- The `de` function computes the **next state** of a module being evaluated given its inputs and its current state. The `de-occ` function, which is mutually recursive with `de`, iteratively computes the (possibly empty) **next state** of each occurrence declared in the module.

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This approach has been demonstrated its **scalability** to large systems, as shown on contemporary x86 designs at Centaur Technology [A. Slobodova et al., 2011].

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Modeling

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- Local communication protocols
- Non-deterministic behavior

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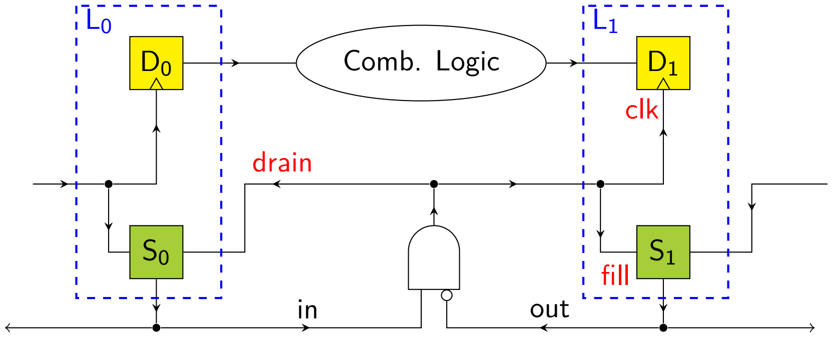
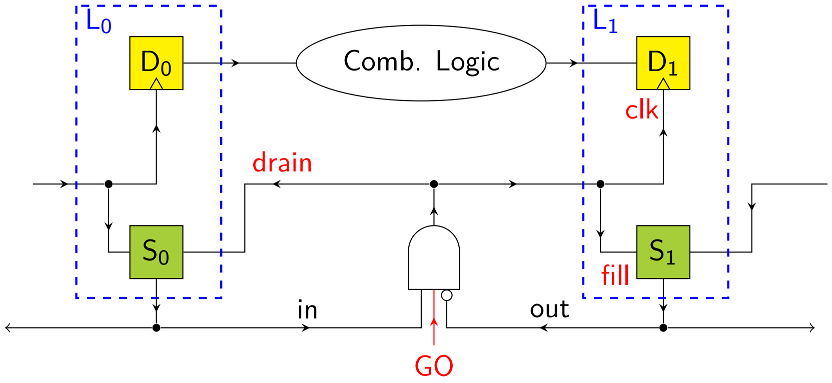
- Non-deterministic behavior
  $\Rightarrow$ Employing an oracle.

The Link-Joint Interface



The Link-Joint Interface



Verification

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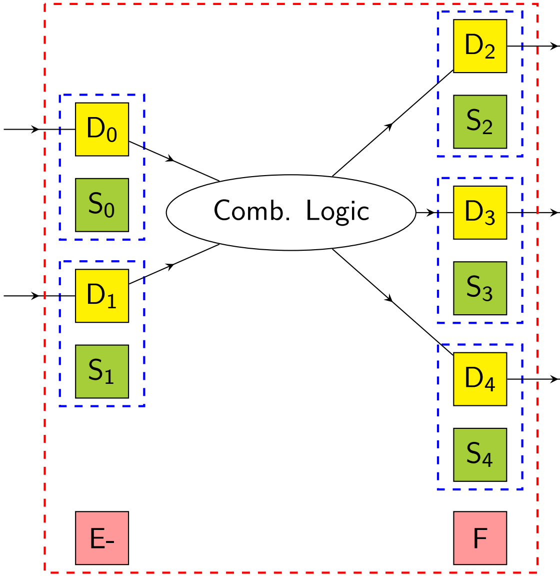
Asynchronous modules are treated as **communication links** that communicate with each other via local communication protocols.

Async Modules vs. Primitive Links

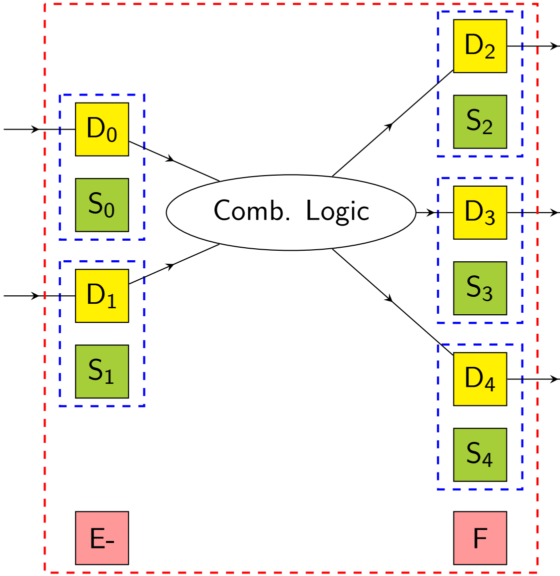


Async Modules vs. Primitive Links

Communication status:

Async modules: full, empty, both full and empty, not ready (neither full nor empty).

Primitive links: either full or empty.



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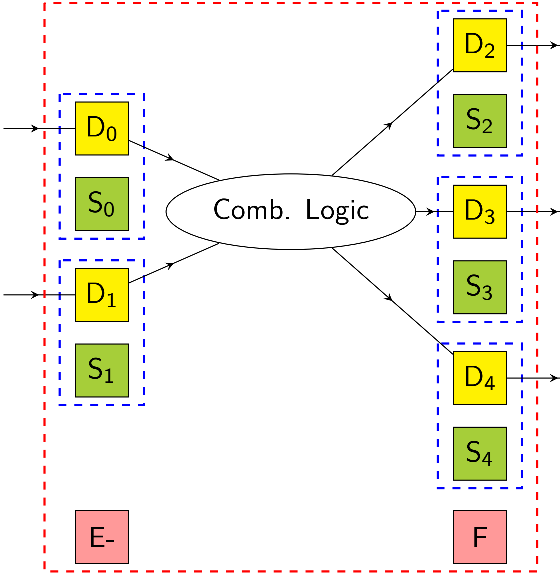
Communication signals:

Async modules use separate incoming and outgoing communication signals.

Primitive links only need one signal for both incoming and outgoing communications.



Dealing with Non-determinism

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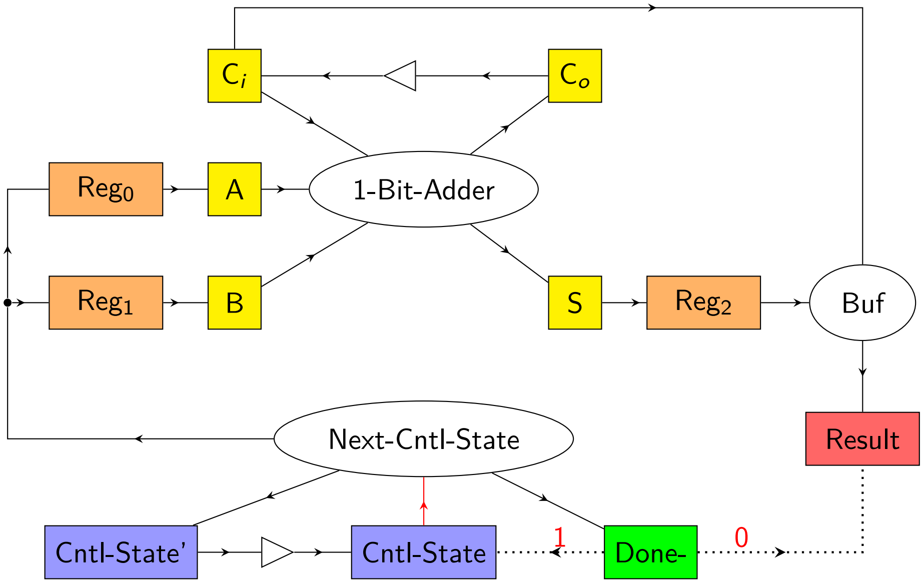
Simplifying the verification task by reducing non-determinism, and consequently reducing the state space.

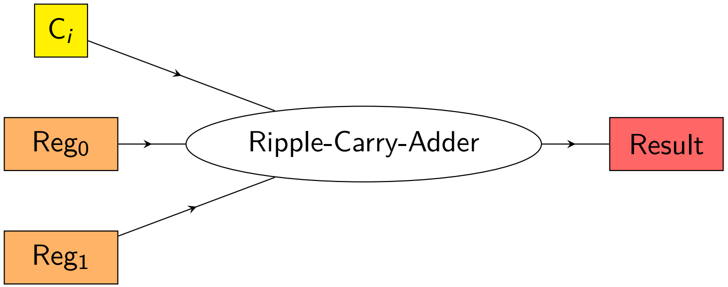
- Imposing extra **sequential dependencies** among operations in asynchronous circuits. In particular, a module is ready to communicate with other modules only if **it finishes all of its internal operations and becomes quiescent**.

Outline

Serial Adder



Ripple-Carry Adder



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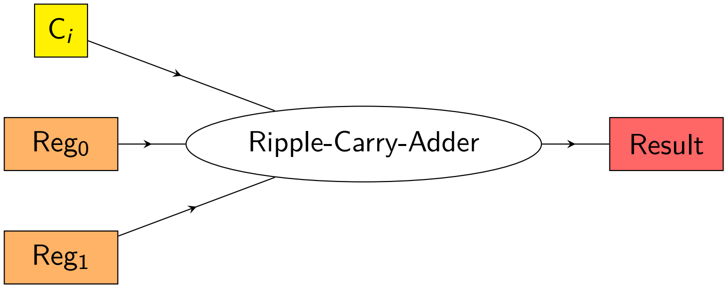
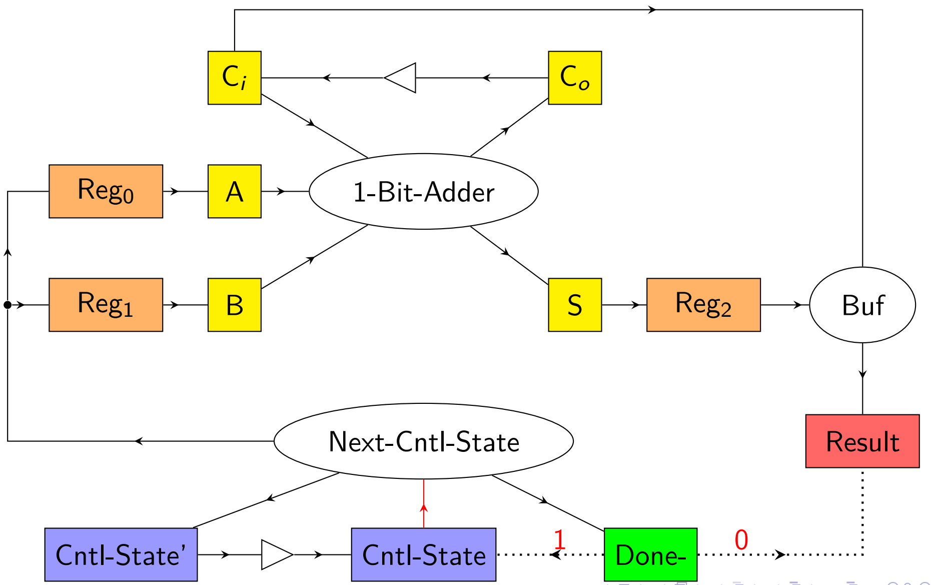


Goal: Given an appropriate initial condition, prove that the asynchronous serial adder produces the same result with the ripple-carry adder.

Serial Adder



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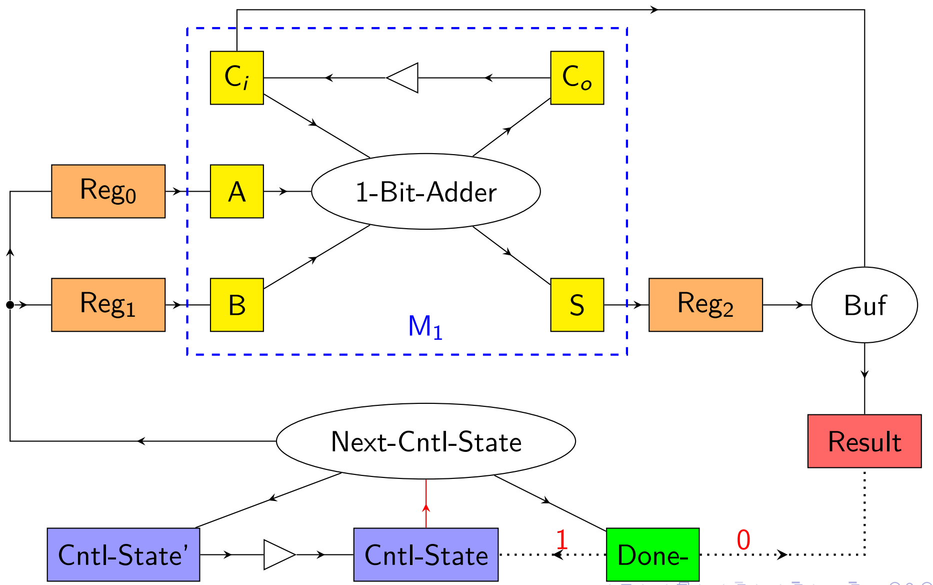

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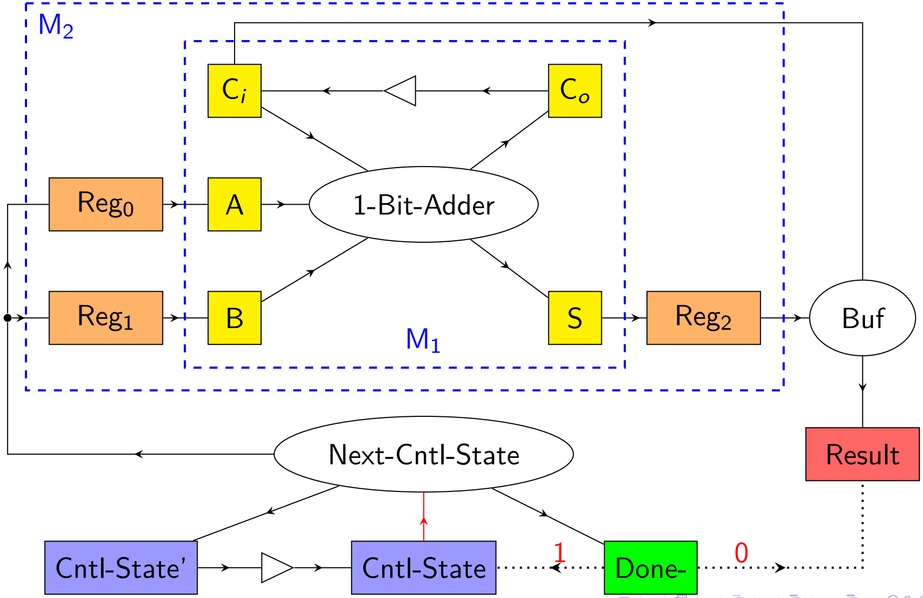

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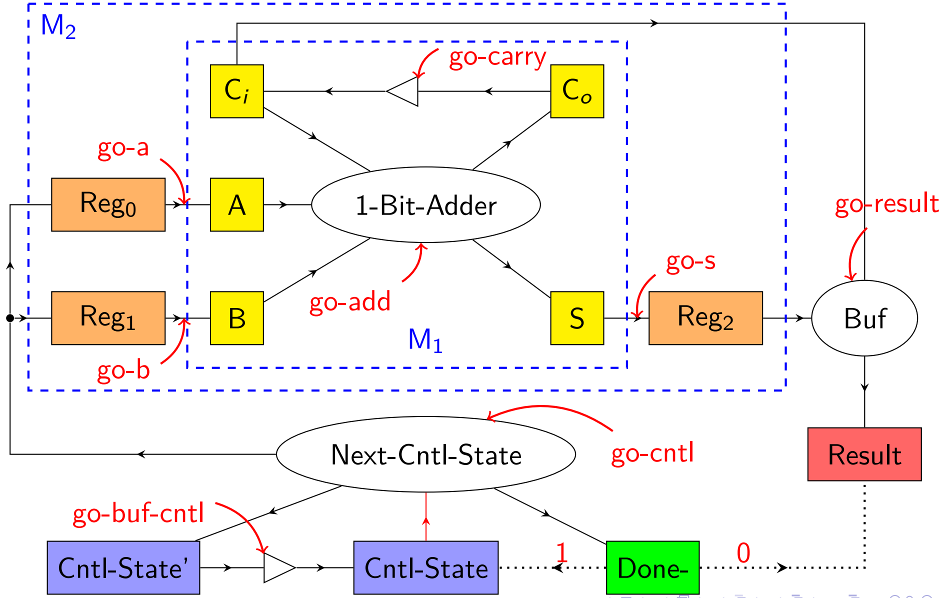

Dependency

$$\begin{tikzcd}
\text{go-a} \arrow[dr] & & & & \\
& \text{go-add} \arrow[r] & \text{go-carry} \arrow[r] & \text{go-s} \arrow[dr] & \\
\text{go-b} \arrow[ur] & & & & \text{go-cntl} \arrow[uullll, red, bend right] \arrow[llll, red, bend left] \arrow[dl, red, bend left] \\
& & & \text{go-buf-cntl} \arrow[ur] &
\end{tikzcd}$$

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Interleaving Example

Inputs = `((...  go-a0 go-b0) (...  go-a1 go-b1) ...)`

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Interleaving Example

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- `(go-a go-b)` ⇒ `((...  T F) (...  go-a1 T) ...)`
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- `((go-a go-b))` ⇒ `((...  T T) ...)`

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Conclusions

We have presented our framework for modeling and verifying asynchronous circuits using the DE system.

Hierarchical verification is critical to circuit verification.

Reasoning with highly non-deterministic behavior is burdensome to asynchronous circuit verification.

References

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A Flexible Formal Verification Framework for Industrial Scale Validation
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PhD Plan

Phase 1: Pick a topic

Phase 2: ?

Phase 3: Defend

Questions?