A Framework for Asynchronous Circuit Modeling and Verification in ACL2

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Outline

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Introduction

Synchronous circuits (or clock-driven circuits): changes in the state of storage elements are synchronized by **a global clock signal**.

Asynchronous circuits (or self-timed circuits): there is no global clock signal distributed in asynchronous circuits. The communications between state-holding elements are performed via **local communication protocols**.

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Why asynchronous?

- Low power consumption,
- High operating speed,
- Elimination of clock skew problems,
- Better composability and modularity for large systems,
- ...

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- We use the DE system [Hunt:2000], which is built in ACL2, to specify and verify self-timed circuit designs.
- Developing a hierarchical verification approach to support scalability.
- Exploring strategies for reasoning with non-deterministic circuit behavior.

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The DE System

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- These lemmas are used to prove the correctness of yet larger modules containing these submodules, **without the need to dig into any details about the submodules**.
- This approach has been demonstrated its **scalability** to large systems, as shown on contemporary x86 designs at Centaur Technology [Slobodova et al.:2011].

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Modeling

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- Local communication protocols
- Non-deterministic behavior due to variable delays in wires and gates

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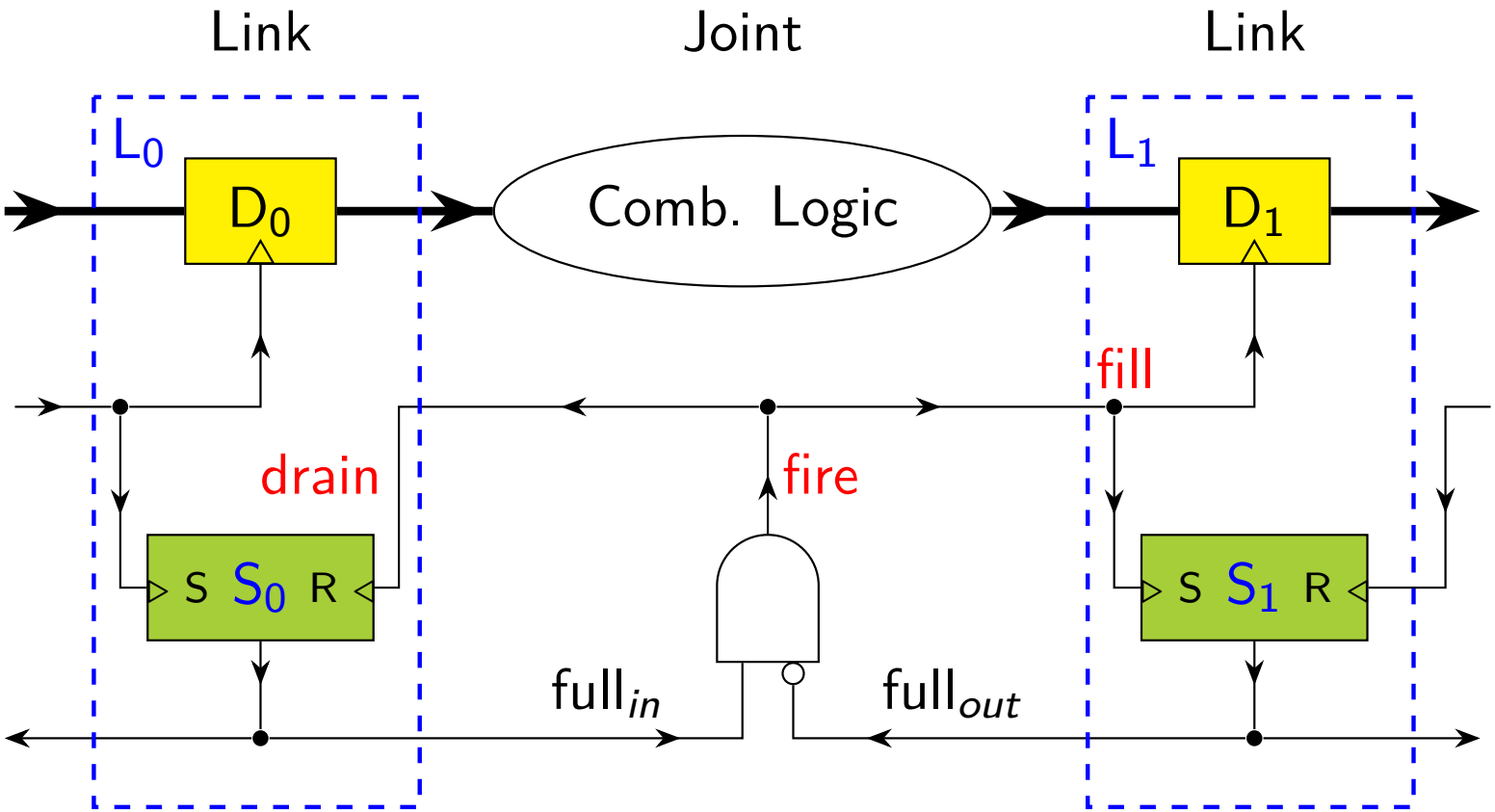
- Joints are handshake components that implement **flow control** and **data operations**.

Joints are the meeting points for links to **coordinate states** and **exchange data**.

The Link-Joint Model



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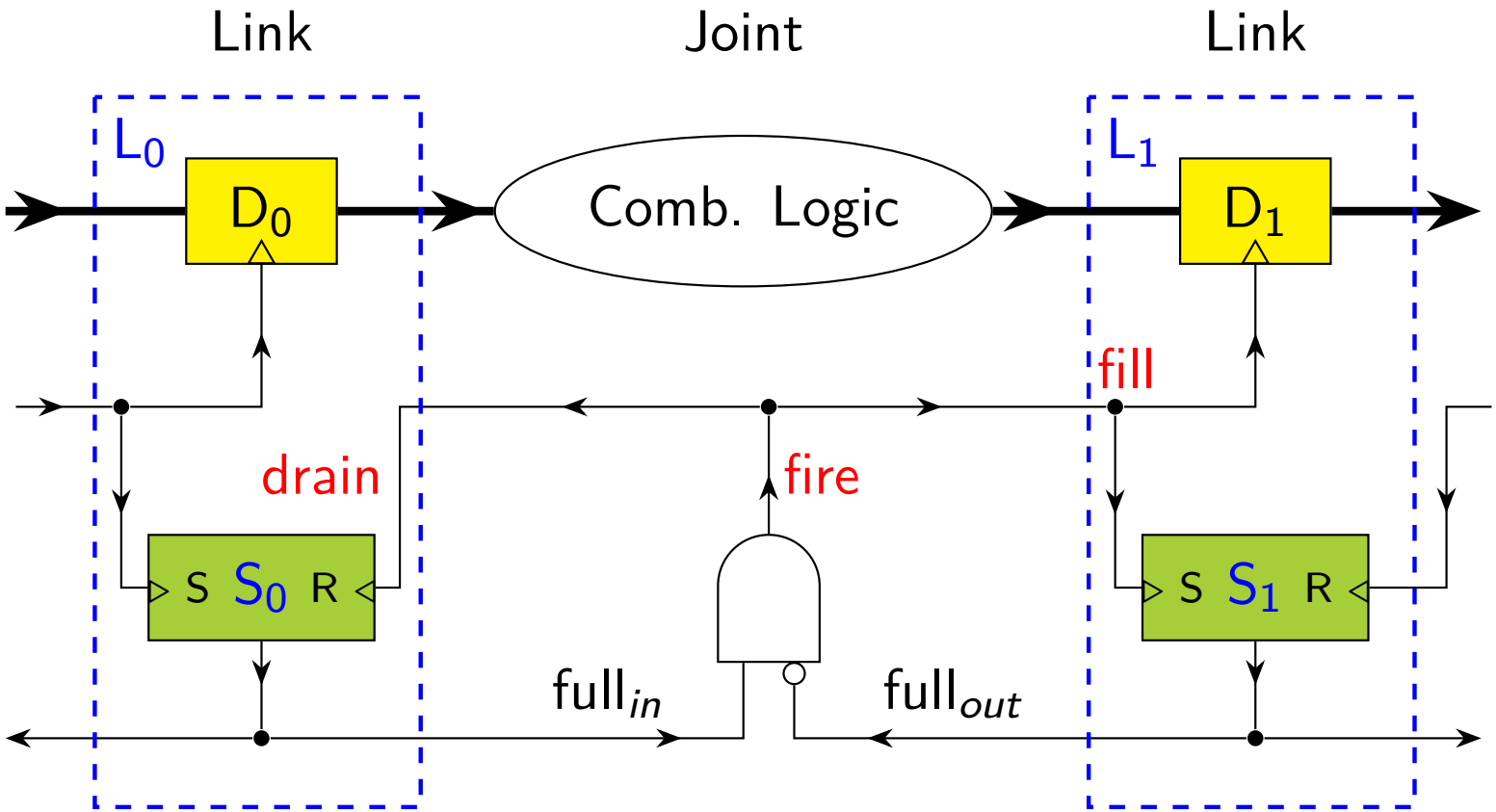

A joint can have several input and output links connected to it.

Necessary conditions for a joint to fire: all of its input links are **full** and all of its output links are **empty**.

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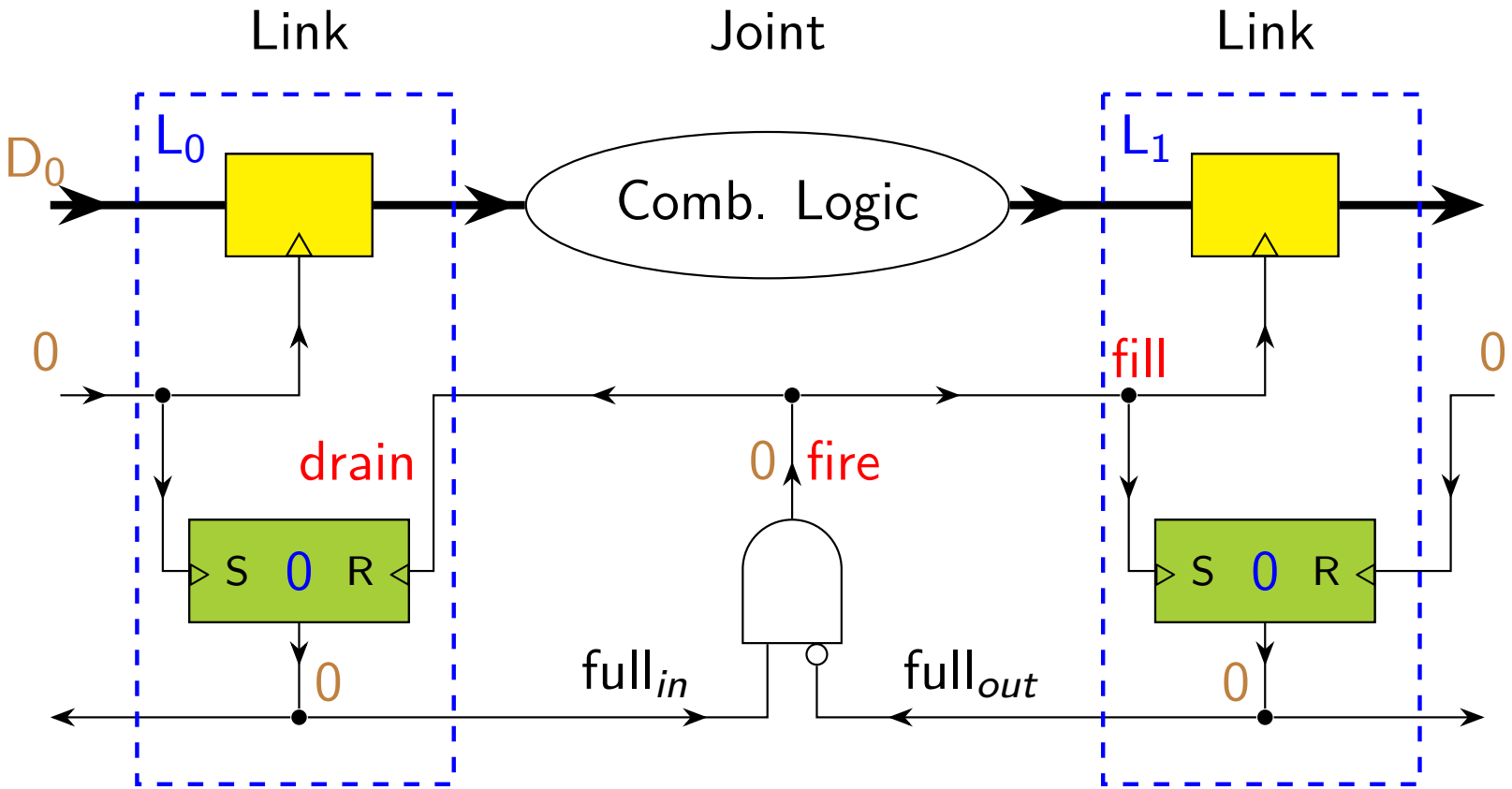

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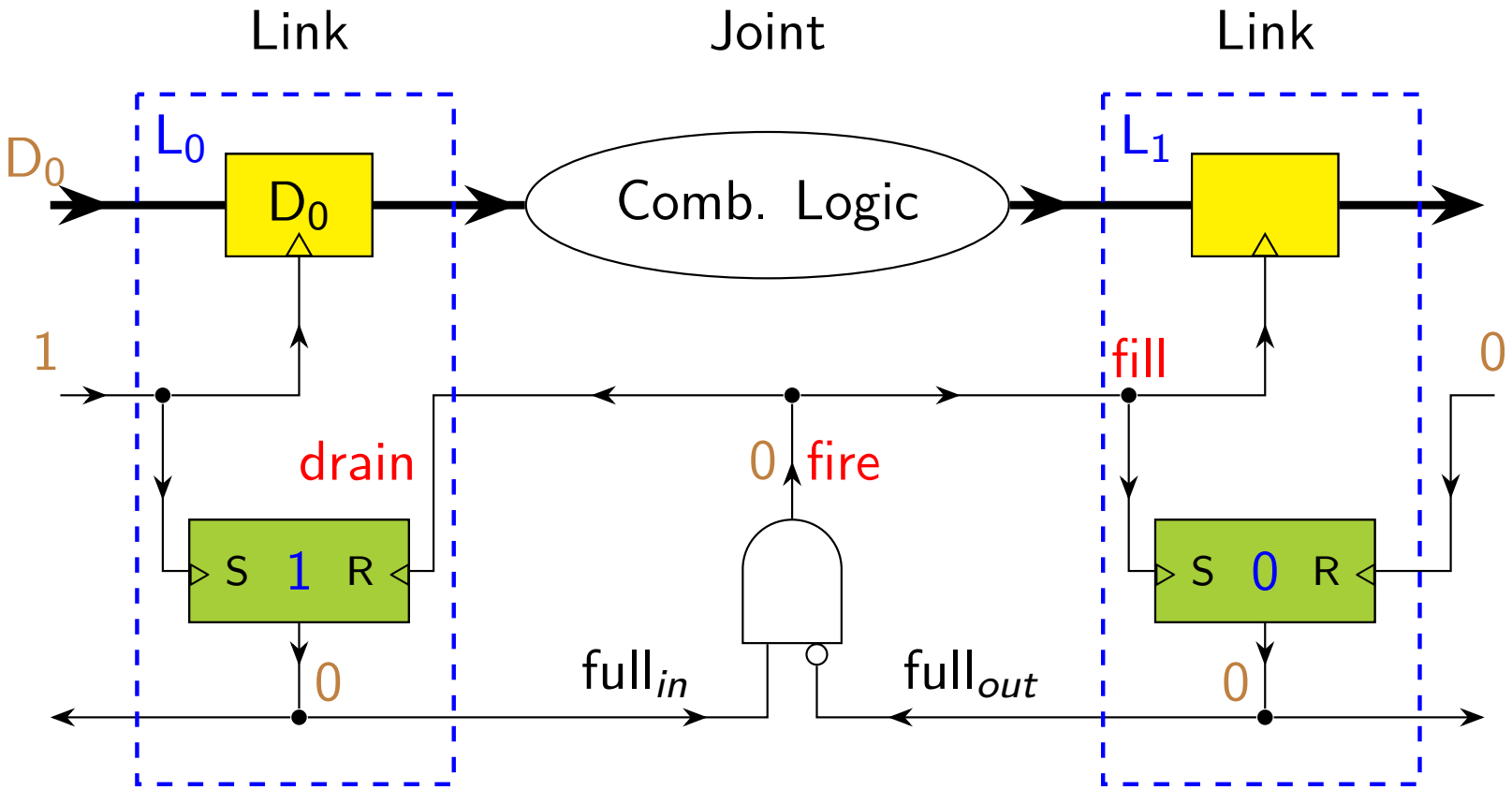

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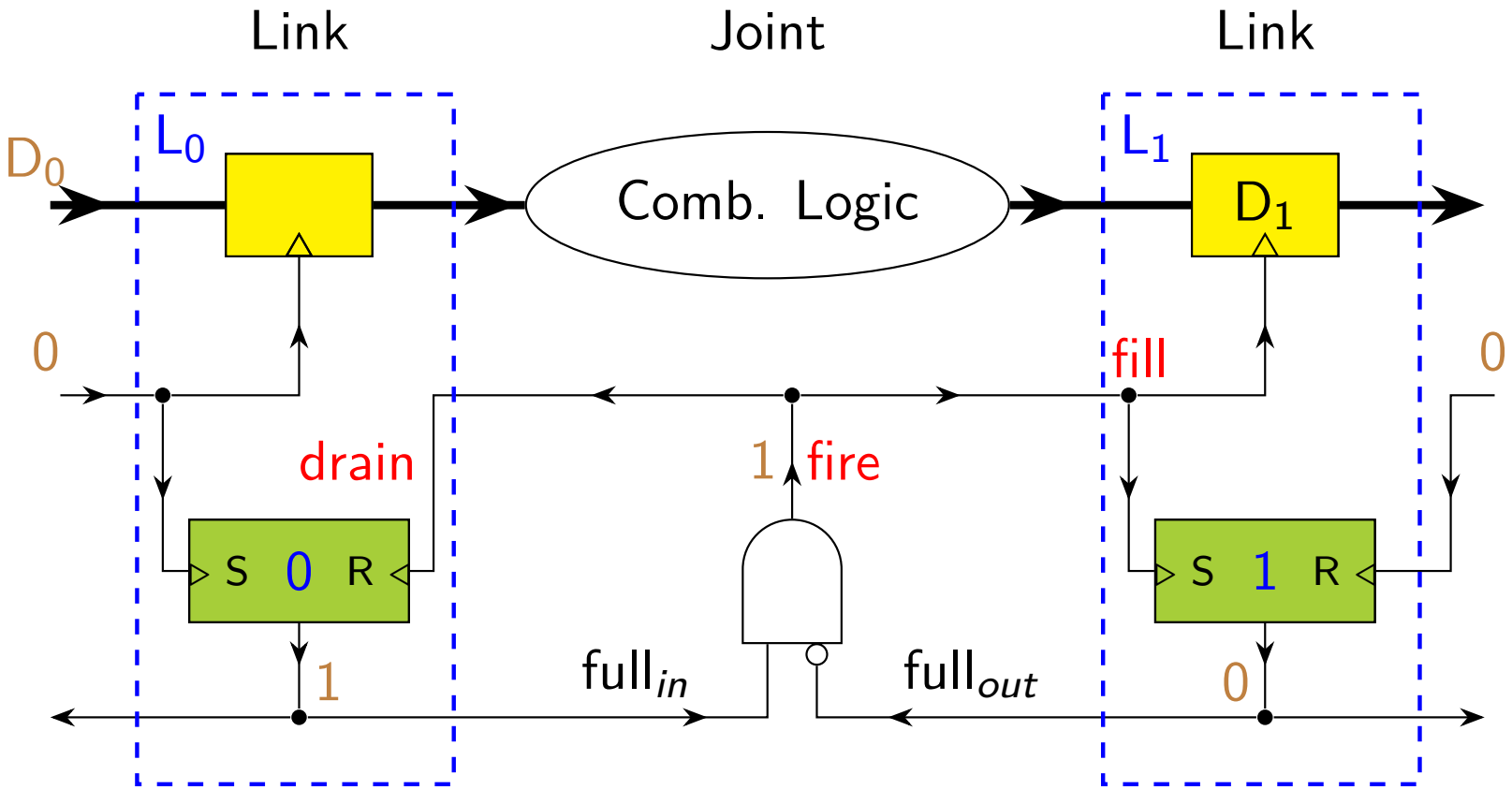

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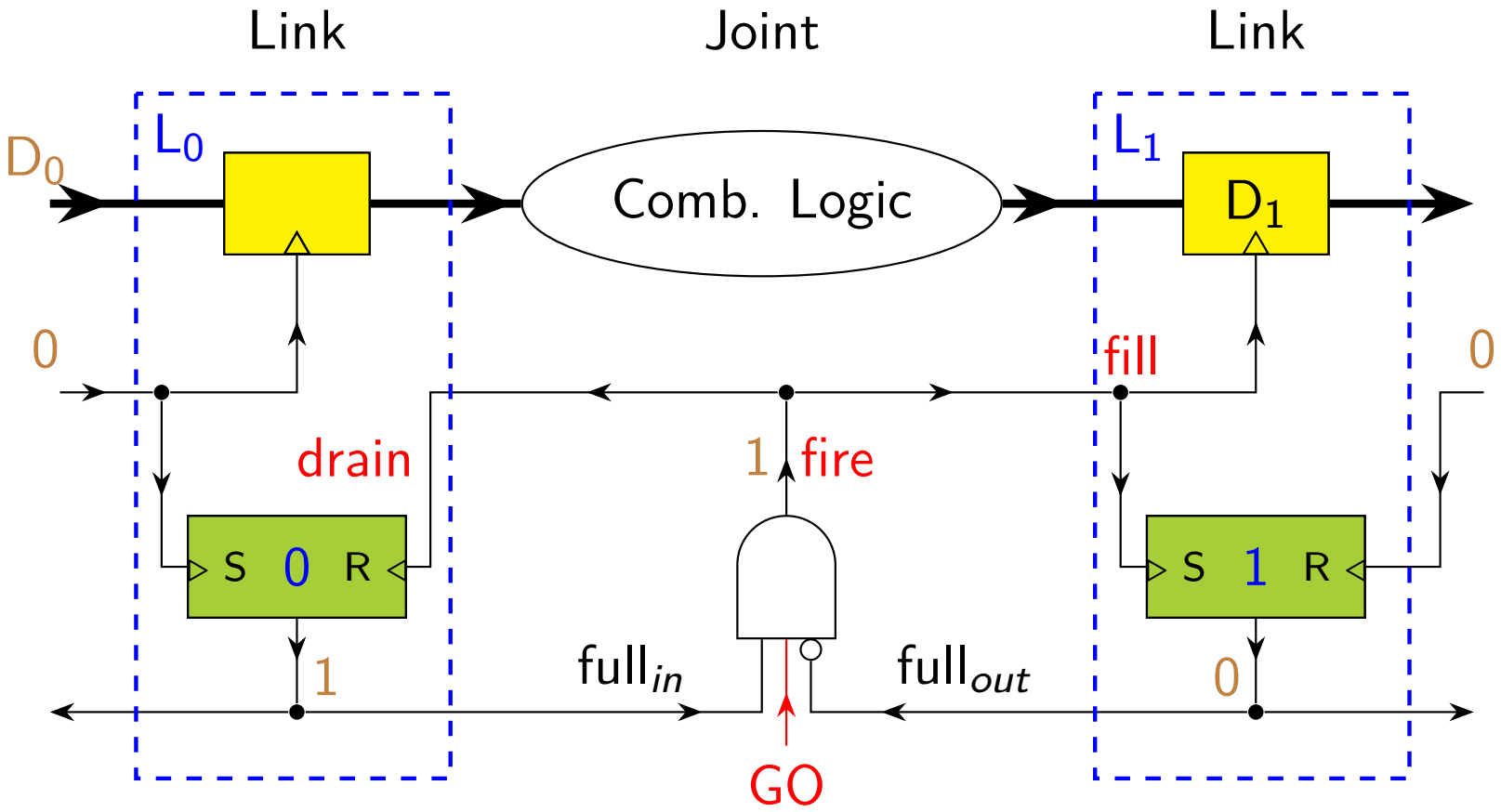

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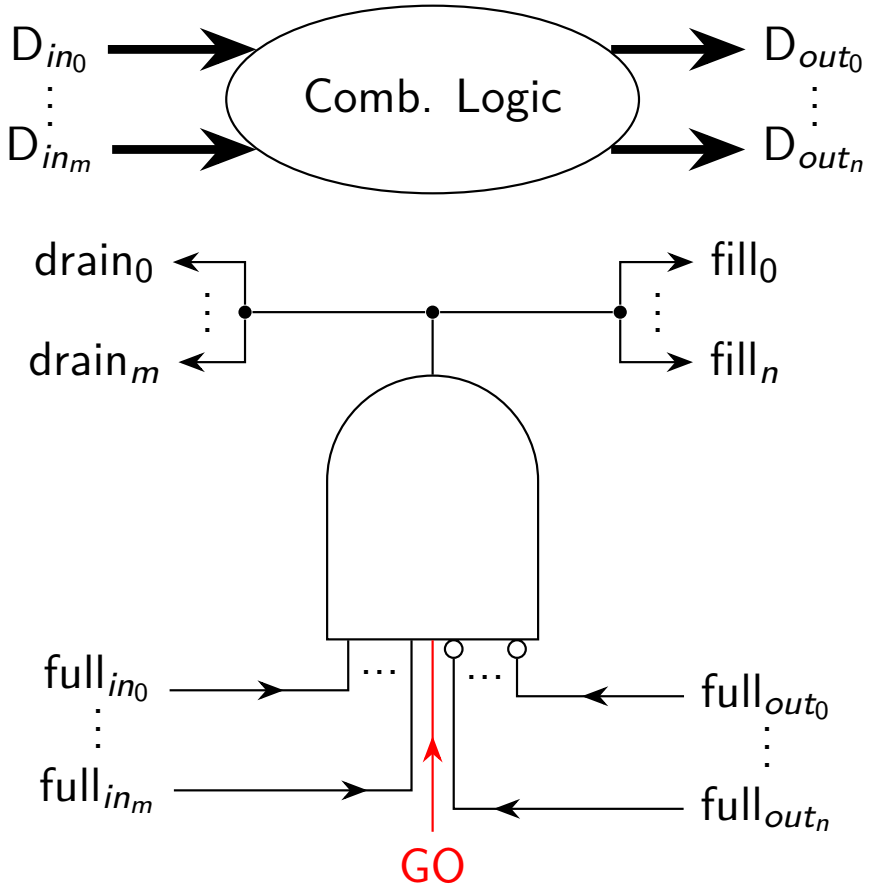


When a joint fires, the following three actions will be executed in parallel:

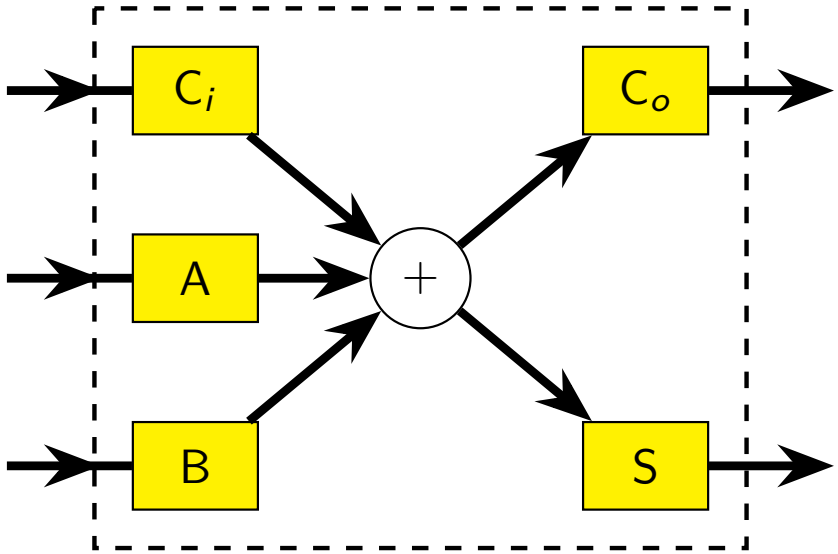
- transfer data computed from the input links to the output links,
- fill the output links, make them **full**,
- drain the input links, make them **empty**.

Verification

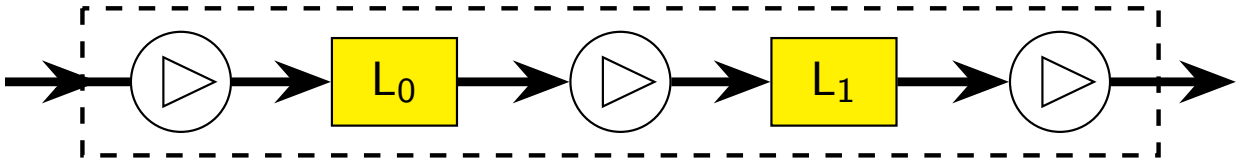
Our framework applies a hierarchical verification approach to formalizing single transitions of circuit behavior (simulated by `se` and `de` functions).

- The output and next state of a module are formalized using the formalized outputs and next states of submodules, without delving into details about the submodules.
- Self-timed modules can be abstracted as "complex" links or "complex" joints.

Self-Timed Modules



A complex link: an adder



A complex joint: a queue $Q2$ of two links

Verification

Compositional reasoning:

- Functional properties of self-timed systems may involve multi-step executions that are quite burdensome to establish directly.
- Decompose the executions into smaller steps in such a way that sub-properties after executing each of these smaller steps can be carried out much easier.
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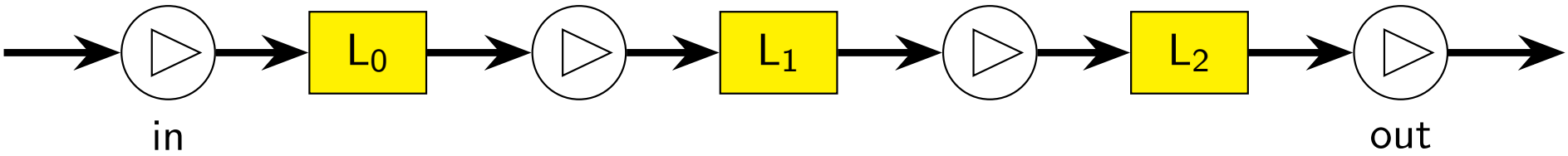
Induction:

- We use induction to prove properties of systems over time, for instance, the relationship between input and output sequences.
- We also apply induction to establishing **loop invariants** of iterative circuits, i.e., circuits with feedback loops.

Outline

Circuits with No Feedback Loops

$Q3$



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Circuits with No Feedback Loops

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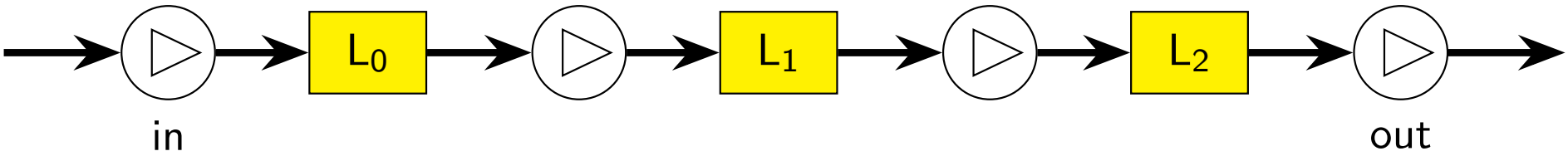

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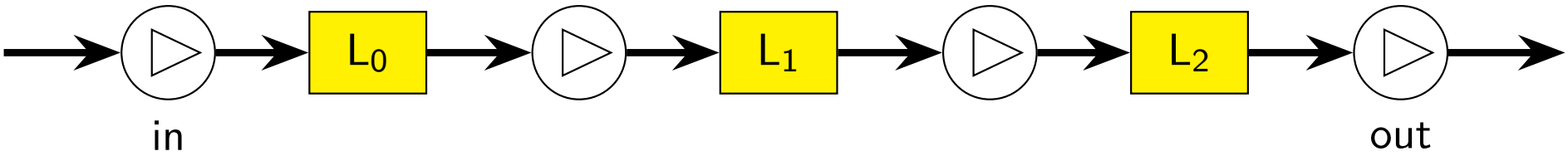

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Module $Q3$ will accept a new input if the **in-act** signal is high. In this case, we call this input valid. We define a (valid) input sequence as a sequence of valid inputs.

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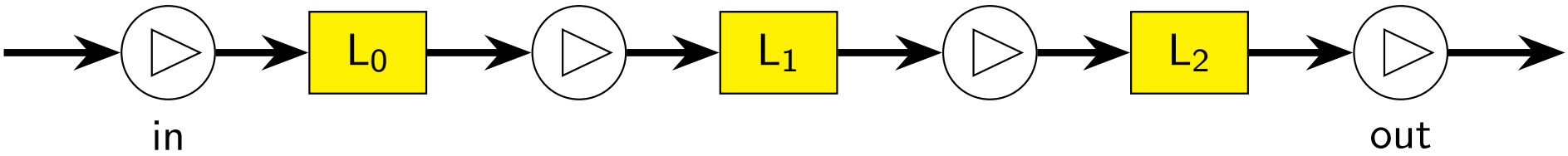

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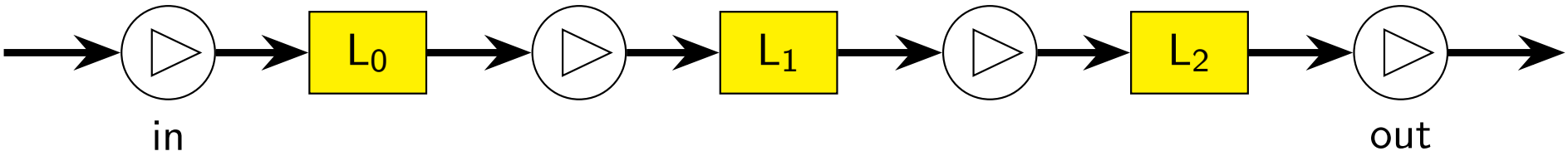
Similarly, we define a (valid) output sequence as a sequence of valid outputs. $Q3$ will report a valid output when the **out-act** signal is high.

Circuits with No Feedback Loops

$Q3$



We define the function **q3$extract-data(st)** that extracts valid data from state *st* of $Q3$, i.e. extracts data from links that are **full** at state *st*. The following equality states the functional correctness of $Q3$:

$$q3\$extract\text{-}data(q3\$run(input\text{-}list, st, n)) \mathbin{++} out\text{-}seq = in\text{-}seq \mathbin{++} q3\$extract\text{-}data(st)$$

where

```
q3$run(input-list, st, n) :=
  if (n <= 0)
     st
  else q3$run(rest(input-list),
              q3$step(first(input-list), st),
              n - 1)
```

Circuits with No Feedback Loops

$$q3\$extract\text{-}data(q3\$run(input\text{-}list, st, n)) \mathbin{++} out\text{-}seq = in\text{-}seq \mathbin{++} q3\$extract\text{-}data(st) \quad (1)$$

Our ACL2 proof of (1) uses **induction** and the following single-step-update property of $Q3$ as a supporting lemma:

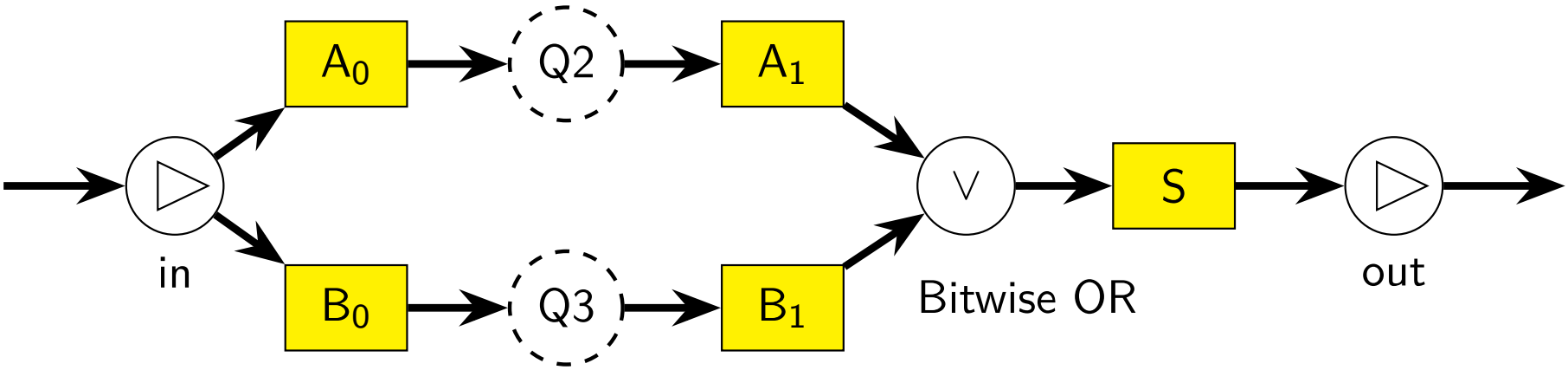
$$q3\$extract\text{-}data(q3\$step(input, st)) = q3\$step\text{-}spec(input, st) \quad (2)$$

where $q3\$step\text{-}spec(input, st) :=$

$$\begin{cases} q3\$extract\text{-}data(st), \text{ if } in\text{-}act = F \wedge out\text{-}act = F \\ [input] \mathbin{++} q3\$extract\text{-}data(st), \text{ if } in\text{-}act = T \wedge out\text{-}act = F \\ remove\text{-}last(q3\$extract\text{-}data(st)), \text{ if } in\text{-}act = F \wedge out\text{-}act = T \\ [input] \mathbin{++} remove\text{-}last(q3\$extract\text{-}data(st)), \text{otherwise} \end{cases}$$

Circuits with No Feedback Loops

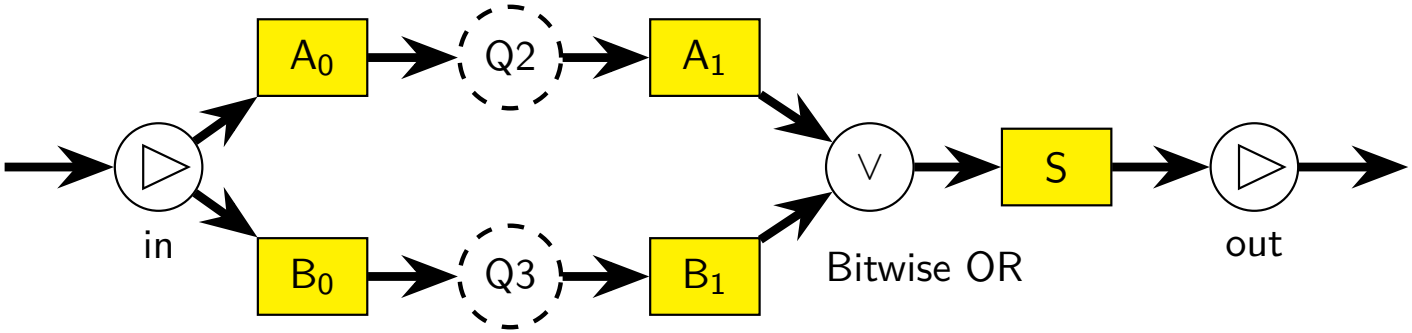
C



In terms of input-output relationship, C simply performs the bitwise OR operation on the two input operands. The operation of C over the input sequence is defined as follows:

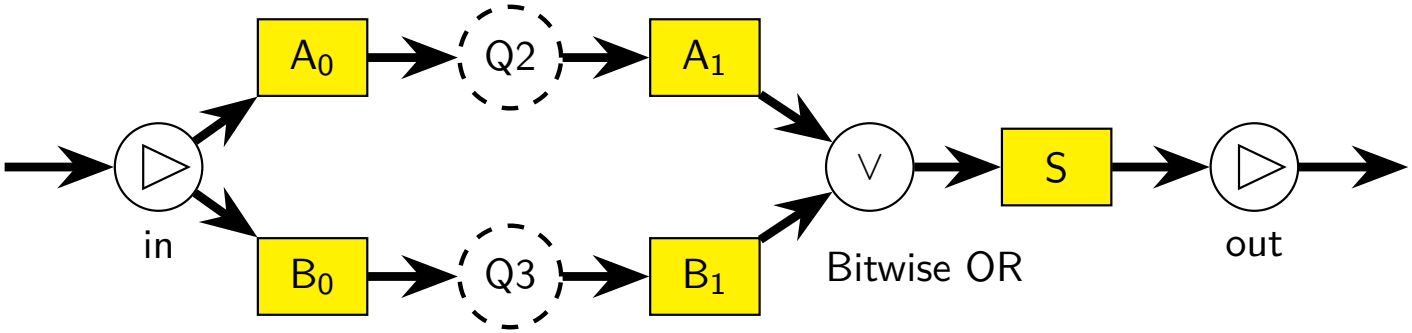
```
c$op(in-seq) :=
  if (in-seq is empty) nil
  else {
    let {
      input := first(in-seq)
      a := first(input)
      b := second(input)}
    [v-or(a, b)] ++ c$op(rest(in-seq))}
```

Circuits with No Feedback Loops




```
c$extract-data(st) :=
  c$op(extract-data(st.a0 ++ st.Q2 ++ st.a1) ⊗
       extract-data(st.b0 ++ st.Q3 ++ st.b1))
  ++
  extract-data(st.s)
```

Circuits with No Feedback Loops

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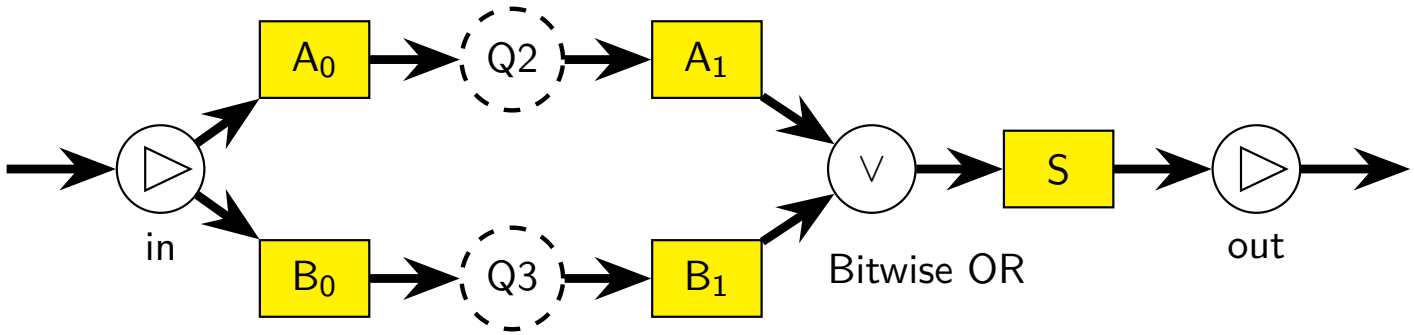
If the current state st of C satisfies the following condition:

$$size(extract\text{-}data(st.a0 \mathbin{++} st.Q2 \mathbin{++} st.a1)) = size(extract\text{-}data(st.b0 \mathbin{++} st.Q3 \mathbin{++} st.b1)) \quad (3)$$

then the following functional property of C holds:

$$c\$extract\text{-}data(c\$run(input\text{-}list, st, n)) \mathbin{++} out\text{-}seq = c\$op(in\text{-}seq) \mathbin{++} c\$extract\text{-}data(st) \quad (4)$$

Circuits with No Feedback Loops



Our ACL2 proof of (4) uses **induction** and the single-step-update property (described below, given that (3) holds) as a supporting lemma.

$$c\$extract\text{-}data(c\$step(input, st)) = c\$step\text{-}spec(input, st) \qquad (5)$$

where $c\$step\text{-}spec(input, st) :=$

$$\begin{cases} c\$extract\text{-}data(st), in\text{-}act = F \wedge out\text{-}act = F \\ [v\text{-}or(input.a, input.b)] \mathbin{++} c\$extract\text{-}data(st), in\text{-}act = T \wedge out\text{-}act = F \\ remove\text{-}last(c\$extract\text{-}data(st)), in\text{-}act = F \wedge out\text{-}act = T \\ [v\text{-}or(input.a, input.b)] \mathbin{++} remove\text{-}last(c\$extract\text{-}data(st)), \text{ otherwise} \end{cases}$$

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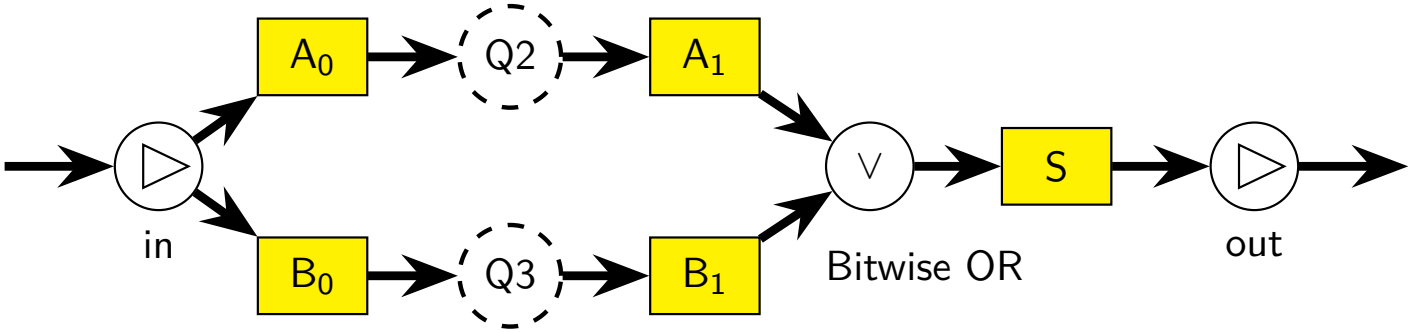

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$$c\$extract\text{-}data(c\$step(input, st)) = c\$step\text{-}spec(input, st) \qquad (5)$$

Our proof of (5) does not concern the details of $Q2$ and $Q3$. All we need to know about these two modules in proving (5) is their single-step-update properties.

In other words, we employ a hierarchical strategy in proving the single-step-update property of a self-timed module.

Circuits with No Feedback Loops

In summary, for each self-timed module that has no feedback loops, we prove the following two properties:

1. the single-step-update property (proved by using hierarchical reasoning),
2. the relationship between the input and output sequences (proved by using induction and the single-step-update property).

Circuits with Feedback Loops

Reasoning with highly non-deterministic behavior in self-timed systems with feedback loops is very challenging.

- Computing loop invariants in these systems becomes much more complicated than in synchronous systems.

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We impose design restrictions on iterative circuits to reduce non-determinism, and consequently reduce the complexity of the set of execution paths:

- These restrictions enable our framework to verify loop invariants efficiently via **induction** and subsequently verify the **functional correctness** of self-timed circuit designs.

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Design restrictions: A module is ready to communicate with other modules only when it finishes all of its internal operations and becomes quiescent.

32-Bit Self-Timed Serial Adder Verification

We demonstrate our framework by modeling and verifying the functional correctness of a 32-bit self-timed serial adder [Chau:2017].

We prove that the self-timed serial adder indeed performs the addition under an appropriate initial condition.

- When the adder finishes its execution, the result is proven to be the sum of the two 32-bit input operands and the carry-in.

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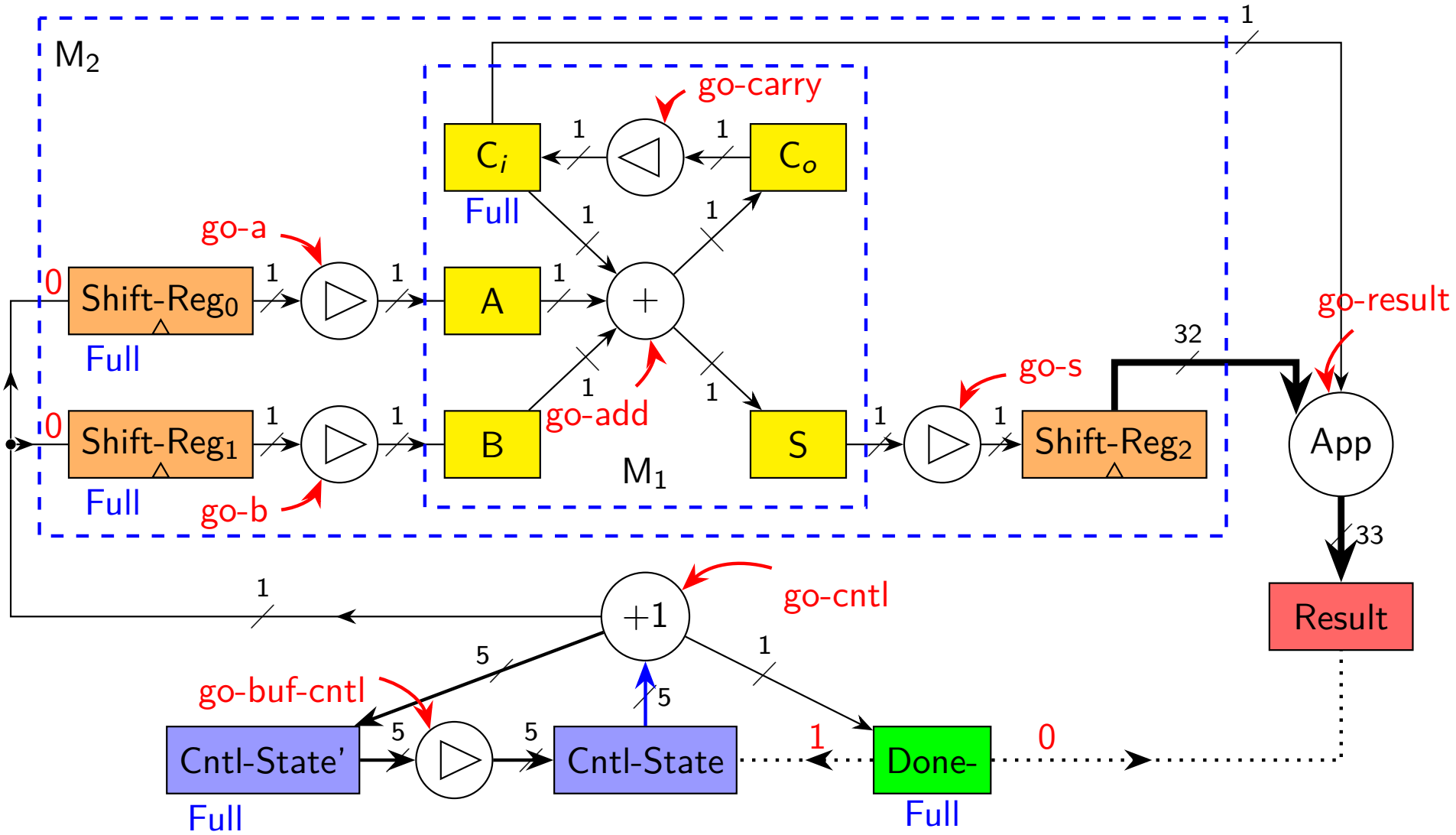
We prove that the self-timed serial adder indeed performs the addition under an appropriate initial condition.

- When the adder finishes its execution, the result is proven to be the sum of the two 32-bit input operands and the carry-in.

Our verification approach applies compositional reasoning.

- Divide the adder's execution into two parts: the loop part and the exit part (the execution after exiting the loop),
- Formalize a loop invariant for the loop part and the adder behavior during the exit part,
- Prove the functional correctness of the adder by glueing these two parts together.

Data Flow of a 32-Bit Self-Timed Serial Adder



Correctness Theorems

Theorem 1 (Partial correctness).

$$
\begin{aligned}
& \mathit{async\_serial\_adder}(\mathit{netlist}) \wedge && (6)\\
& \mathit{init\_state}(\mathit{st}) \wedge && (7)\\
& (\mathit{operand\_size} = 32) \wedge && (8)\\
& \mathit{interleavings\_spec}(\mathit{input\_seq}, \mathit{operand\_size}) \wedge && (9)\\
& (\mathit{st}' = \mathit{run}(\mathit{netlist}, \mathit{input\_seq}, \mathit{st}, n)) \wedge && (10)\\
& \mathit{full}(\mathit{result\_status}(\mathit{st}')) && (11)\\
\Rightarrow\ & (\mathit{result\_value}(\mathit{st}') = \mathit{shift\_reg\_0\_value}(\mathit{st}) + \\
& \qquad \mathit{shift\_reg\_1\_value}(\mathit{st}) + \\
& \qquad \mathit{ci\_value}(\mathit{st}))
\end{aligned}
$$

Correctness Theorems

Theorem 2 (Termination).

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& (\mathit{st}' = \mathit{run}(\mathit{netlist}, \mathit{input\_seq}, \mathit{st}, n)) \wedge && (10)\\
& (n \geq \mathit{num\_steps}(\mathit{input\_seq}, \mathit{operand\_size})) && (11')\\
\Rightarrow\ & \mathit{full}(\mathit{result\_status}(\mathit{st}')) &&
\end{aligned}
$$

Outline

Future Work

We are developing a new proof technique for partial correctness of iterative self-timed circuits that does not have any conditions on the values of **go** signals.

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We intend to follow a **hierarchical approach** to prove module-level properties of iterative circuits of the following form:

- Given an initial state of the module, the module's **final state** meets its specification after that module completes execution.

Conclusions

We have presented a framework for modeling and verifying self-timed circuits using the DE system.

Our goal is to develop a methodology that is capable of verifying the functional correctness of self-timed circuit designs at large scale.

- This work also provides libraries for analyzing self-timed systems in ACL2.

We model self-timed systems as networks of links communicating with each other locally via joints, using the link-joint model introduced by Roncken et al.

We also model the **non-determinism of event-ordering** in self-timed circuits by associating each joint with an external go signal.

Our key proof techniques are hierarchical reasoning, compositional reasoning, and induction.

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Questions?