Modeling and Verifying Asynchronous Circuits Using the DE System

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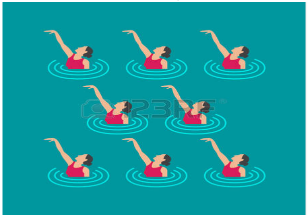
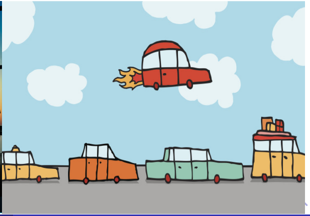
Introduction

Synchronous circuits (or clocked circuits): changes in the state of storage elements are synchronized by **a global clock signal**.



Asynchronous circuits (or self-timed circuits): no global clock signal. The communications between storage elements are performed via **local communication protocols**.



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Electrical-level timing analysis is conducted to assure that signal propagation of ready signals is always slower than data propagation so that **data are valid when transferred**.

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Scalable methods for self-timed system verification are highly desirable.

We are not aware of any scalable formal methods for validating functional properties of self-timed systems.

Goals and Impact

Goals:

- Develop scalable methods for reasoning about the functional correctness of self-timed circuits and systems, while **abstracting away circuit-level timing constraints**.
- Implement those methods using the ACL2 theorem proving system, providing a useful automated framework with associated libraries to support the mechanical analysis of general-purpose, self-timed circuit designs.

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Impact: If successful, this project will:

- advance the state-of-the-art in self-timed circuit specification and verification, and provide a means to support building **reliable complex hardware systems** using the self-timed paradigm; and thus,
- support a computing paradigm where **systems can proceed at their best rate and no longer require clock signals**.

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Develop a hierarchical reasoning approach that is amenable to verifying correctness of large, non-deterministic systems without a large growth of the time complexity.

- Avoid exploring the operations **internal to a verified submodule** as well as their interleavings.
- The **input-output relationship** of a verified submodule is determined based on the communication signals at the submodule's input and output ports, while **abstracting away all execution paths internal to that submodule**.

What Has Been Done?

- Extended the DE system to modeling self-timed circuit designs.
  - Extended the DE primitive database with a new link-control primitive that coordinates the means to update the state of a (storage) link.
  - Formally specified several self-timed circuit models using the extended DE system.

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  Implemented strategies for reasoning with non-deterministic circuit behavior efficiently.

- Successfully applied our verification approach to several self-timed circuit models.

Future Work

Goal: Demonstrate the effectiveness of our compositional, mechanized methodology for scalable formal verification of functional properties of self-timed circuit designs.

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- Verify a self-timed **serial adder** model without imposing the design restrictions inherent in our previous work [Chau et al.:2017].
- Demonstrate compositionality by certifying that the functionality of *gcd* is preserved when replacing its **combinational ripple-carry-adder** sub-circuit with a functionally-equivalent, **self-timed serial adder**.

Outline

1 The DE System

2 Modeling and Verification Approach

3 Case Studies

4 Conclusions

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- The DE simulator is used repeatedly to evaluate a circuit netlist description at **each global clock "tick"**.
- Prove the following two lemmas **hierarchically** for each module: a value lemma specifying the module's outputs and a state lemma specifying the module's next state.
- The value and state lemmas of **composite modules** are proved by automatic application of those lemmas of their submodules, **without the need to dig into any details about the submodules**.

The DE System

In our self-timed modeling, the DE simulator is called upon to carry out its function any time any primary input or internal state changes value.

Allow the design to proceed at its own rate moderated by **oracle** values — extra input values modeling non-determinacy — that can cause logic to **delay an arbitrary amount**.

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Extend the DE primitive database with a link-control primitive that models the **validity of data** stored in a communication link.

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- Joints are handshake components that implement **data operations** and **flow control**.
- Links are connected via joints, and joints are connected via links. A joint can have several input and output links connected to it, while a link connects exactly to one input and one output joint.

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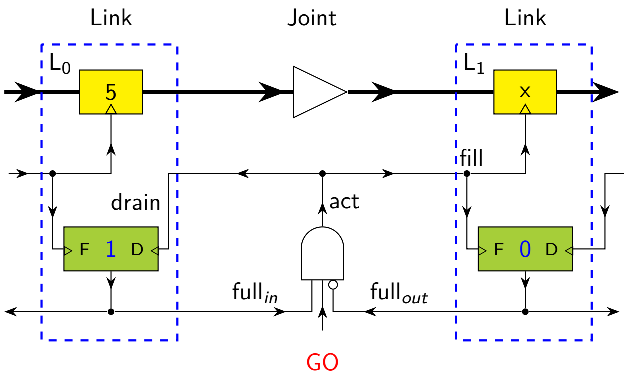
Necessary conditions for a **joint-action** to fire: all input and output links of that action are **full** and **empty**, respectively.

The Link-Joint Model



The green boxes represent the instances of the link-control primitive that is added to the DE primitive database.

When a joint acts, three tasks will be executed in parallel:

- transfer data computed from the input links to the output links;
- fill a subset of the output links, leaving them **full**;
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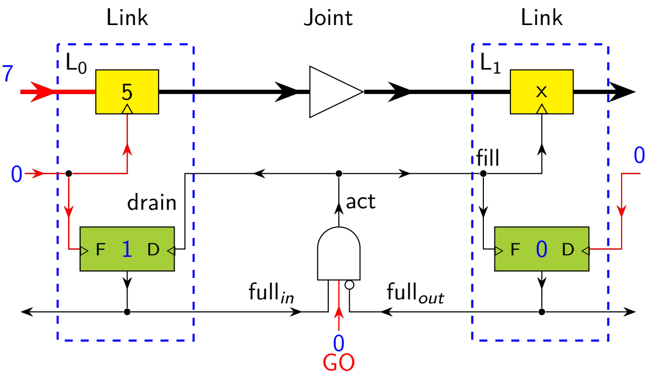

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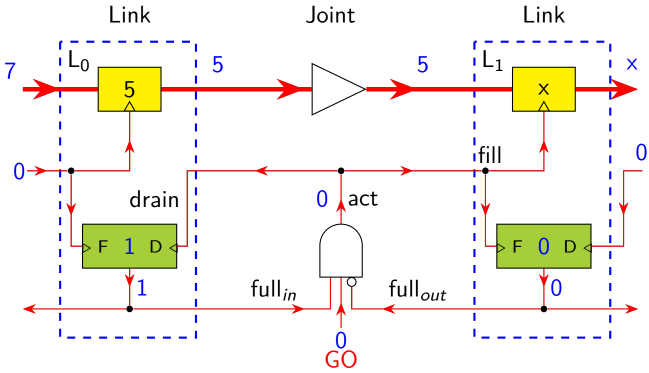

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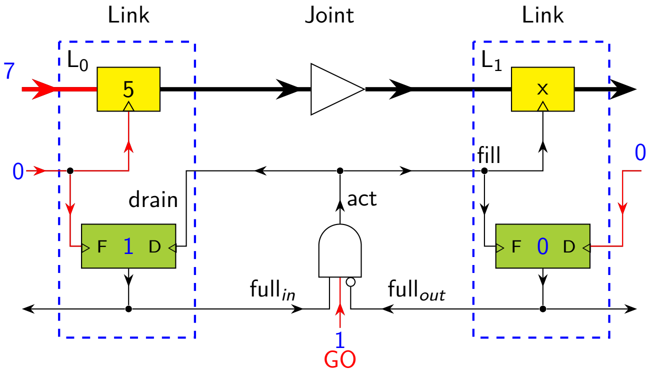

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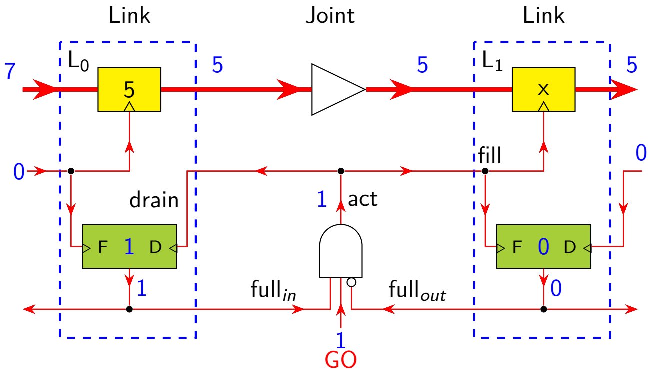

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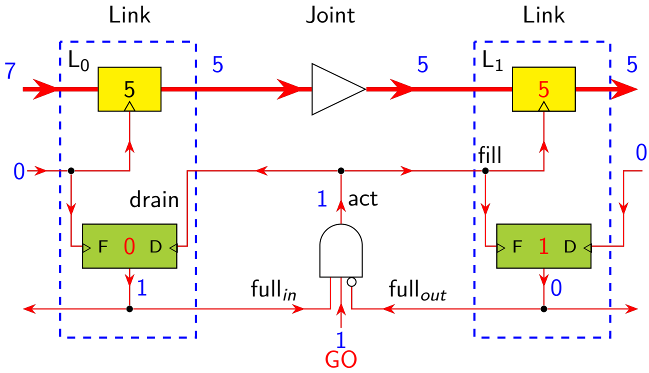

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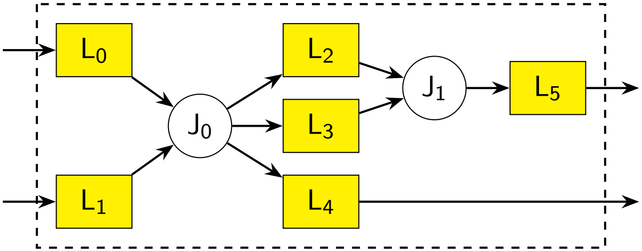
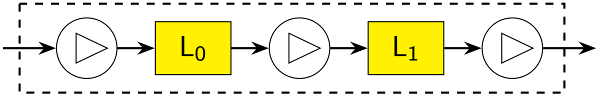
Self-Timed Modules



Complex link



Complex joint: a queue of length two, *Q*2

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Objective: Verify the **functional correctness** of self-timed circuit designs.

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- Formalize the relationship between input and output sequences.
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    - The **multi-step input-output relationship** is then proved by **induction** with the single-step-update property.

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Case Studies

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Example 2: A Greatest-Common-Divisor (GCD) Circuit

Example 3: Hierarchical Reasoning

Example 4: Complex Links

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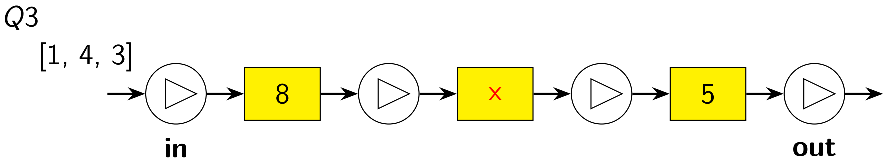

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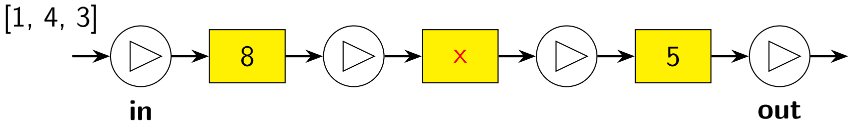

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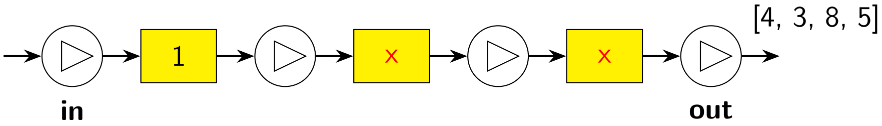

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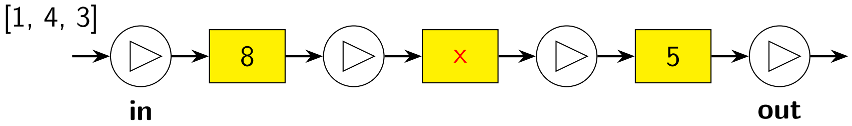

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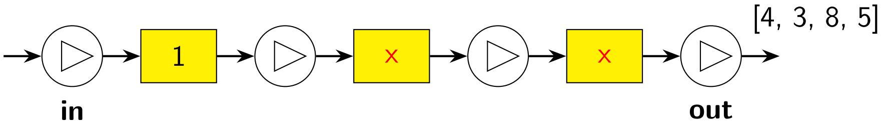

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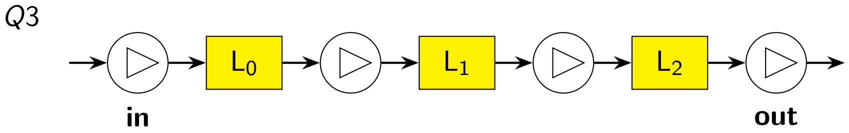

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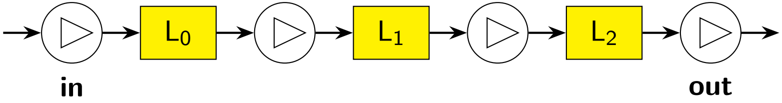

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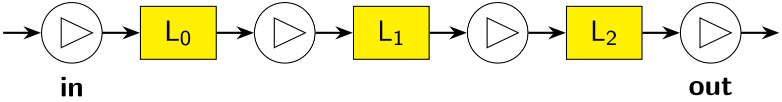

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$Q3$ accepts a new data item each time the in-act signal fires. We define in-seq, the **accepted input sequence**, as the sequence of data items that have passed joint **in**.

Similarly, we define out-seq, the **valid output sequence**, as the sequence of data items that have passed through joint **out** while out-act fires.

Example 1: A FIFO Circuit

The relationship between $Q3$'s in-seq and out-seq.

$$q3\$extract(q3\$run(input\text{-}list, st, n)) ++ out\text{-}seq = in\text{-}seq ++ q3\$extract(st)$$

```
$q3\$run(input\text{-}list, st, n) :=$
  if $(n \leq 0)$ $st$
  else
    $q3\$run(tail(input\text{-}list),$
            $q3\$step(head(input\text{-}list), st),$ // Return the next state of Q3
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The extraction function ***q3$extract(st)*** extracts valid data from state ***st*** of $Q3$, i.e., extracts data from links that are **full** at state ***st***.

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out-seq = *in-seq* when the initial and final states contain no valid data.

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Our ACL2 proof of (1) uses **induction** and the following single-step-update property of $Q3$ as a supporting lemma,

$$q3\$extract(q3\$step(input, st)) = q3\$extracted\text{-}step(input, st) \tag{2}$$

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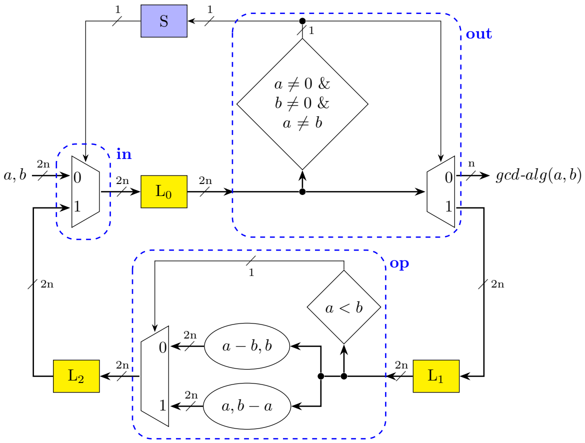
where $q3\$extracted\text{-}step(input, st) :=$

$$\begin{cases} q3\$extract(st), \textbf{if } in\text{-}act = nil \wedge out\text{-}act = nil \\ [input.data] ++ q3\$extract(st), \textbf{if } in\text{-}act = t \wedge out\text{-}act = nil \\ remove\text{-}last(q3\$extract(st)), \textbf{if } in\text{-}act = nil \wedge out\text{-}act = t \\ [input.data] ++ remove\text{-}last(q3\$extract(st)), \textbf{otherwise} \end{cases}$$

Example 2: A Greatest-Common-Divisor (GCD) Circuit



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gcd-alg(a, b) :=
while (a ≠ 0) ∧ (b ≠ 0) ∧ (a ≠ b) do
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return
    if (a = 0) then b else a
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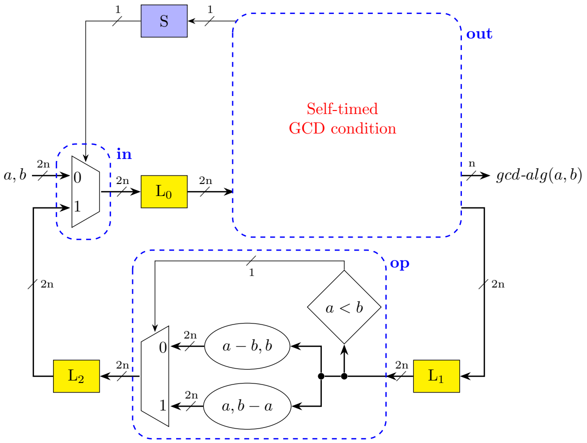

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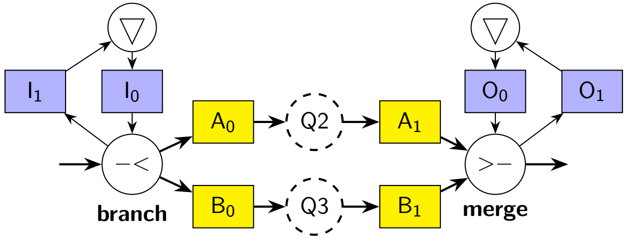

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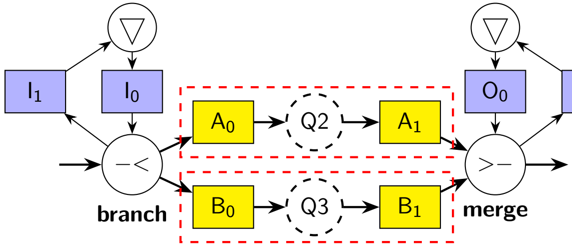
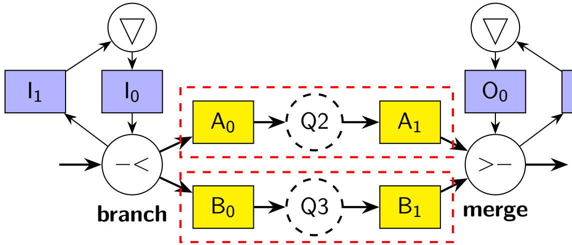
RR



Abstracting two queues ($A_0 \rightarrow Q2 \rightarrow A_1$) and ($B_0 \rightarrow Q3 \rightarrow B_1$) as two complex links makes reasoning more efficient by reducing case splits in proving the invariant as well as the single-step-update property for *RR*.

Example 4: Complex Links

RR



Abstracting two queues ($A_0 \rightarrow Q2 \rightarrow A_1$) and ($B_0 \rightarrow Q3 \rightarrow B_1$) as two complex links makes reasoning more efficient by reducing case splits in proving the invariant as well as the single-step-update property for *RR*.

The verification time of *RR* is reduced from more than 23.5 minutes to 14 seconds by using the complex links.

Outline

1 The DE System

2 Modeling and Verification Approach

3 Case Studies

4 Conclusions

Conclusions

We have presented a framework for formally modeling and verifying self-timed circuit designs using the DE system.

We have developed a hierarchical reasoning method that is capable of verifying the **functional correctness** of self-timed circuit designs at large scale.

This work has also provided a library for analyzing self-timed systems in ACL2.

We model self-timed systems as networks of links communicating with each other locally via joints, using the link-joint model.

We model the **non-determinism of event-ordering** in self-timed circuits by associating each joint with an external go signal that, when disabled, prevents a joint from **firing**.

Timeline

- **Spring 2018 – Fall 2018:** Enhance automation of our framework.
- **Spring 2018 – Summer 2018:** Verify self-timed circuit models that include FCFS arbitrated merge operations.
- **Fall 2018:** Verify a self-timed serial adder model using our new approach.
- **Fall 2018:** Demonstrate compositionality by proving that the functionality of *gcd* is preserved when replacing its combinational ripple-carry-adder sub-circuit with a functionally-equivalent, self-timed serial adder.
- **Spring 2019:** Dissertation writing and final defense.

Publications

Cuong Chau, Warren A. Hunt Jr., Matt Kaufmann, Marly Roncken, and Ivan Sutherland
Data-Loop-Free Self-Timed Circuit Verification
In the 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2018. To appear.

Marly Roncken, Ivan Sutherland, Chris Chen, Yong Hei, Warren Hunt Jr., and **Cuong Chau**, with Swetha Mettala Gilla, Hoon Park, Xiaoyu Song, Anping He, and Hong Chen
How to Think about Self-Timed Systems
In the IEEE Asilomar Conference on Signals, Systems, and Computers, 2017. To appear.

Cuong Chau, Warren A. Hunt Jr., Marly Roncken, and Ivan Sutherland
A Framework for Asynchronous Circuit Modeling and Verification in ACL2
In the 13th Haifa Verification Conference (HVC), 2017, pp. 3-18.

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Computer-Aided Reasoning: ACL2 Case Studies, Kluwer Academic Publishers Norwell, MA, USA, 151 – 166.

M. Roncken, S. Gilla, H. Park, N. Jamadagni, C. Cowan, I. Sutherland (2015)
Naturalized Communication and Testing
ASYNC 2015, 77 – 84.

M. Roncken, I. Sutherland, C. Chen, Y. Hei, W. Hunt Jr., C. Chau, S. M. Gilla, H. Park, X. Song, A. He, and H. Chen (2017)
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Asilomar 2017, to appear.

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MEMOCODE 2011, 89 – 97.

Questions?