A Framework for Asynchronous Circuit Modeling and Verification in ACL2

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Outline

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Introduction

Synchronous circuits (or clock-driven circuits): changes in the state of storage elements are synchronized by **a global clock signal**.

Asynchronous circuits (or self-timed circuits): there is no global clock signal distributed in asynchronous circuits. The communication between state-holding elements is performed via **local communication protocols**.

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Why asynchronous?

- Low power consumption,
- High operating speed,
- Low electromagnetic interference,
- Better composability and modularity in large systems,
- ...

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- We use the DE system [Hunt:2000], which is built in ACL2, to specify and verify self-timed circuit designs.
- Developing a hierarchical verification approach to support scalability.
- Exploring strategies for reasoning with non-deterministic circuit behavior.

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- These lemmas are used to prove the correctness of yet larger modules containing these submodules, **without the need to dig into any details about the submodules**.

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- These lemmas are used to prove the correctness of yet larger modules containing these submodules, **without the need to dig into any details about the submodules**.
- This approach has been demonstrated its **scalability** to large systems, as shown on contemporary x86 designs at Centaur Technology [Slobodova et al.:2011].

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- Local communication protocols
- Non-deterministic behavior due to variable delays in wires and gates

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  $\Rightarrow$ Employing an oracle, which we call a collection of go signals.

The Link-Joint Model

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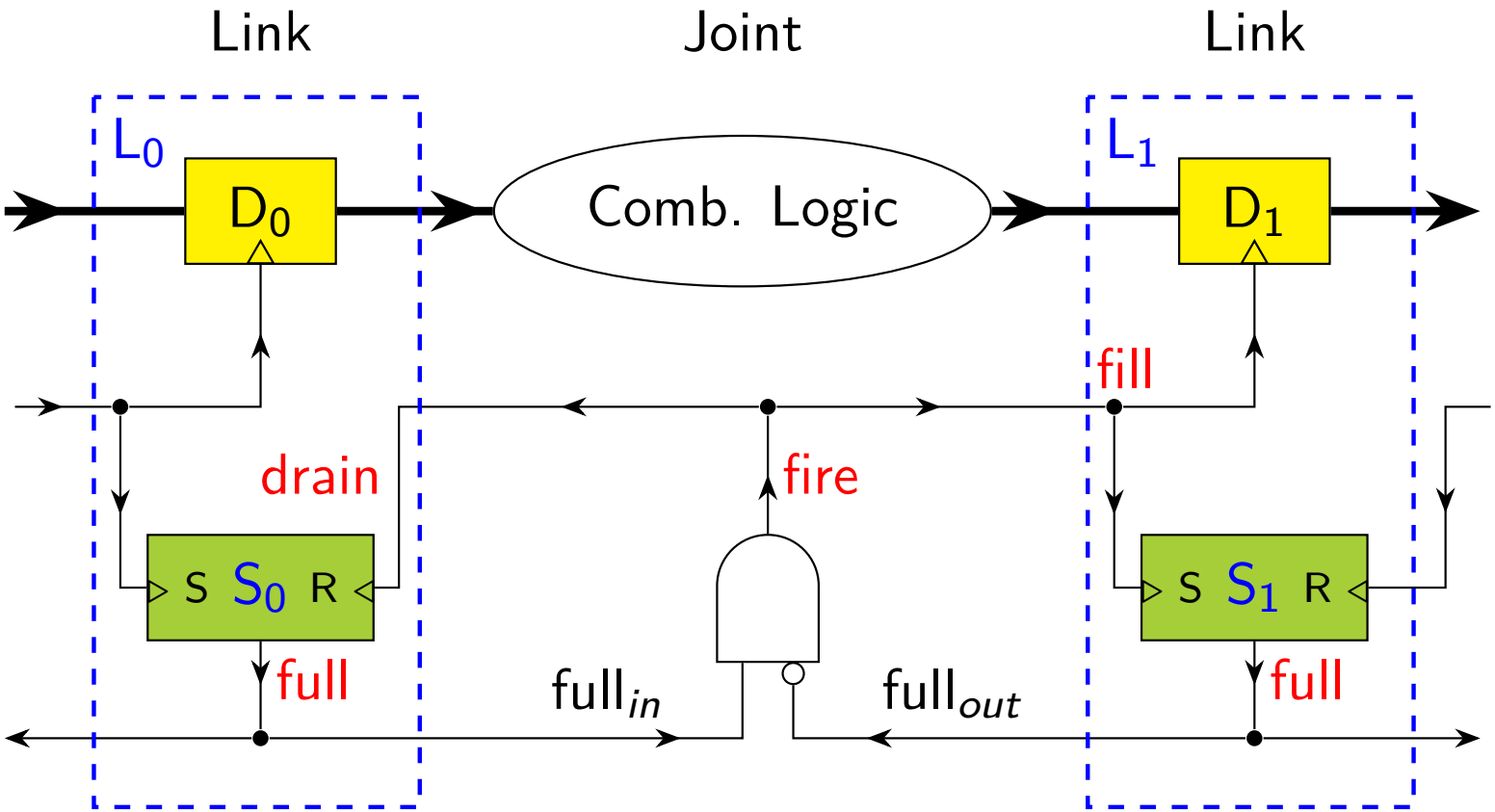
Joints are the meeting points for links to **coordinate states** and **exchange data**.

The Link-Joint Model



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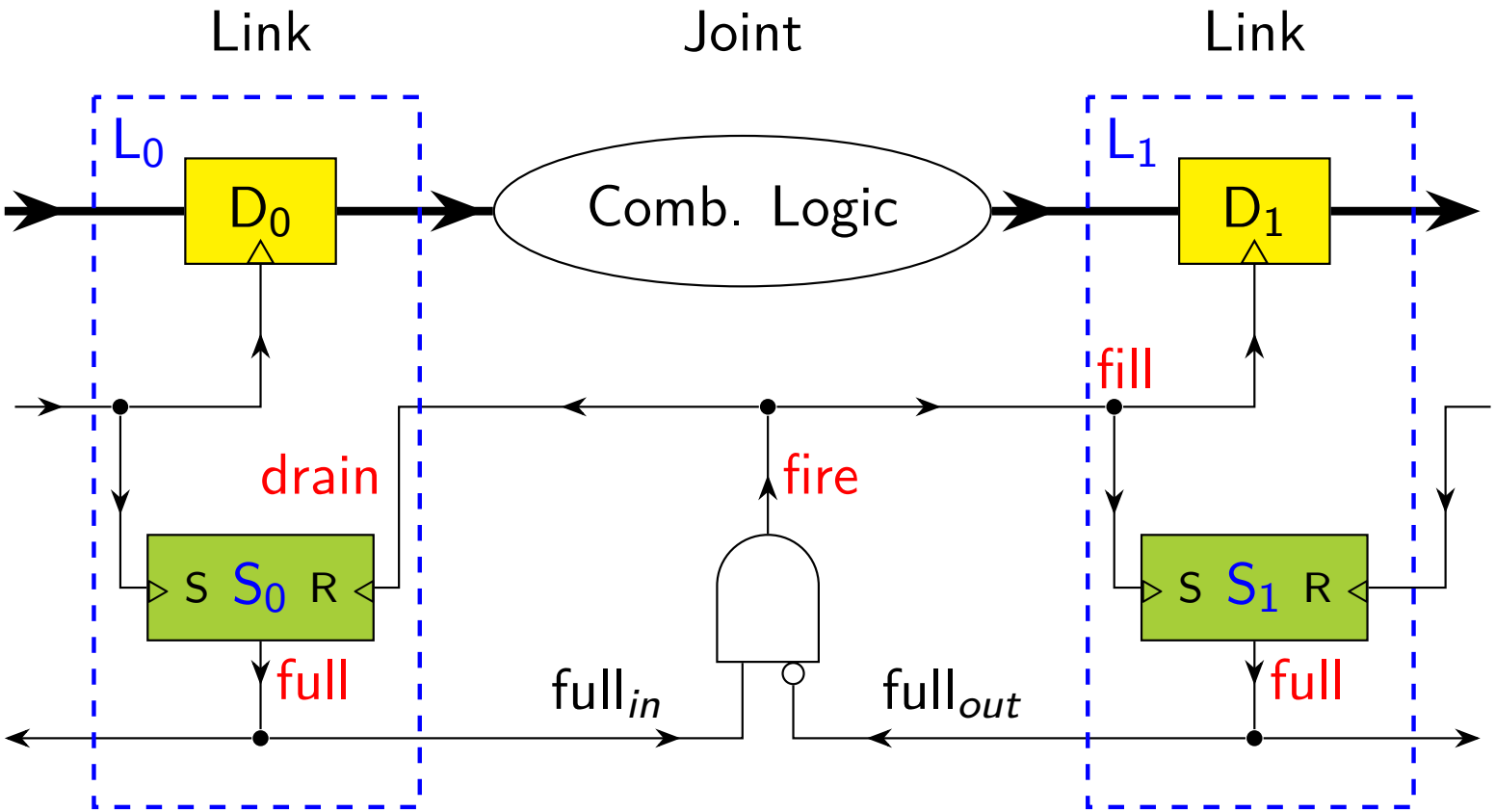

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Necessary conditions for a joint to fire: all of its incoming links are **full** and all of its outgoing links are **empty**.

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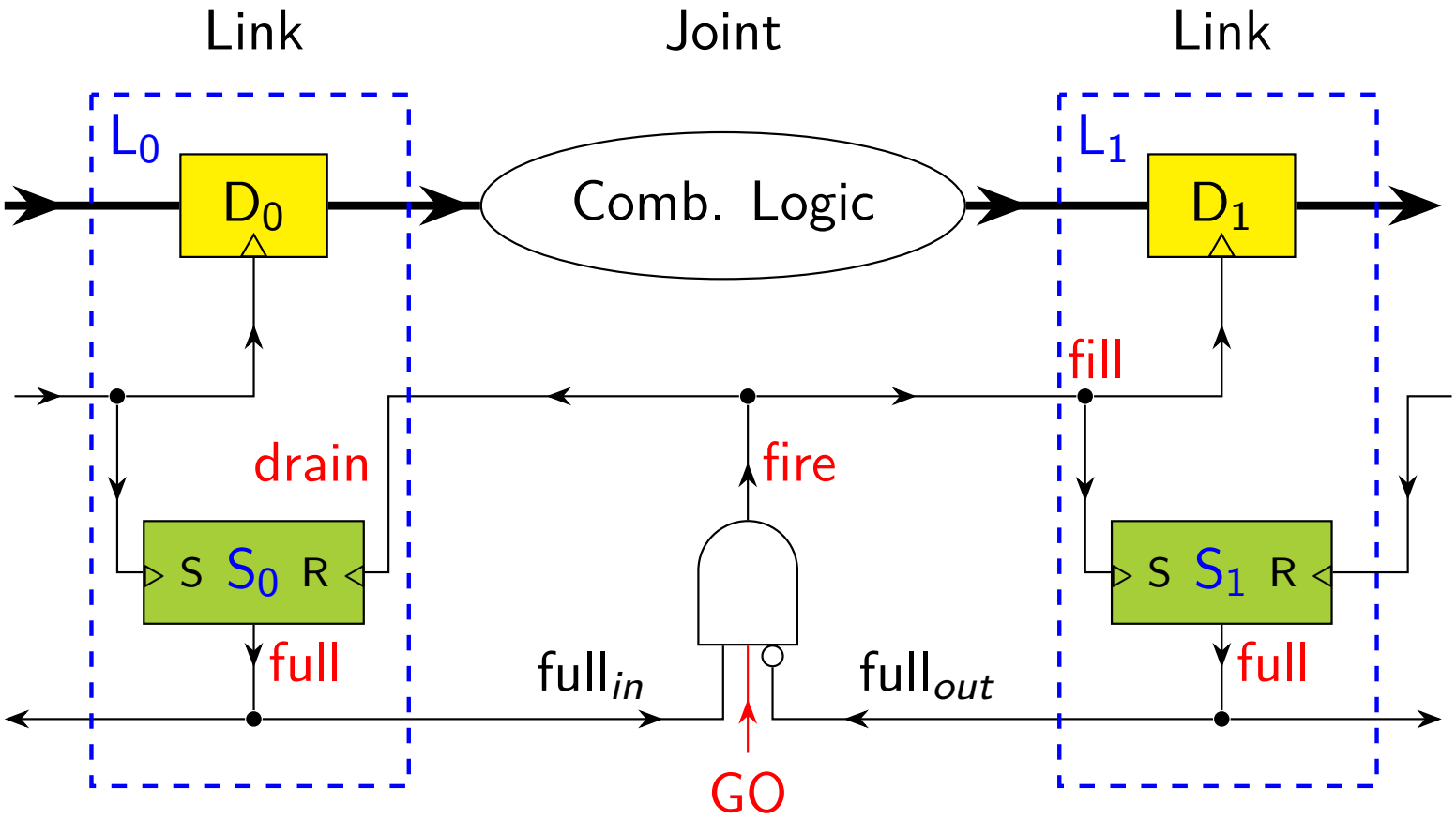

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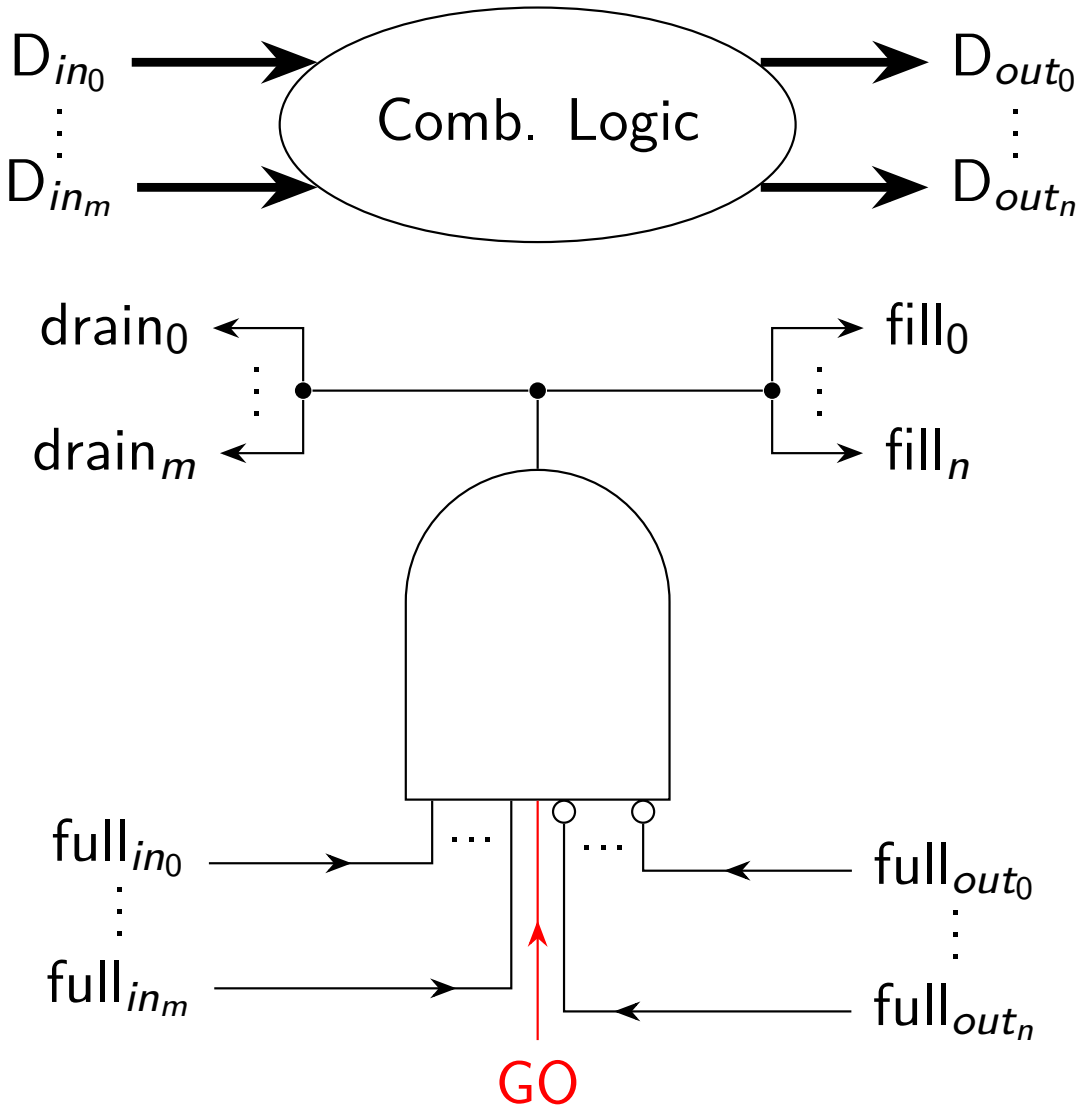
When a joint fires, the following three actions will be executed in parallel:

- transfer data computed from the incoming links to the outgoing links,
- fill the outgoing links, make them **full**,
- drain the incoming links, make them **empty**,

The Link-Joint Model



Verification

Our framework applies a hierarchical verification approach to formalizing single transitions of circuit behavior (simulated by `se` and `de` functions).

- The output and next state of a module are formalized using the formalized outputs and next states of submodules, without delving into details about the submodules.

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- Computing invariance properties in self-timed systems becomes much more complicated than in synchronous systems.

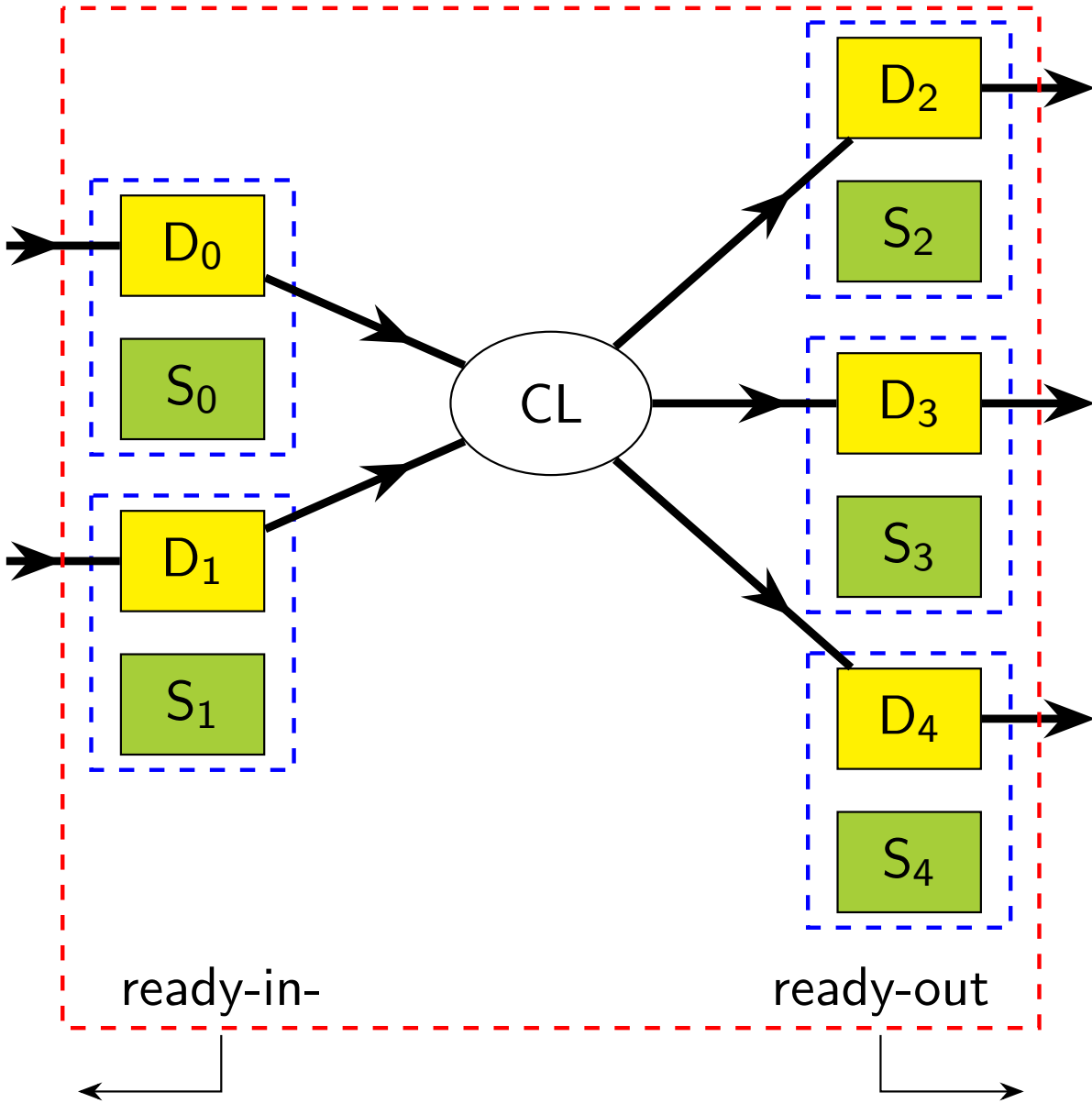
We impose design restrictions to reduce non-determinism, and consequently reduce the complexity of the set of execution paths:

- These restrictions enable our framework to verify loop invariants efficiently via **induction** and subsequently verify the functional correctness of self-timed circuit designs.

Self-Timed Modules

Self-timed modules can be treated either as links or joints.

Our framework currently treats modules as "complex" links.



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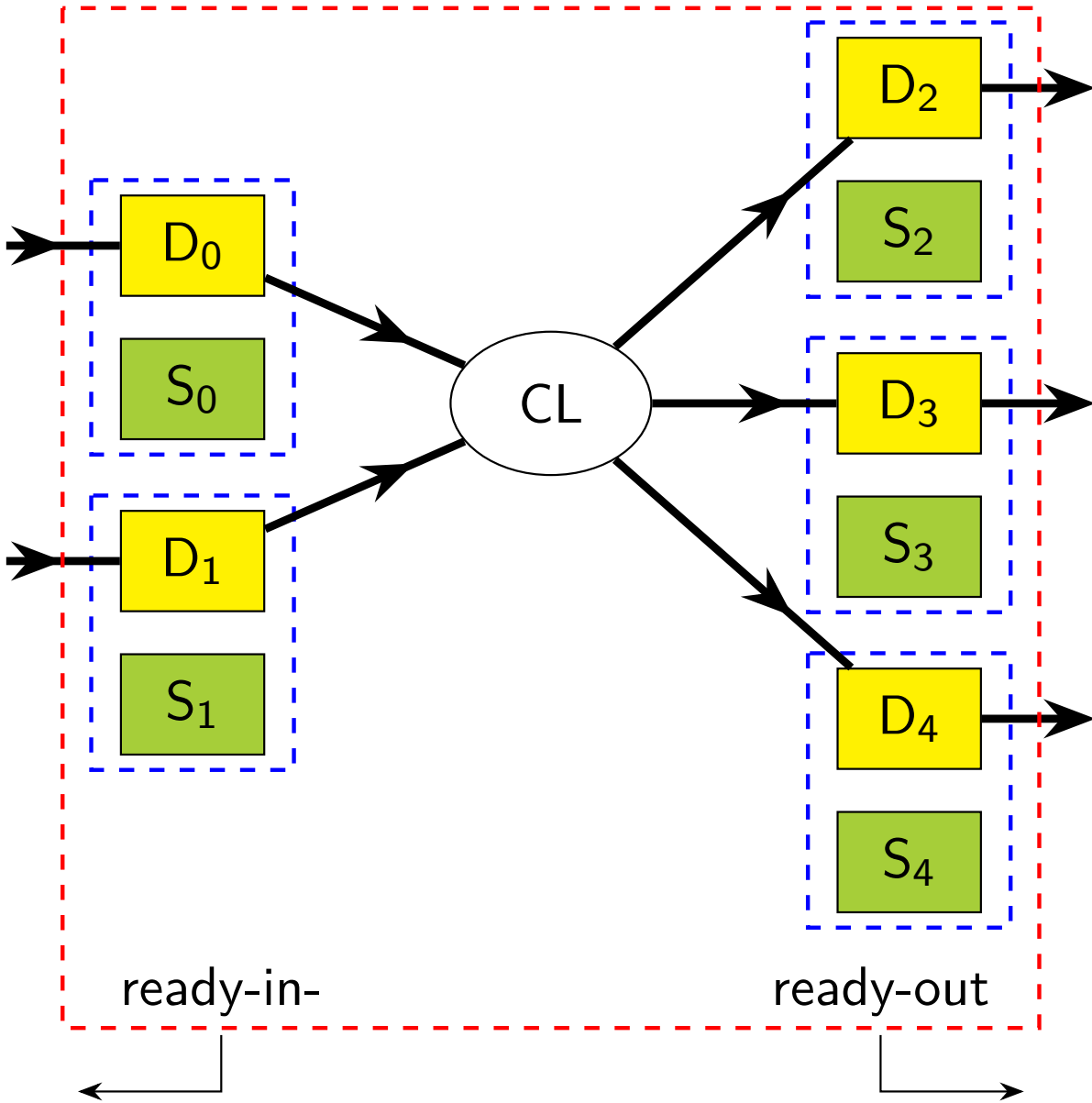
$\Rightarrow$ Self-timed modules also report both **data** and **communication states** to the joints connecting them.



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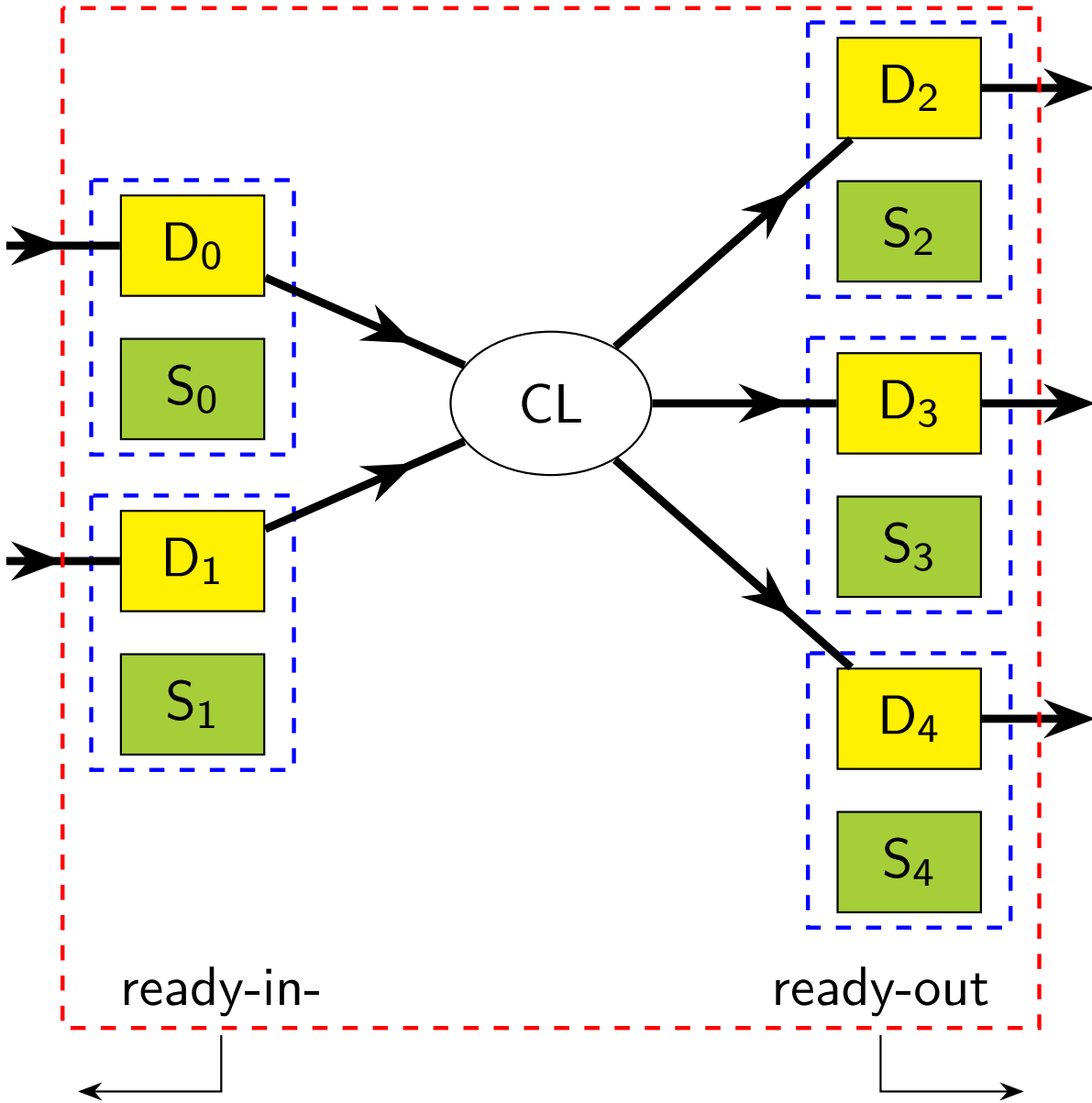
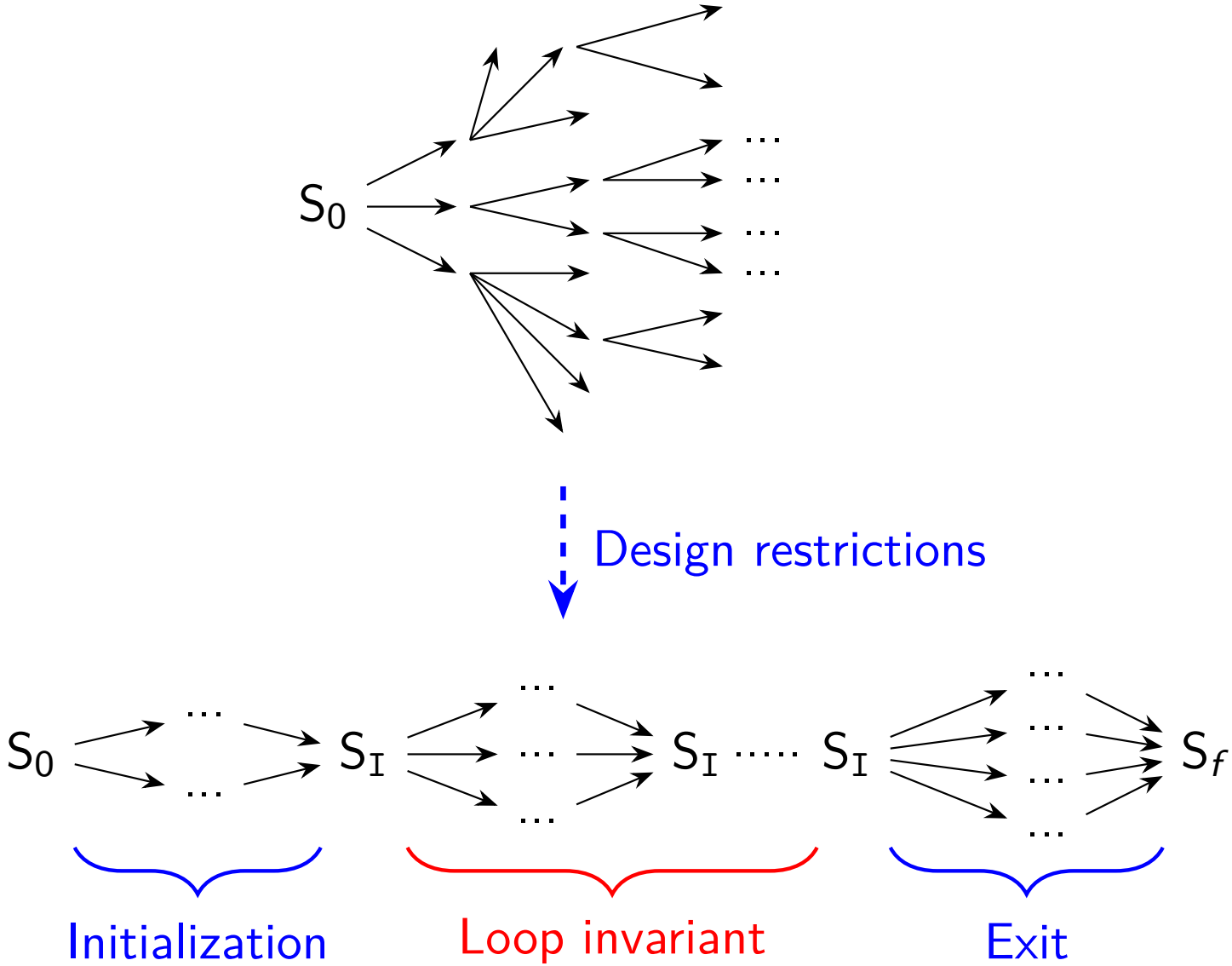
We plan to explore a notion of modules being treated as "complex" joints in the future.



Design Restrictions

Design restrictions: A module is ready to communicate with other modules only when it finishes all of its internal operations and becomes quiescent.

State Space Reduction



S_0: initial state, S_I: invariant state, S_f: final state

Outline

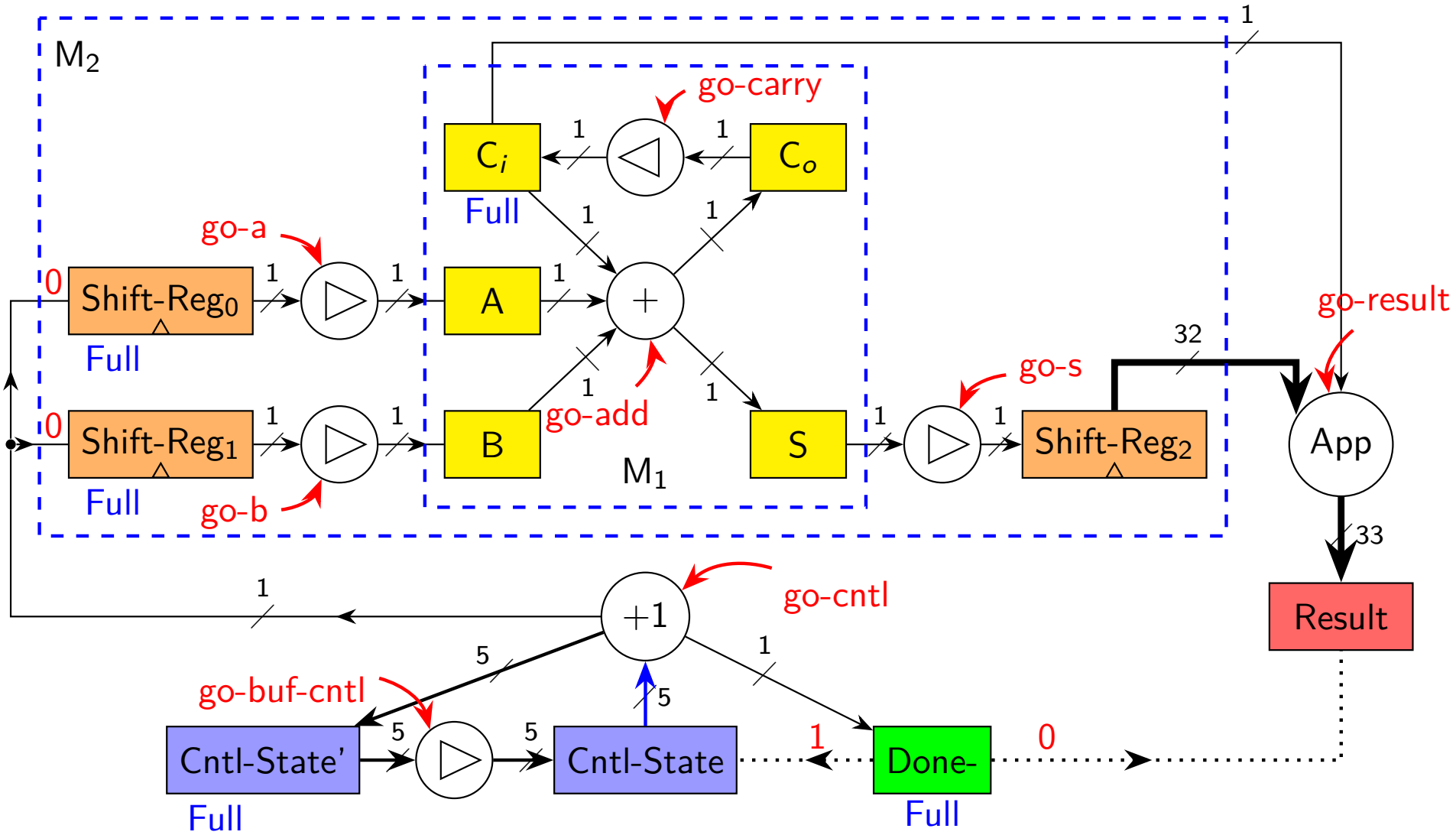
32-Bit Self-Timed Serial Adder Verification

We demonstrate our framework by modeling and verifying the functional correctness of a 32-bit self-timed serial adder.

We prove that the self-timed serial adder indeed performs the addition under an appropriate initial condition.

- When the adder finishes its execution, the result is proven to be the sum of the two 32-bit input operands and the carry-in.

Data Flow of a 32-Bit Self-Timed Serial Adder



Correctness Theorems

Theorem 1 (Partial correctness).

$$
\begin{aligned}
& async\_serial\_adder(netlist) \wedge && (1)\\
& init\_state(st) \wedge && (2)\\
& (operand\_size = 32) \wedge && (3)\\
& interleavings\_spec(input\_seq, operand\_size) \wedge && (4)\\
& (st' = run(netlist, input\_seq, st, n)) \wedge && (5)\\
& full(result\_status(st')) && (6)\\
\Rightarrow\ & (result\_value(st') = shift\_reg\_0\_value(st) + \\
& \qquad shift\_reg\_1\_value(st) + \\
& \qquad ci\_value(st))
\end{aligned}
$$

Correctness Theorems

Theorem 2 (Termination).

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& (\mathit{operand\_size} = 32) \wedge && (3)\\
& \mathit{interleavings\_spec}(\mathit{input\_seq}, \mathit{operand\_size}) \wedge && (4)\\
& (\mathit{st}' = \mathit{run}(\mathit{netlist}, \mathit{input\_seq}, \mathit{st}, n)) \wedge && (5)\\
& (n \geq \mathit{num\_steps}(\mathit{input\_seq}, \mathit{operand\_size})) && (6')\\
\Rightarrow\ & \mathit{full}(\mathit{result\_status}(\mathit{st}')) &&
\end{aligned}
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Future Work

We plan to prove the partial correctness of the self-timed serial adder without specifying the interleavings of the go signals' values. In other words, we aim to remove **Hypothesis 4** from Theorem 1.

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We intend to follow a **hierarchical approach** to prove module-level properties of the following form:

- Given an initial state of the module, the module's **final state** meets its specification after that module completes execution.

Conclusions

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Our verification framework is able to establish loop invariants using induction when the circuit behavior obeys the design restrictions we propose.

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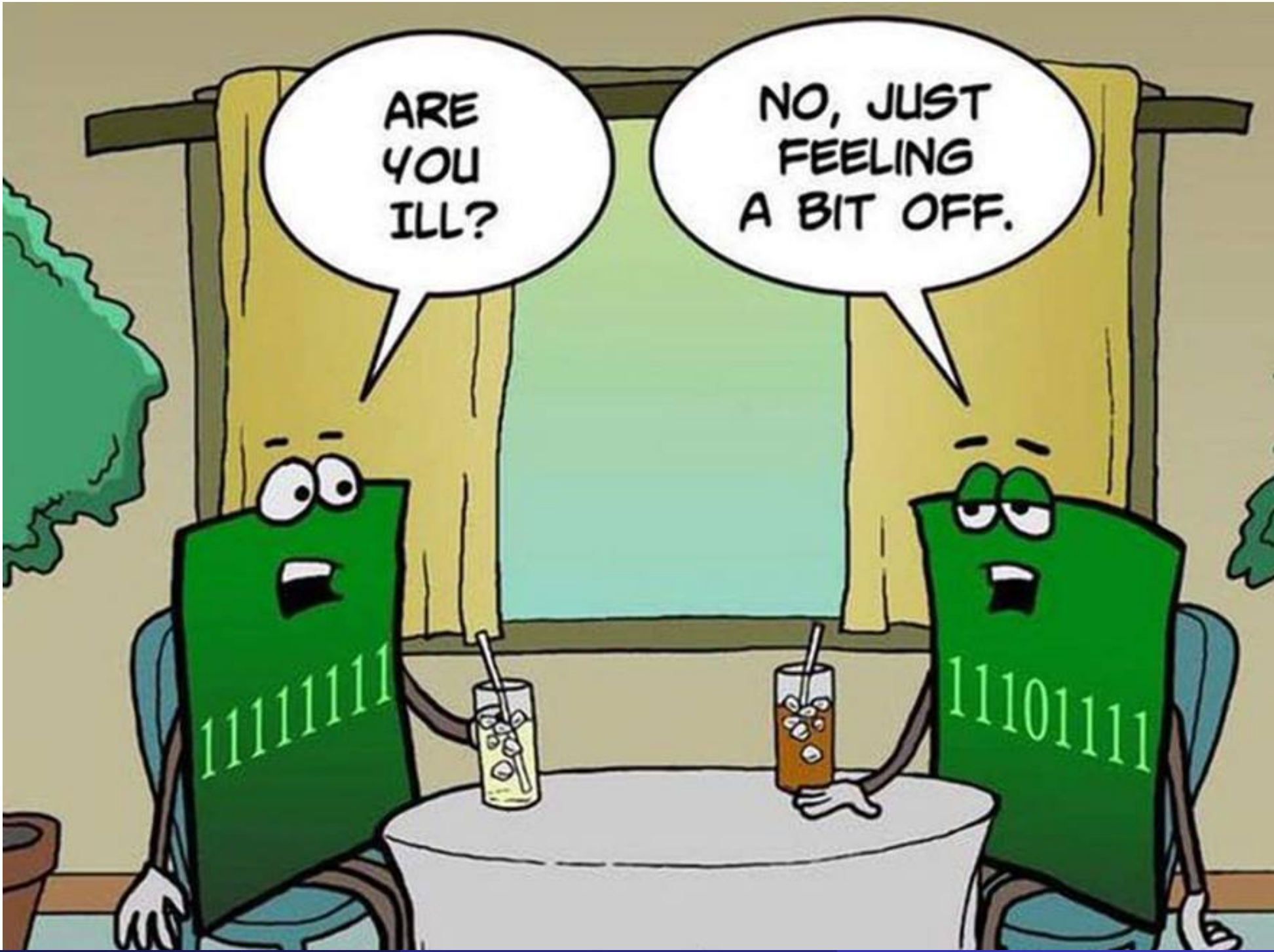
ARE YOU ILL?
NO, JUST FEELING A BIT OFF.
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Questions?