cs378: Concurrency Honors: FPGA Needleman-Wunsch Lab 5 Writeup Template

You
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1 Graphs

1.1 CPU

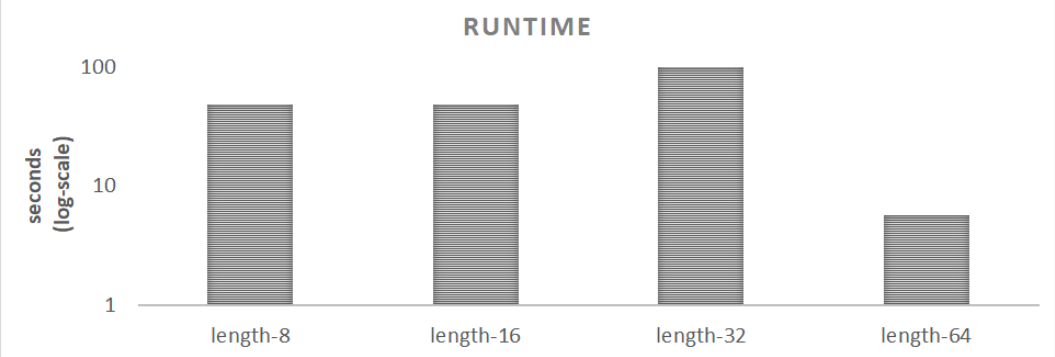

Figure 1: Runtime of CPU NW implementation on inputs of length 8,16,32,64. *NOTE: the data in this graph are random. If your data are different that's GOOD.*

A graph showing the runtime on inputs of length 8,16,32,64 using your sequential CPU solution is given in Figure 1.

1.2 Cascade in Software Run Time

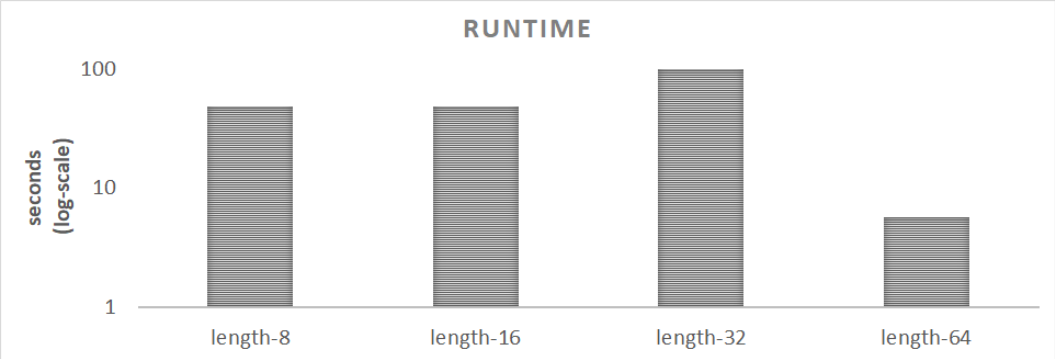

Figure 2: Runtime of Verilog implementation running in Cascade software mode on inputs of length 8,16,32,64. *NOTE: the data in this graph are random. If your data are different that's GOOD.*

A graph showing the runtime on inputs of length 8,16,32,64 using cascade running in software emulation only mode is given in Figure 2.

1.3 Cascade in Hardware Run Time

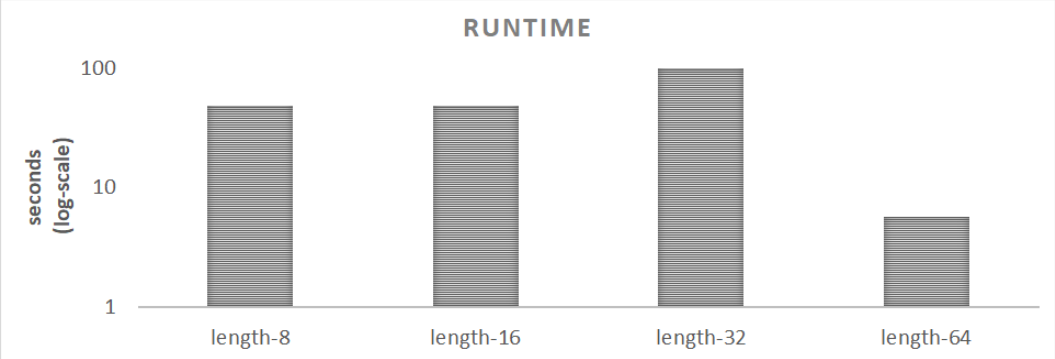

Figure 3: Runtime of Verilog implementation running in Cascade software mode on inputs of length 8,16,32,64. *NOTE: the data in this graph are random. If your data are different that's GOOD.*

A graph showing the runtime on inputs of length 8,16,32,64 using cascade running on the DE10-nano is given in Figure 3.

2 Questions

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- Report the GPU hardware details, CPU hardware details, and OS version on the machine where you did your measurements.
- How do you explain the differences in runtime and scalability between your CPU solution and your Verilog version?

- How do you explain the differences in runtime and scalability between your Verilog version running in software emulation versus on the DE10?
- How much time did you spend on the lab?

3 Extra Credit

Please document any extra credit work you did in detail.