Parallel Architectures

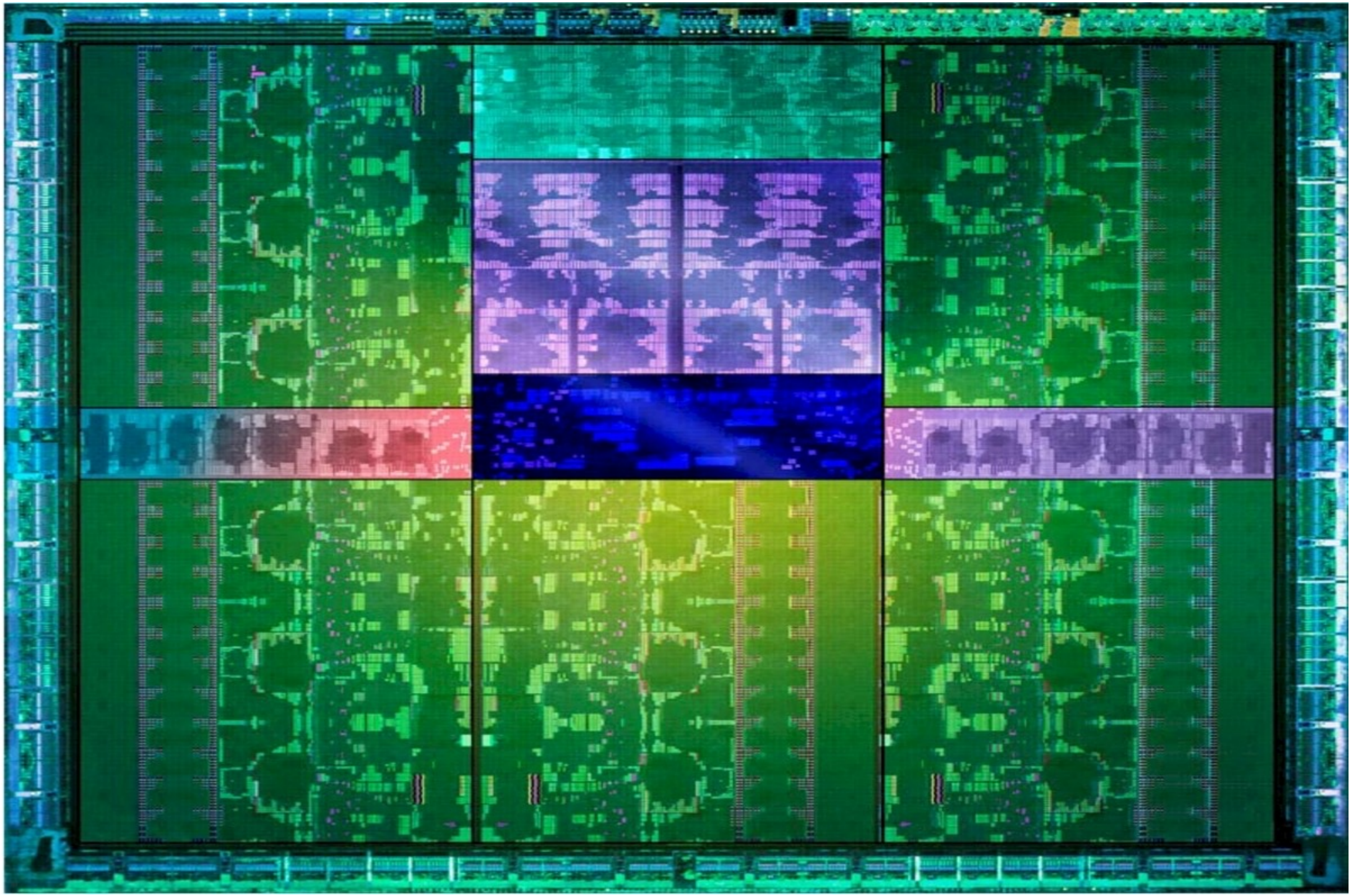
Chris Rossbach

Outline for Today

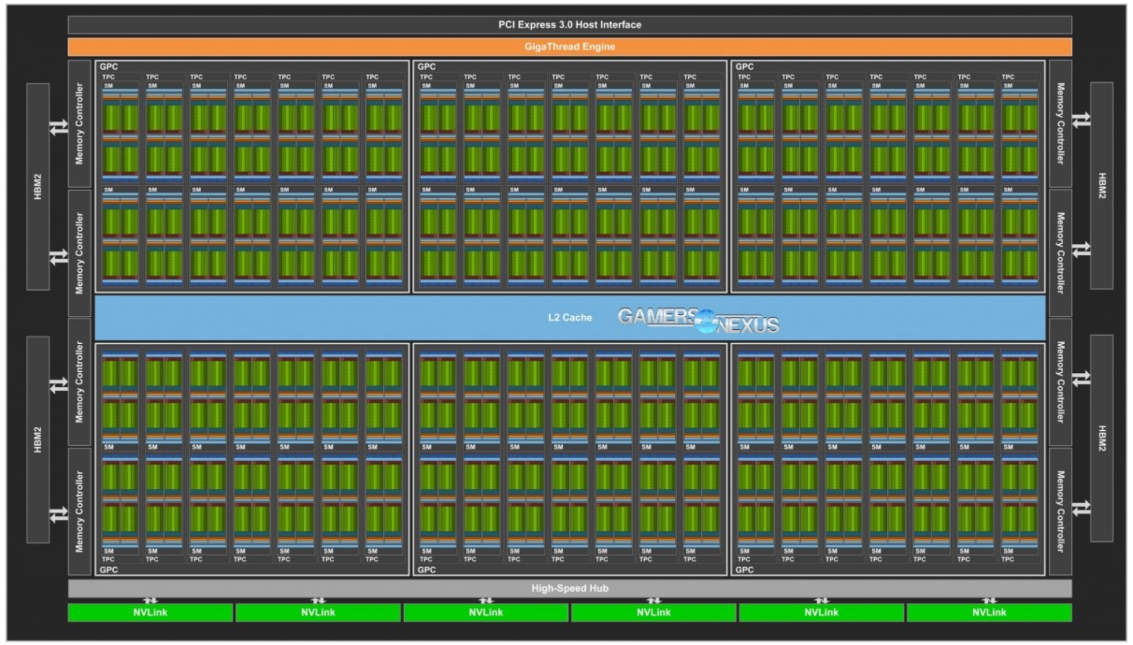
- Questions?
- Administrivia
    - Exam soon
- Agenda
    - Parallel Architectures (GPU background)

Faux Quiz questions

- What is hardware multi-threading; what problem does it solve?
- What is the difference between a vector processor and a scalar?
- Implement a parallel scan or reduction
- How are GPU workloads different from GPGPU workloads?
- How does SIMD differ from SIMT?
- List and describe some pros and cons of vector/SIMD architectures.
- GPUs historically have elided cache coherence.Why? What impact does it have on the the programmer?
- List some ways that GPUs use concurrency but not necessarily parallelism.



A modern GPU: Volta V100



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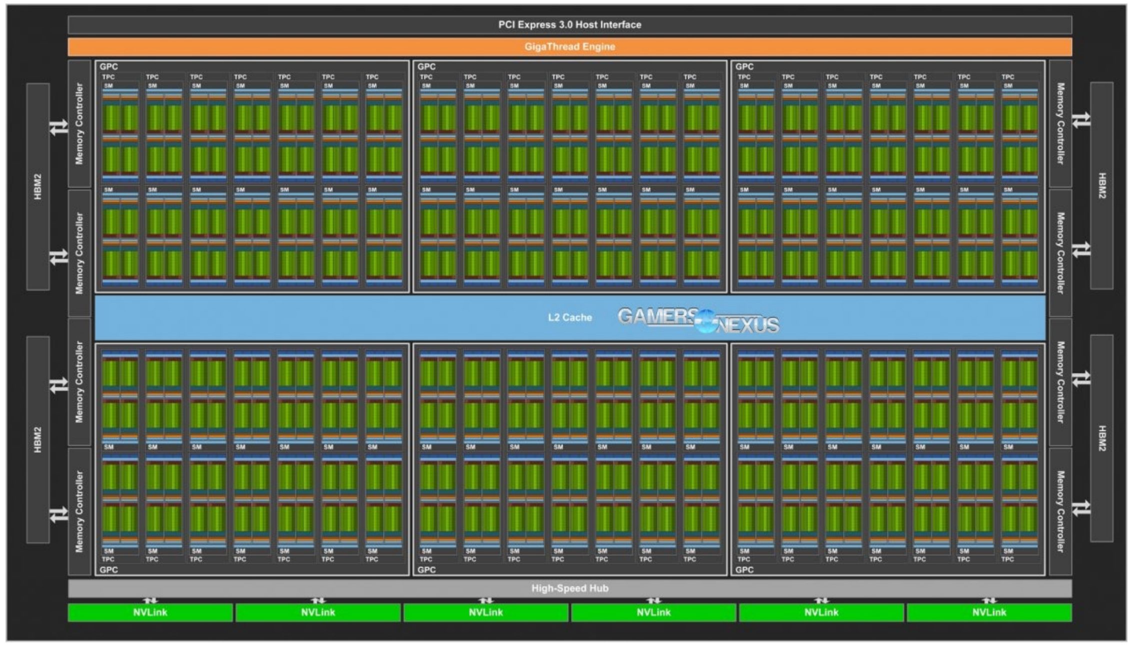

- 80 SMs
  - Streaming Multiprocessor

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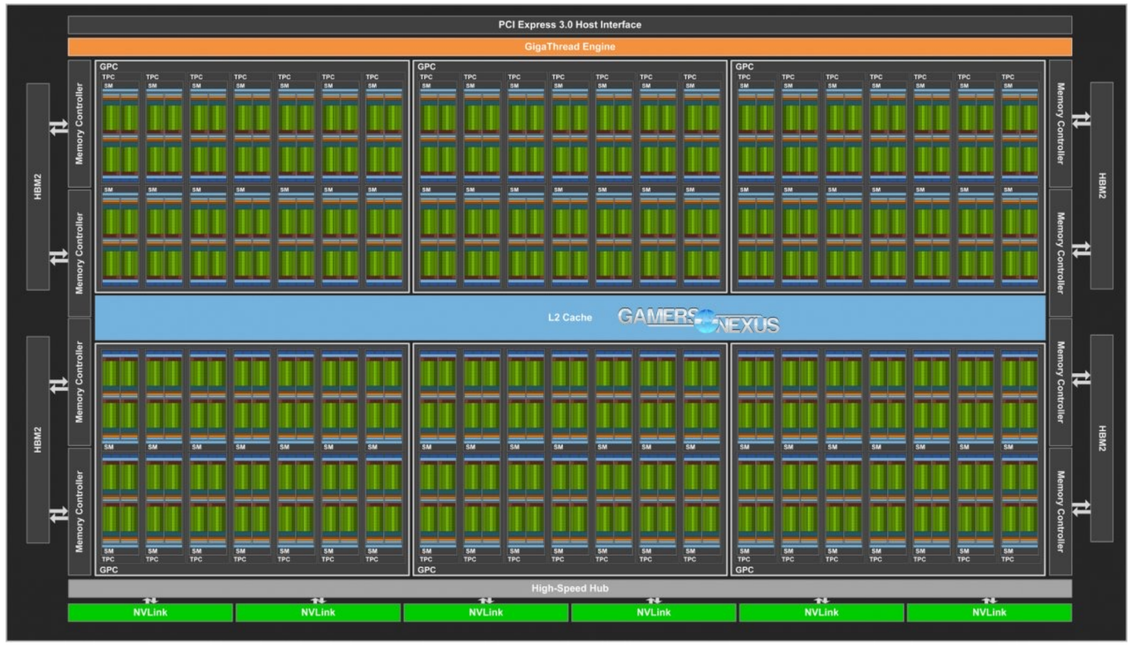

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Also:
CU or *ACE*

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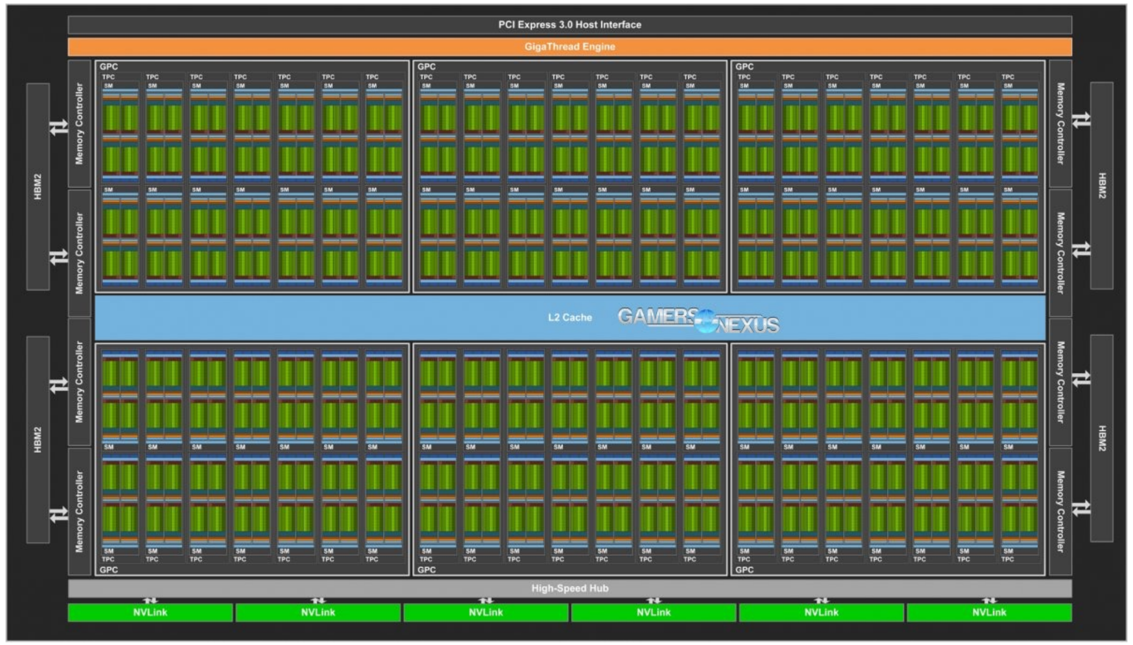

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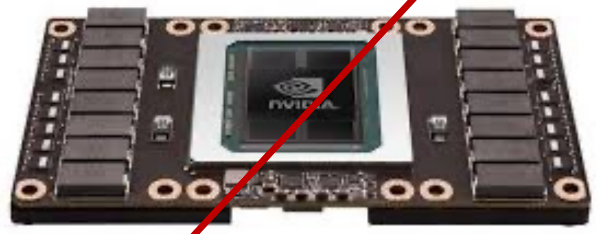

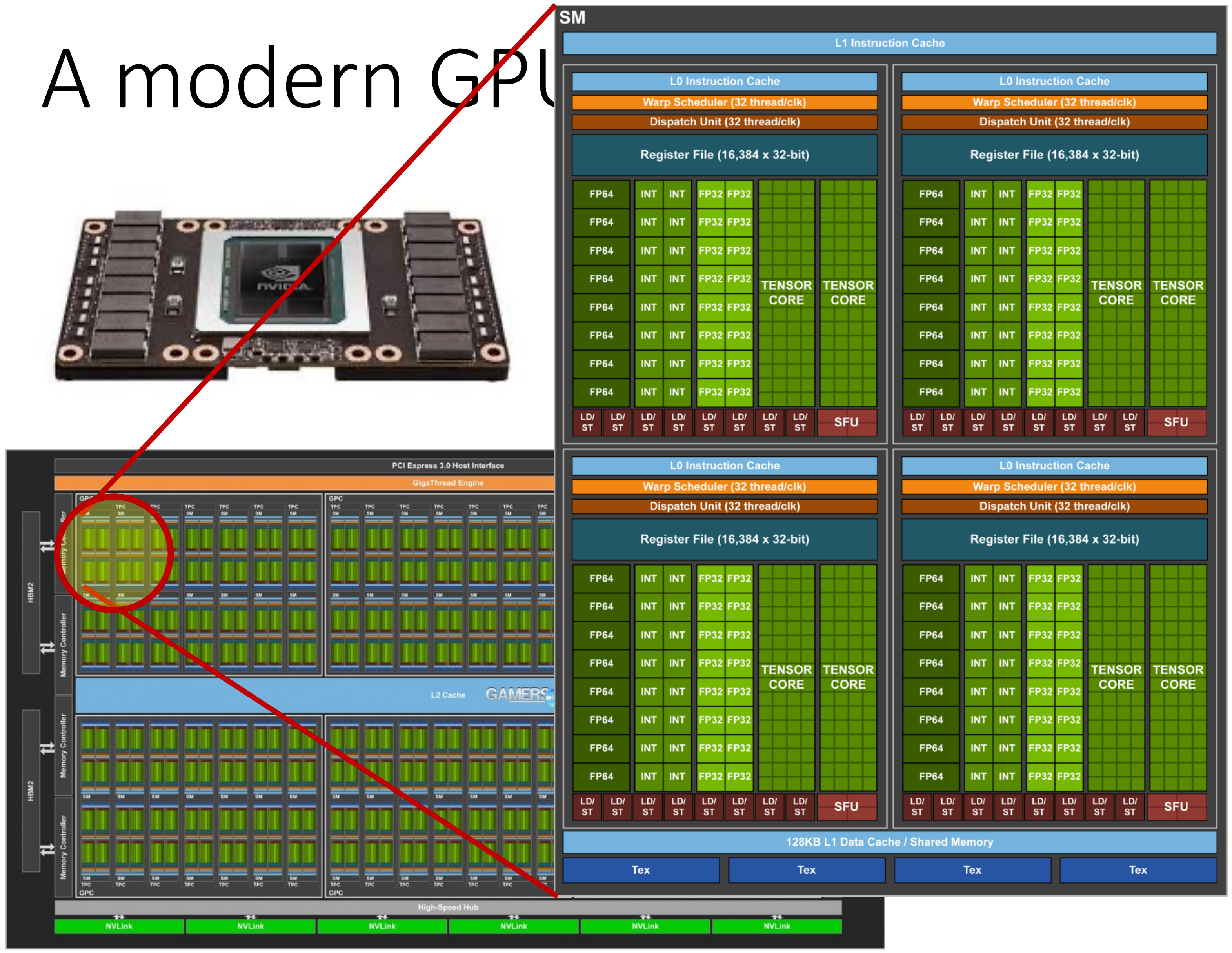
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FP32
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LD/ST
SFU
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  - 5210 threads!
  - 15.7 TFLOPS

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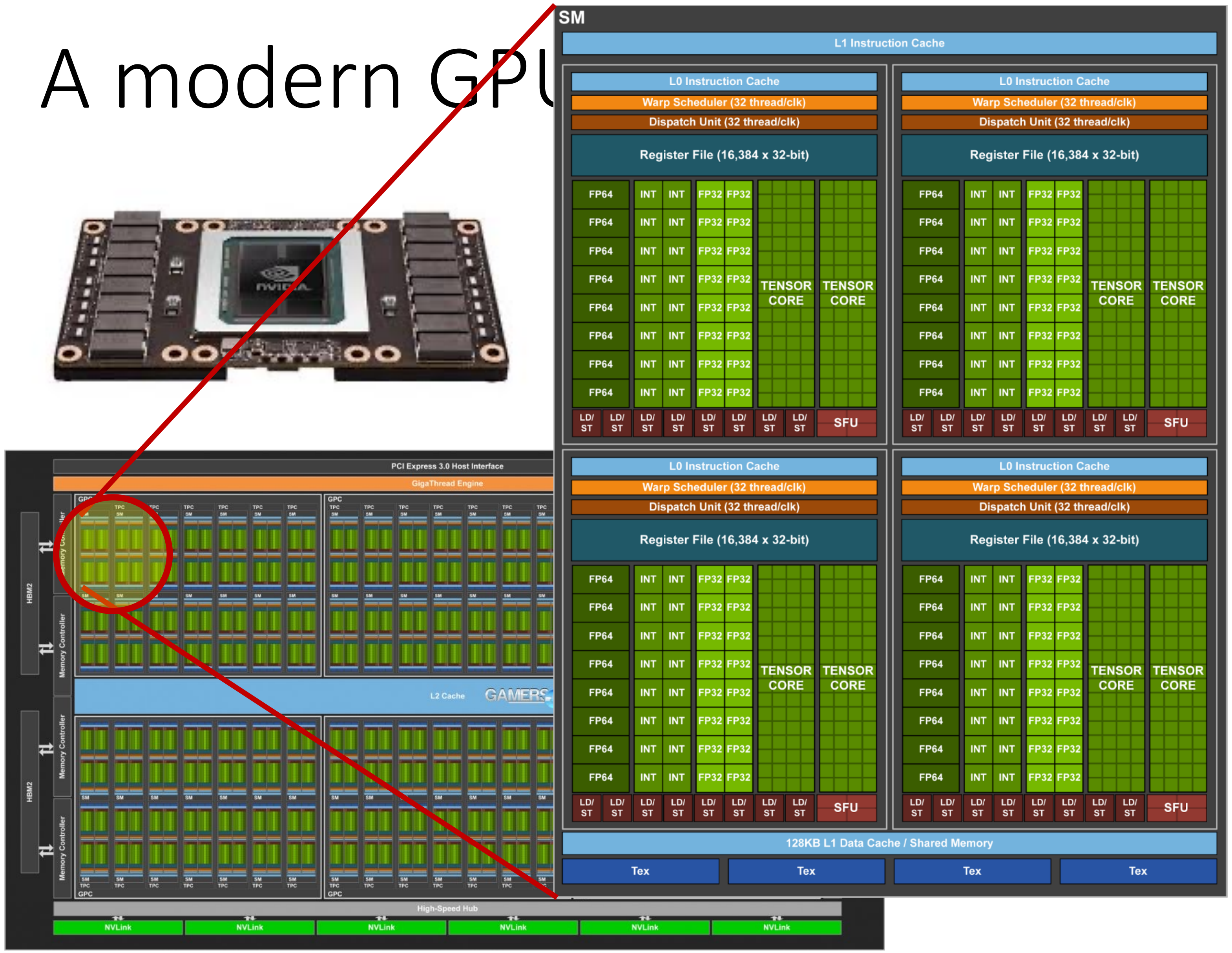
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Roughly: all of pfxsum 1,000s X/sec

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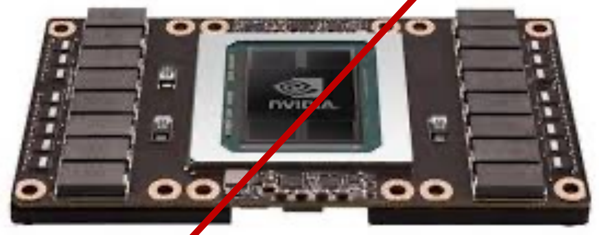

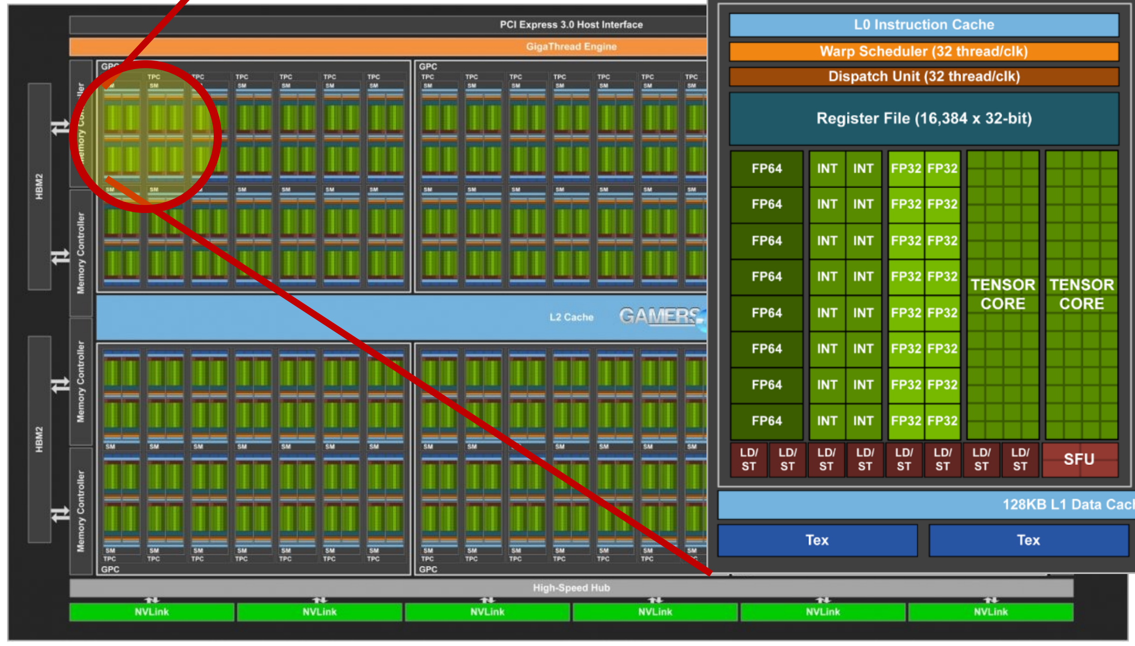

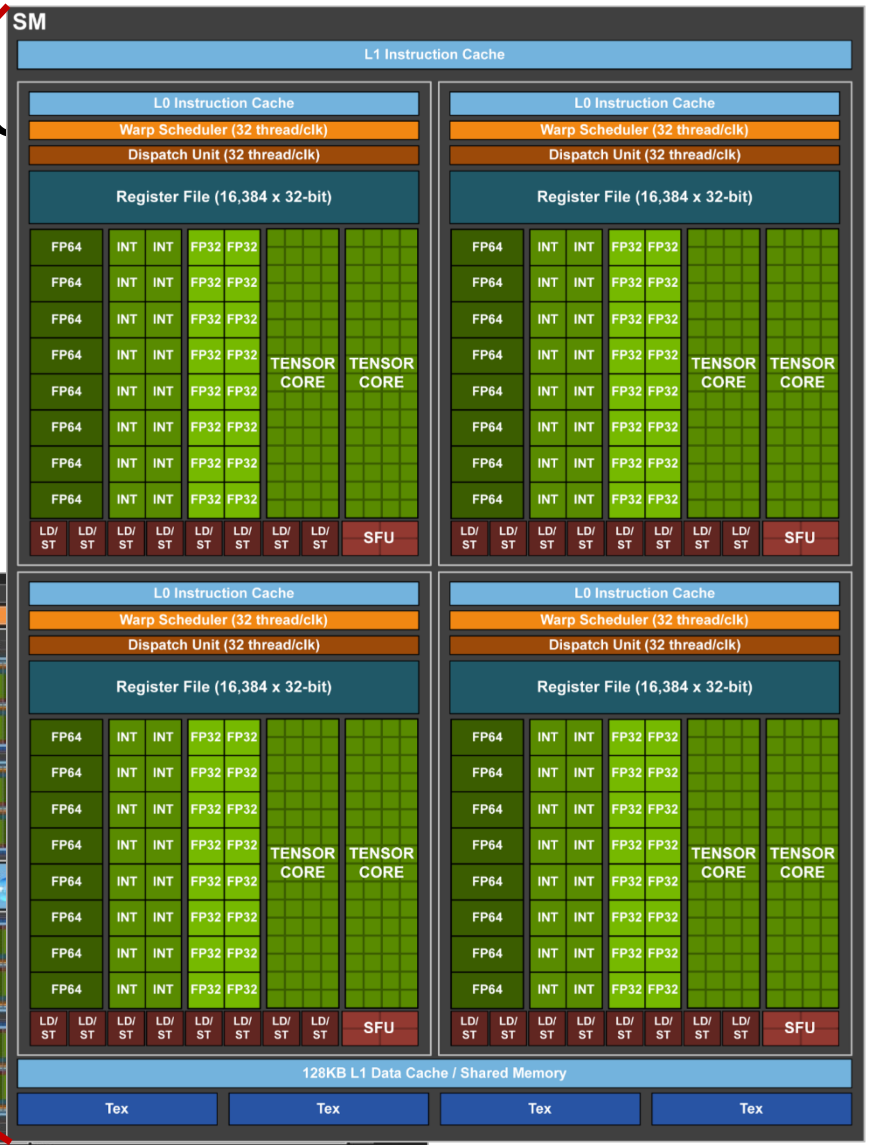
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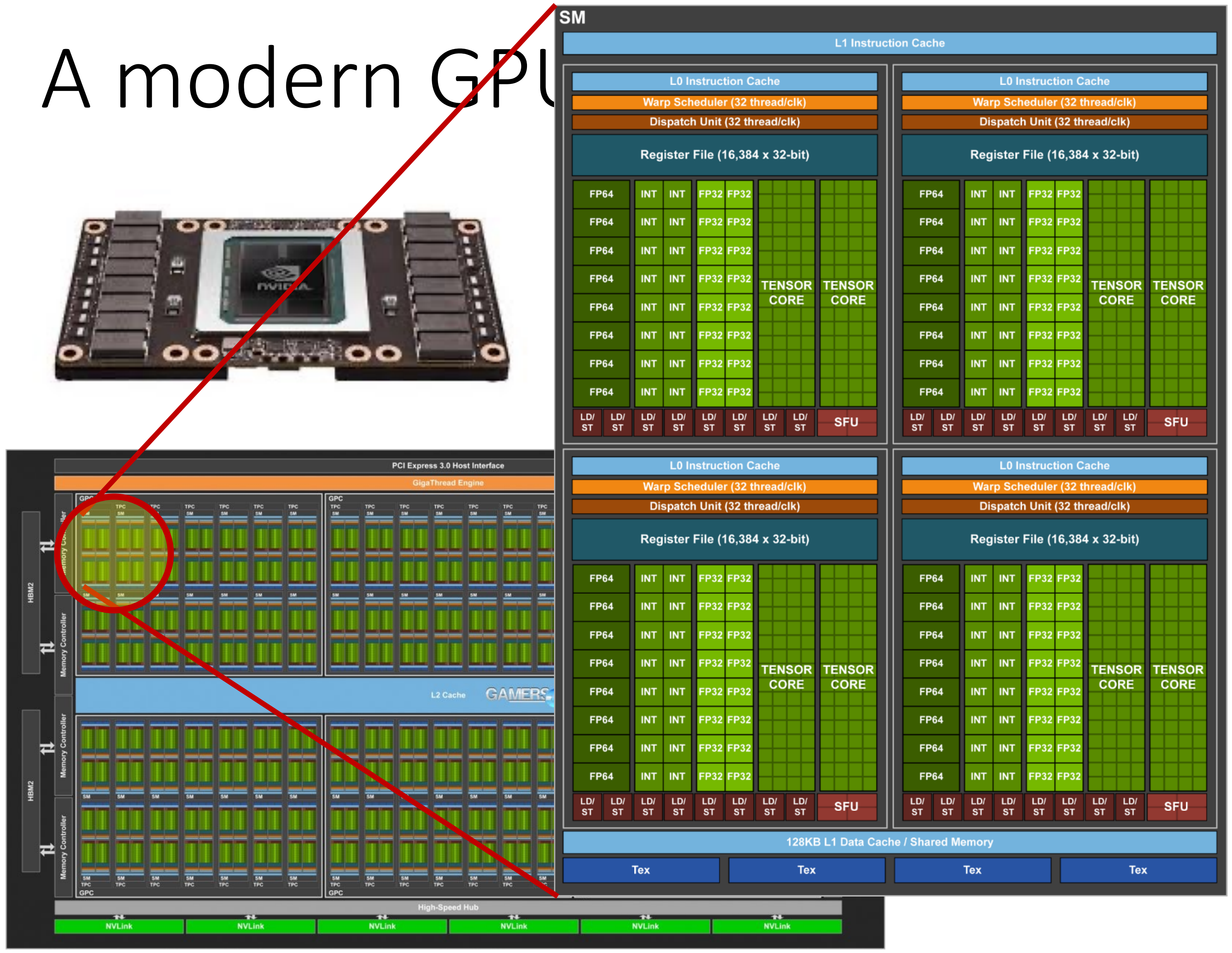

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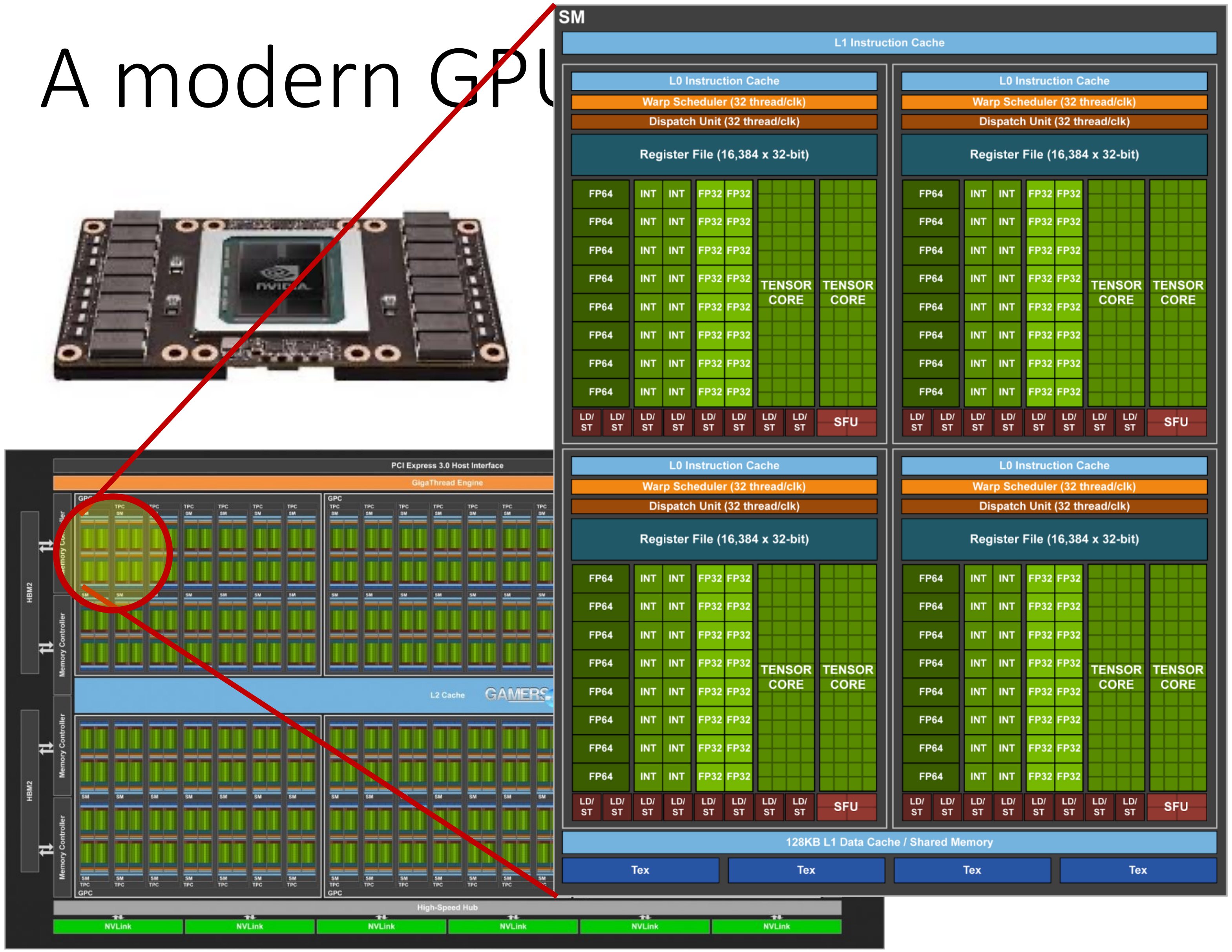
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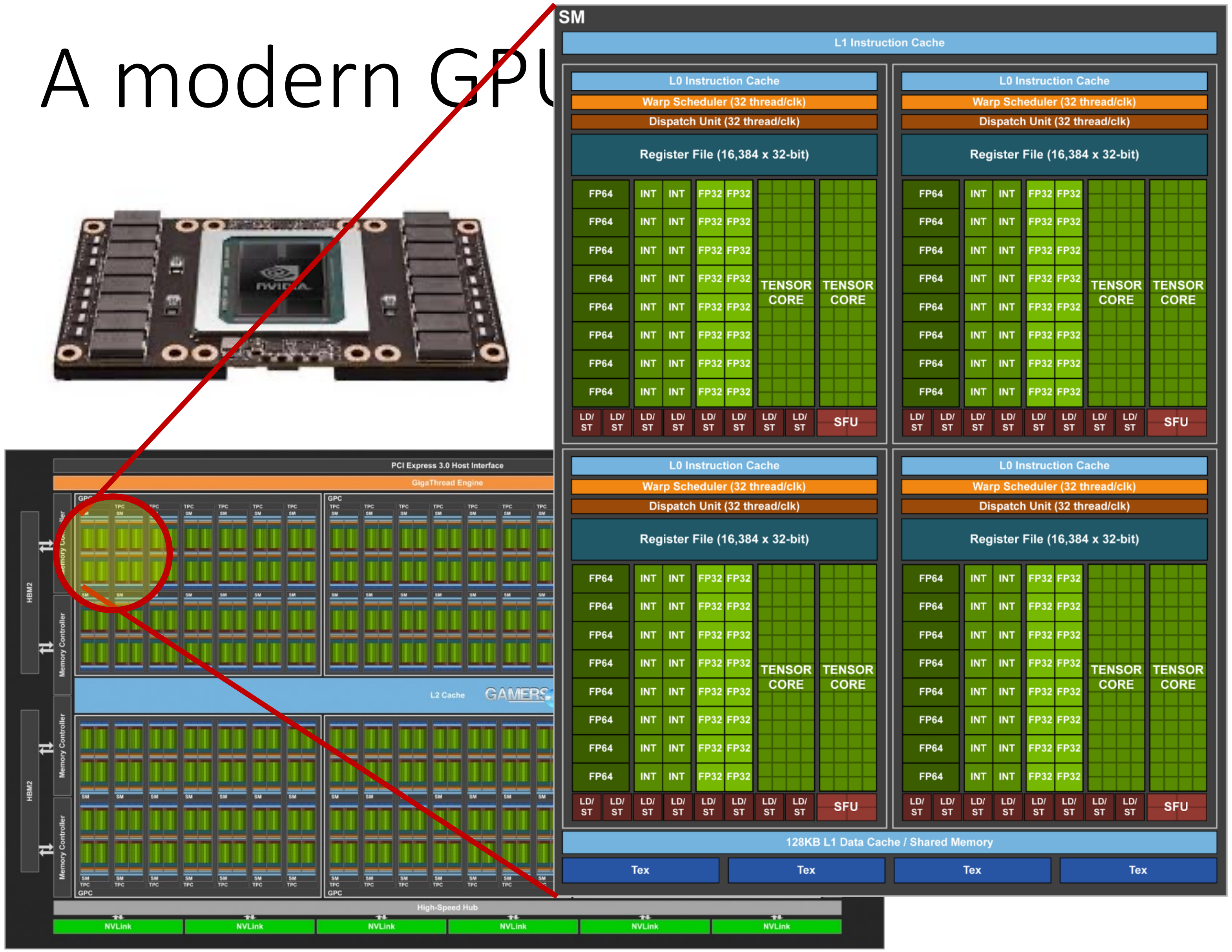

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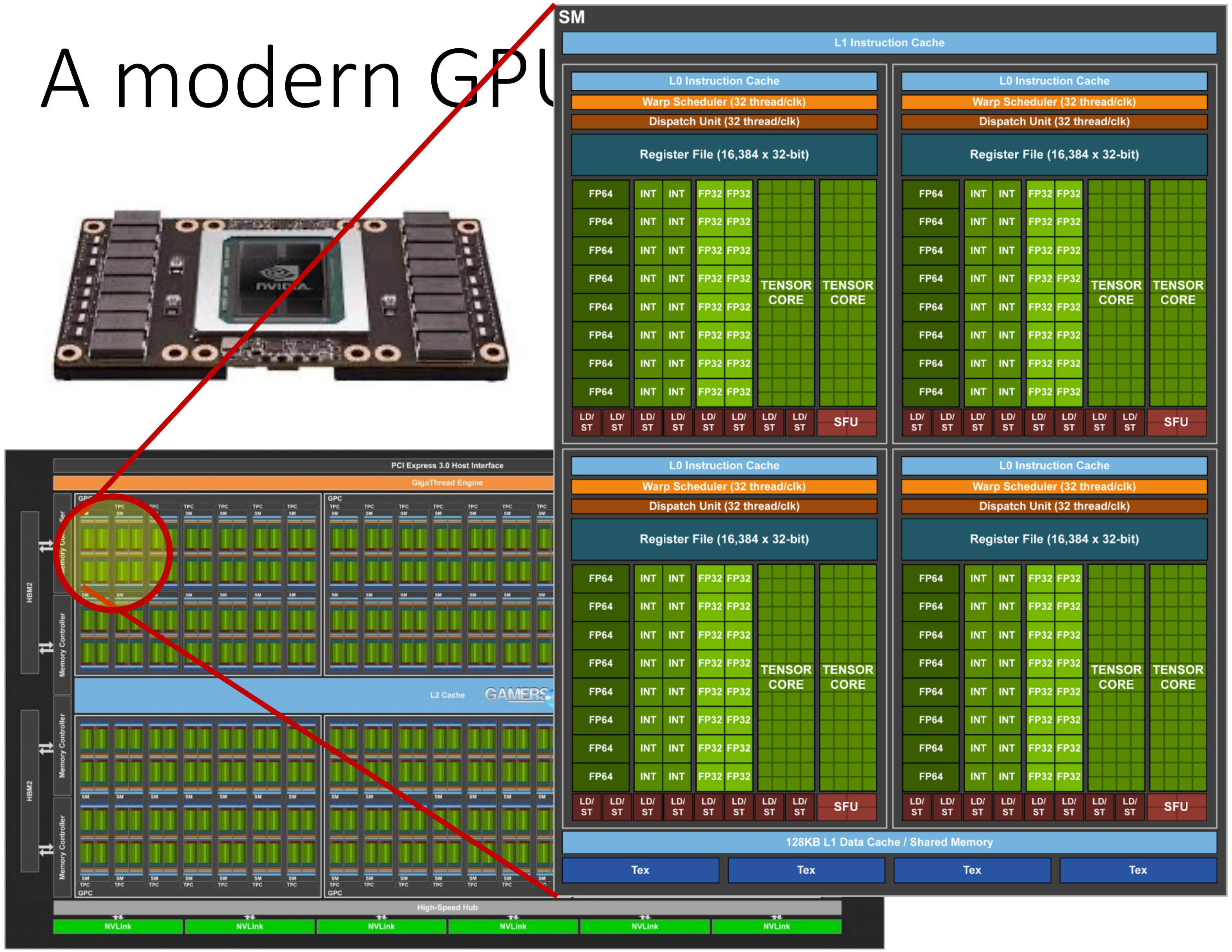
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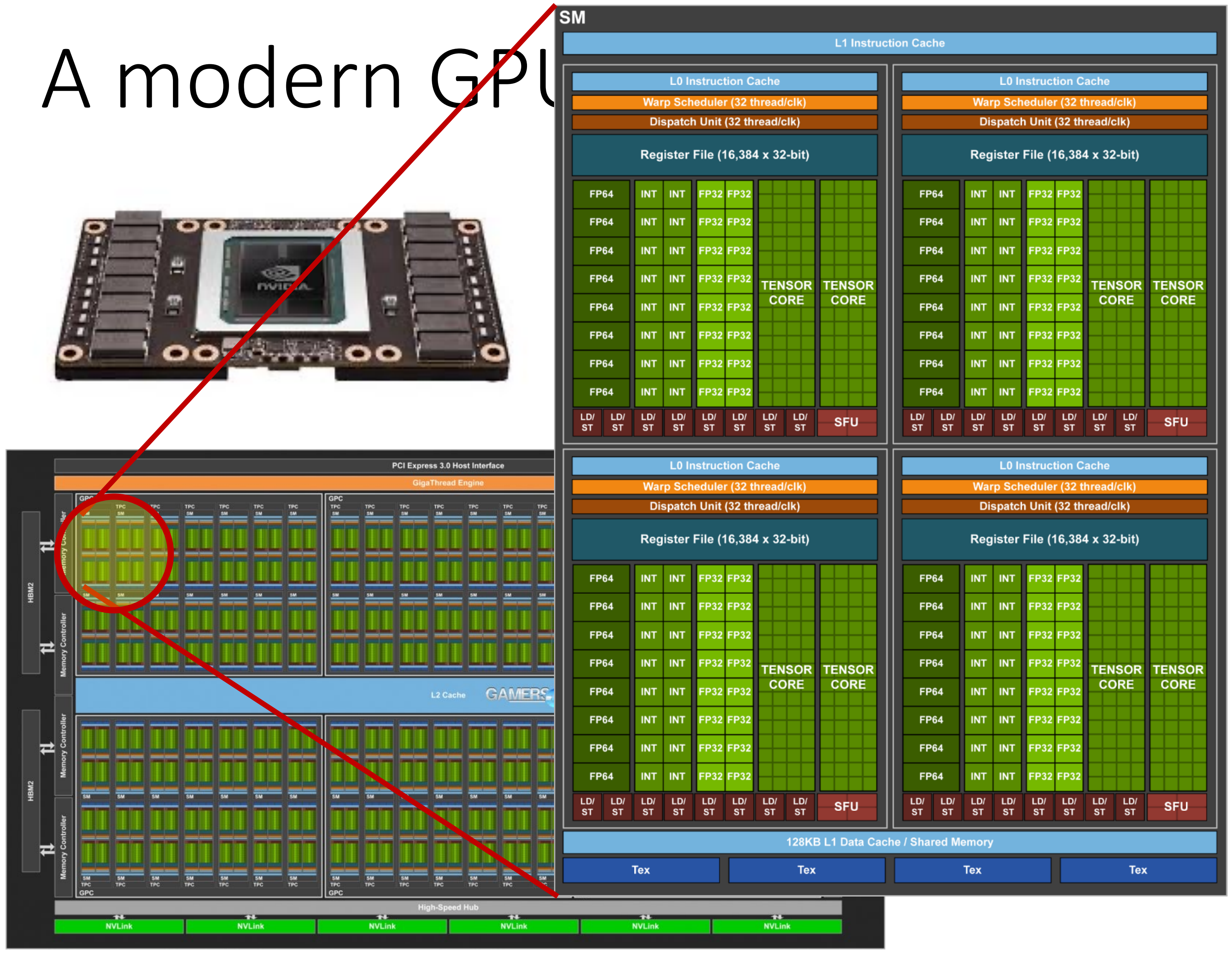
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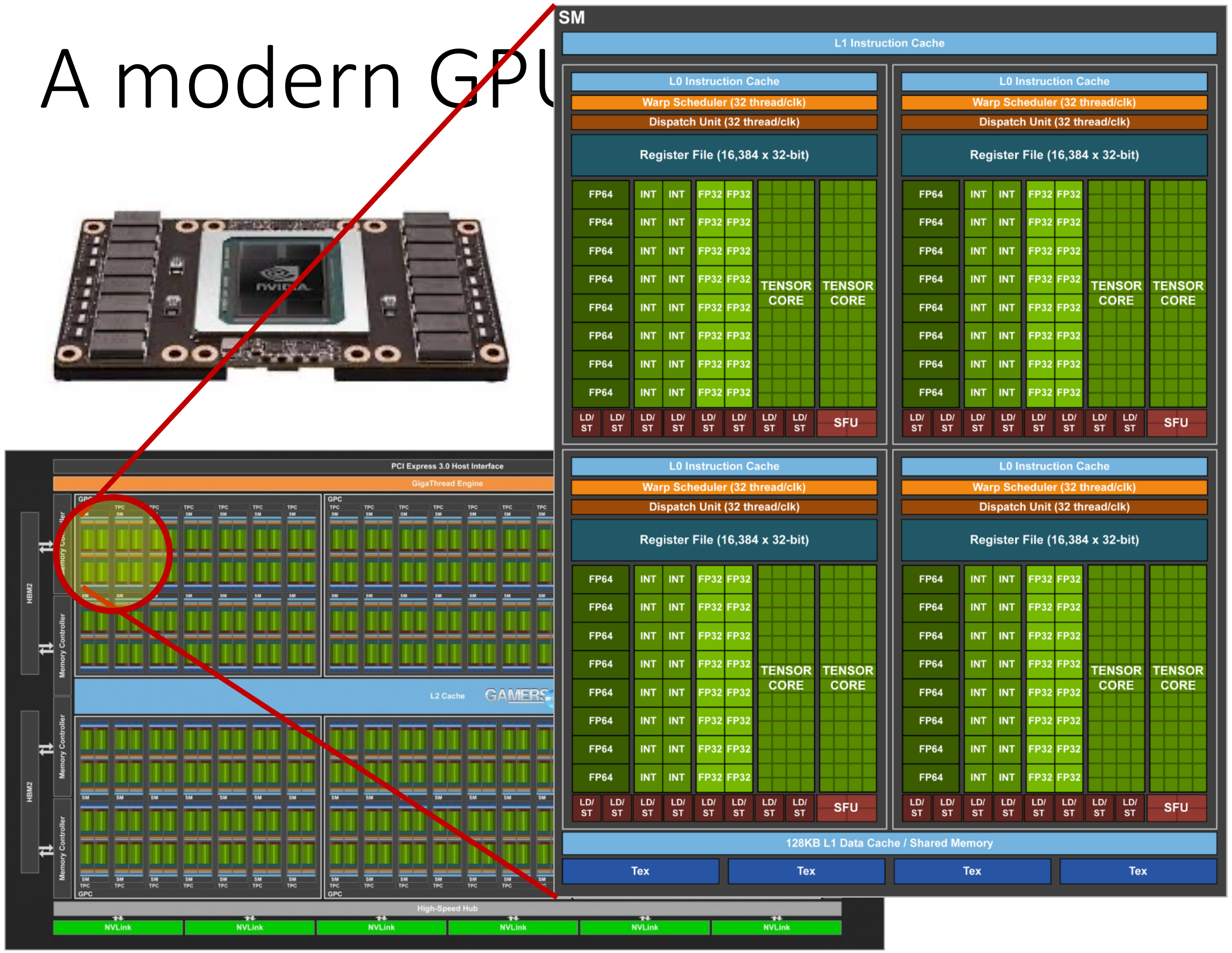
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How do you program a machine like this? pthread_create()?

GPUs: Outline

- Background from many areas
  - Architecture
    - Vector processors
    - Hardware multi-threading
  - Graphics
    - Graphics pipeline
    - Graphics programming models
  - Algorithms
    - parallel architectures $\rightarrow$ parallel algorithms
- Programming GPUs
  - CUDA
  - Basics: getting something working
  - Advanced: making it perform

Architecture Review: Pipelines

Processor algorithm:

```
main() {
  while(true)
    do_next_instruction();
}
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do_next_instruction() {
  instruction = fetch();
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Processor algorithm:

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    main() {
      v
    
    }



  do_n
    inst
    ops
    exe
    access_memory(ops, regs);
    write_back(regs);
  }
```

```
main() {
  pthread_create(do_instructions);
  pthread_create(do_decode);
  pthread_create(do_execute);
  …
  pthread_join(… );
  …
}
```

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```

```
do_instructions() {
  while(true) {
    instruction = fetch();
    enqueue(DECODE, instruction);
}}

do_decode() {
  while(true) {
    instruction = dequeue();
    ops, regs = decode(instruction);
    enqueue(EX, instruction);
}}

do_execute() {
  while(true) {
    instruction = dequeue();
    execute_calc_addrs(ops, regs);
    enqueue(MEM, instruction);
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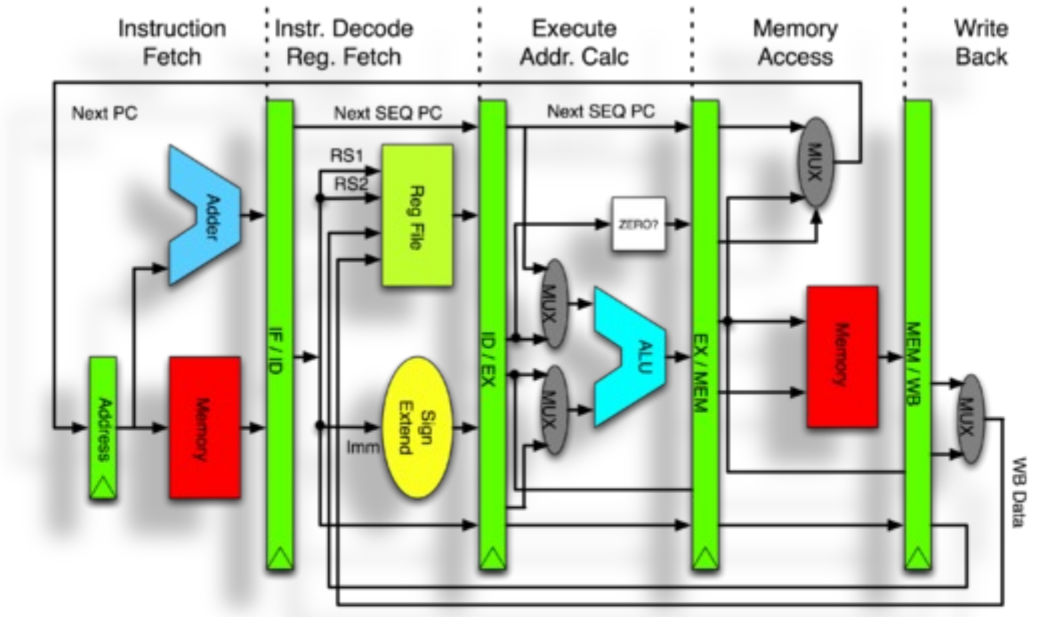

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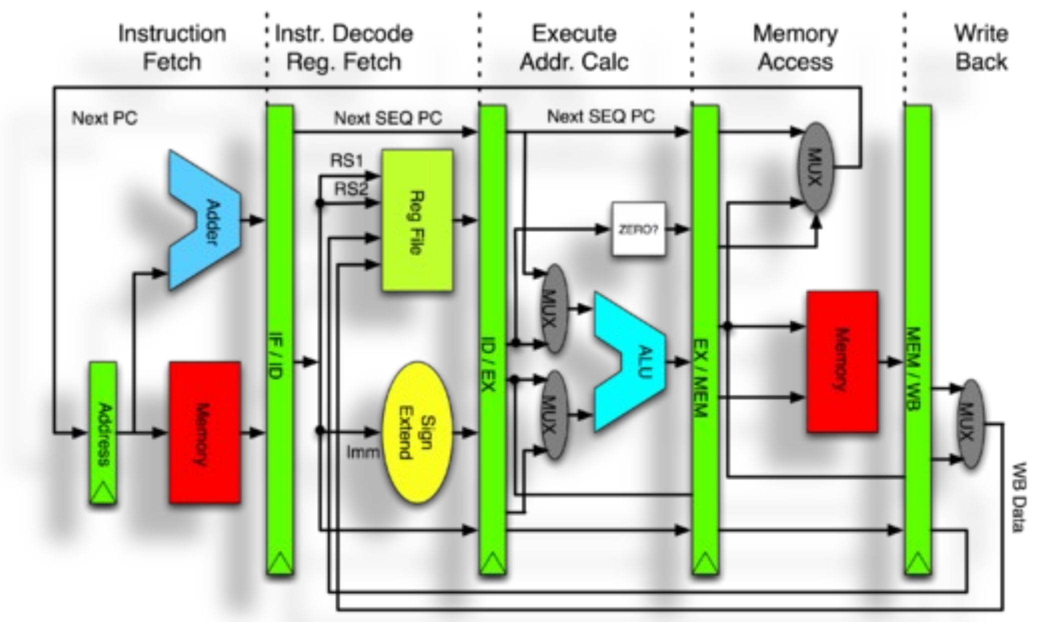

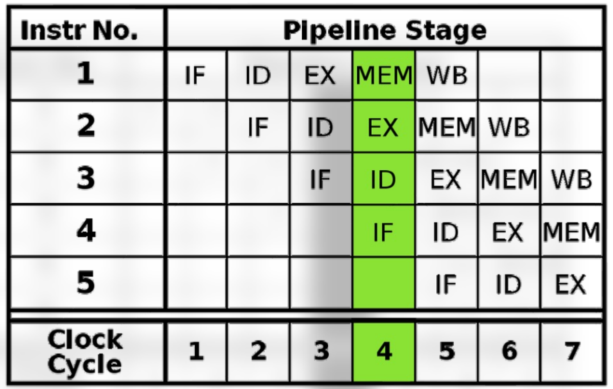

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2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

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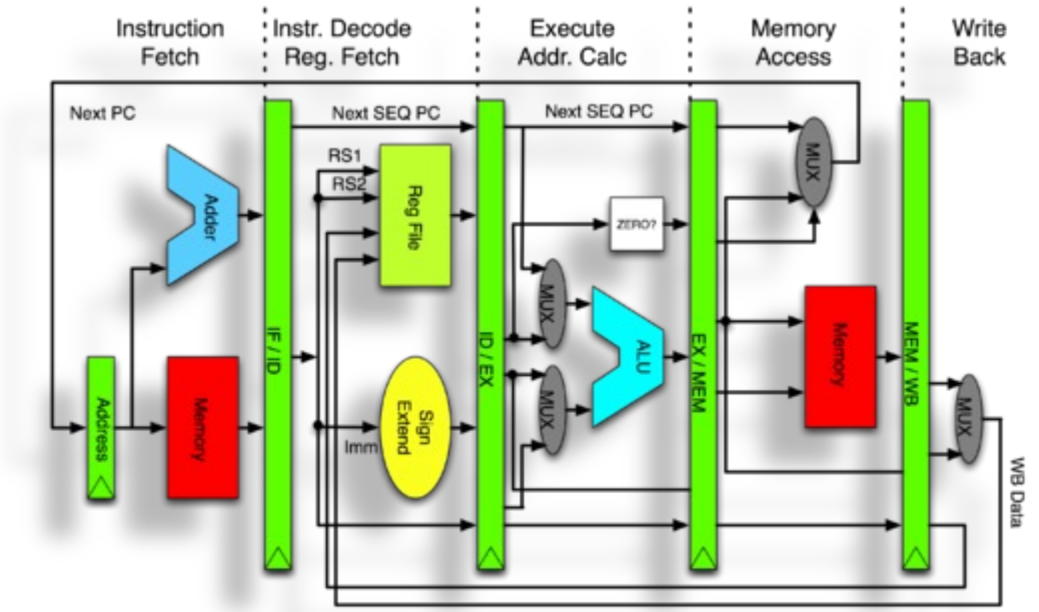

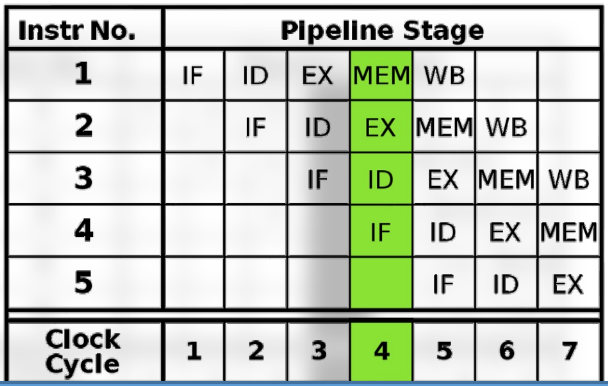

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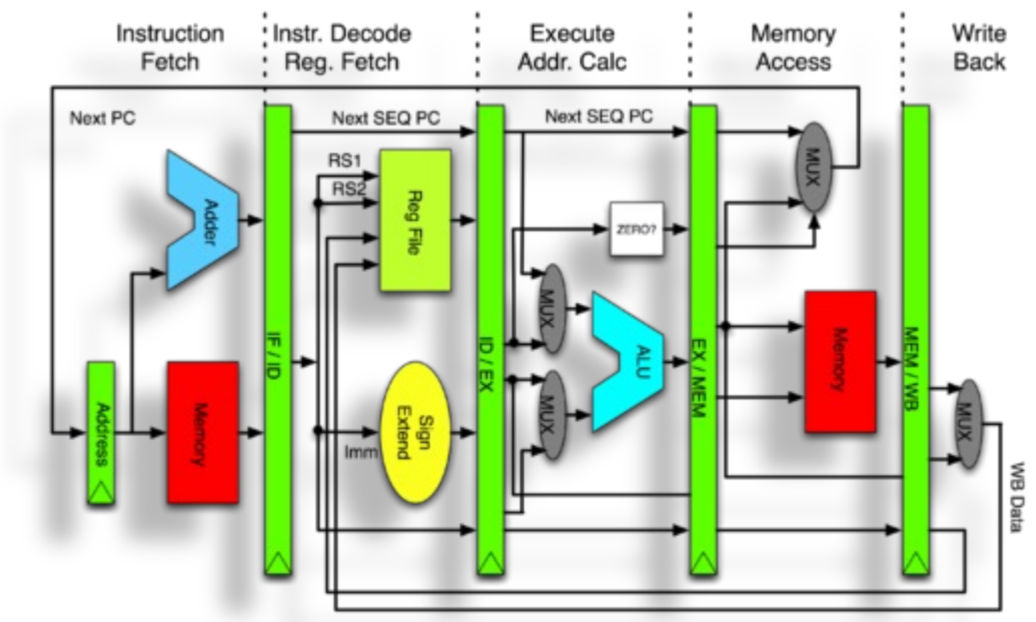

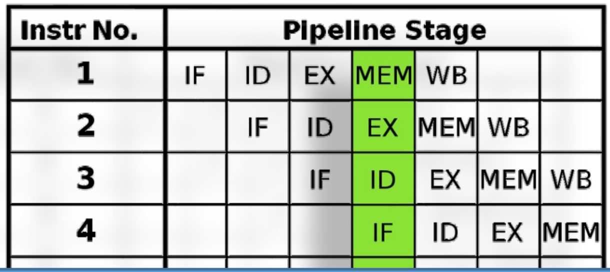

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Works well if pipeline is kept full
What kinds of things cause "bubbles"/stalls?

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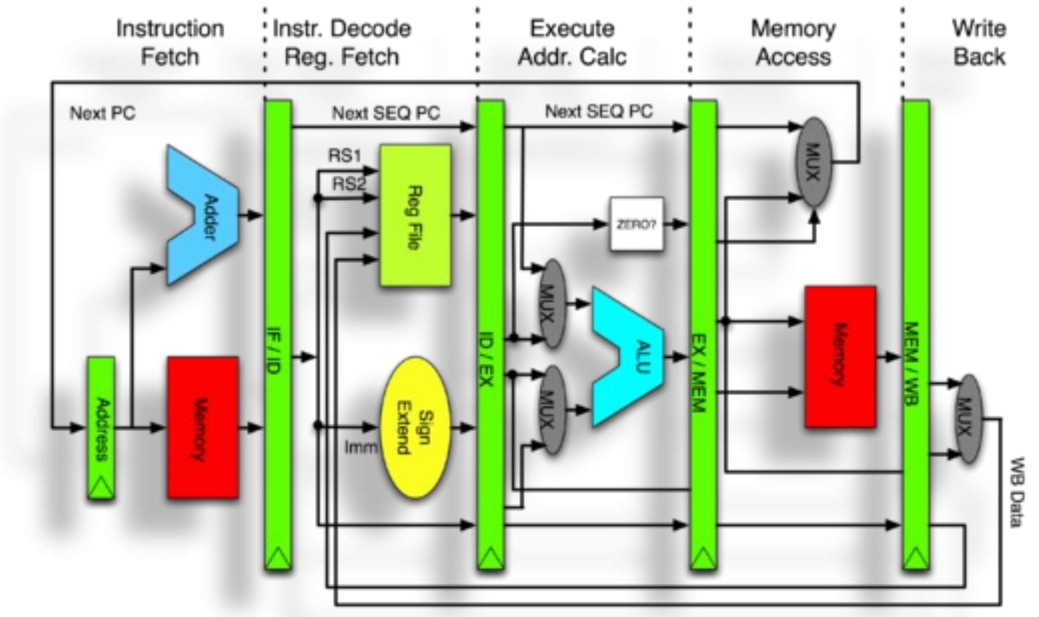

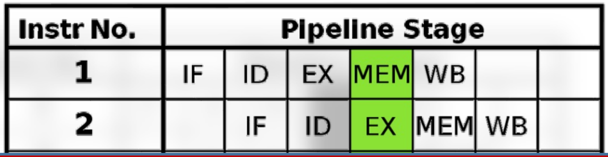

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How can we get *more* parallelism?

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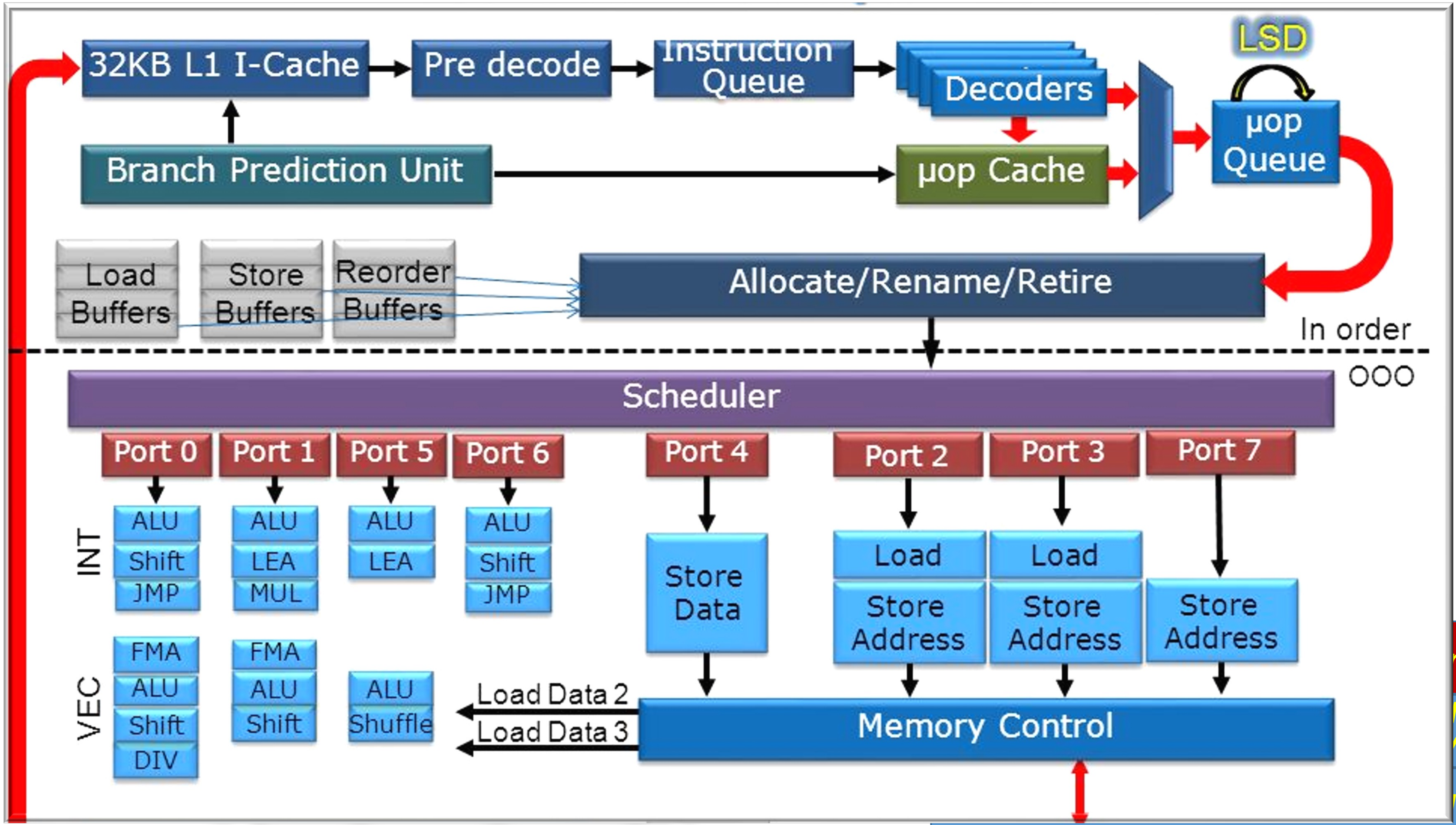

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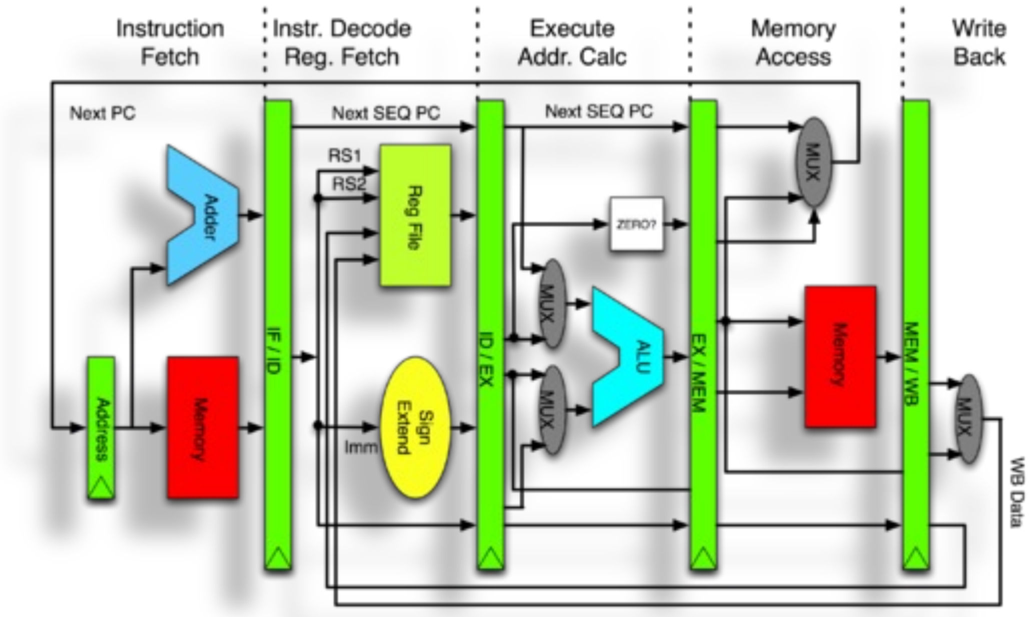

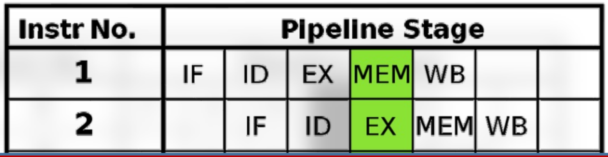

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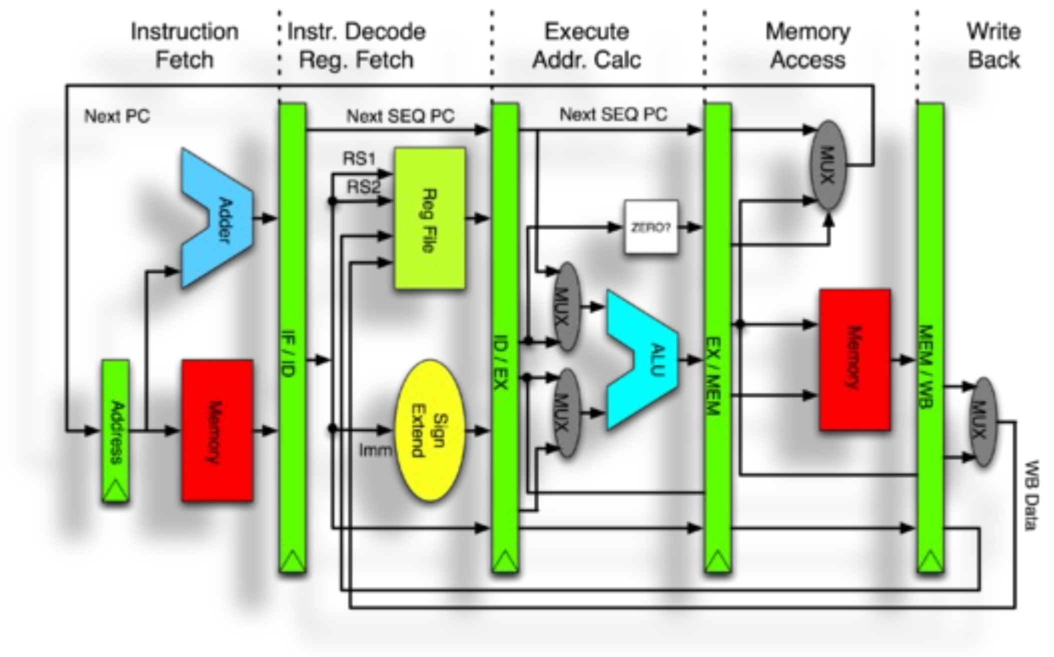

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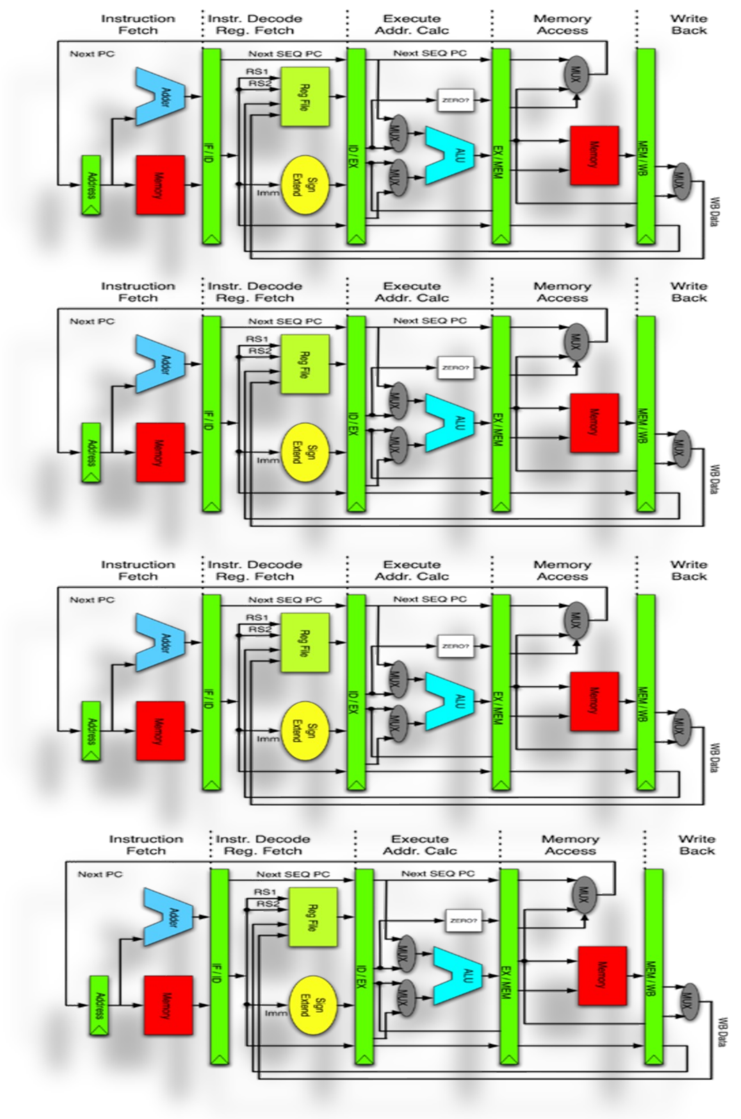

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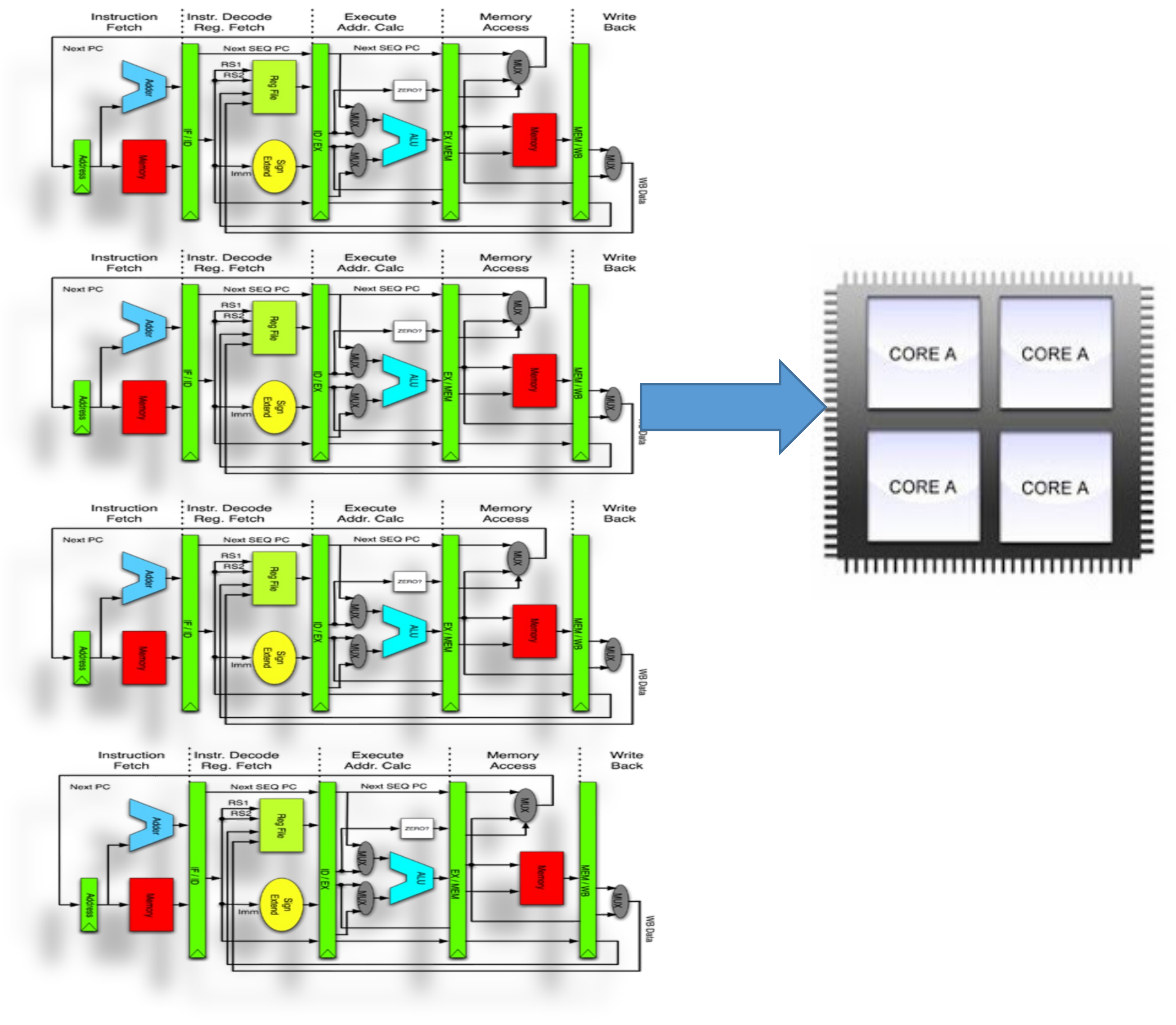

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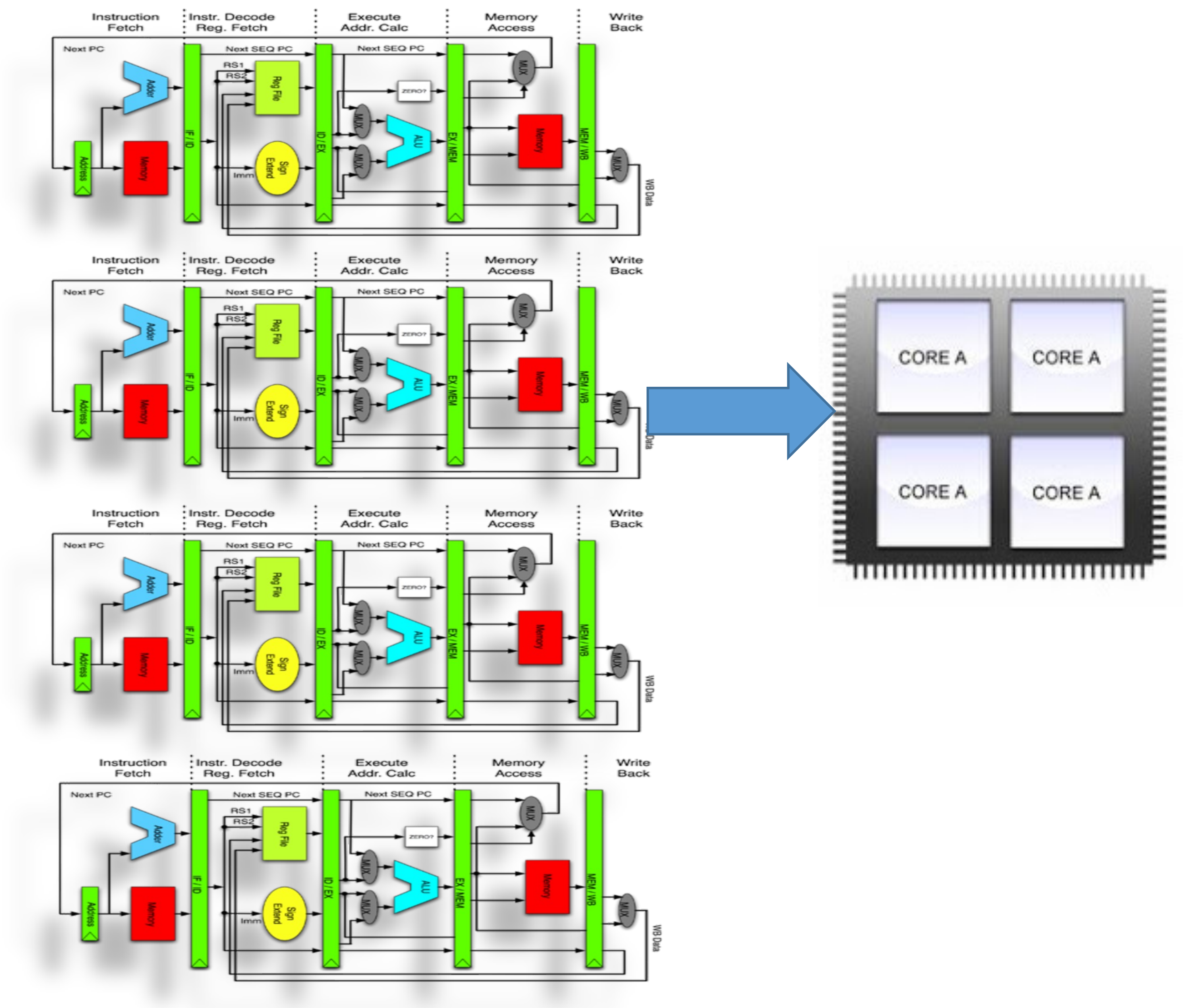

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  for(i=0; i<CORES; i++) {
    pthread_create(
        do_instructions());
  }
}
do_instructions() {
  while(true) {
    instruction = fetch();
    ops, regs = decode(instruction);
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- ***Pros: Simple***
- ***Cons: programmer has to find the parallelism!***

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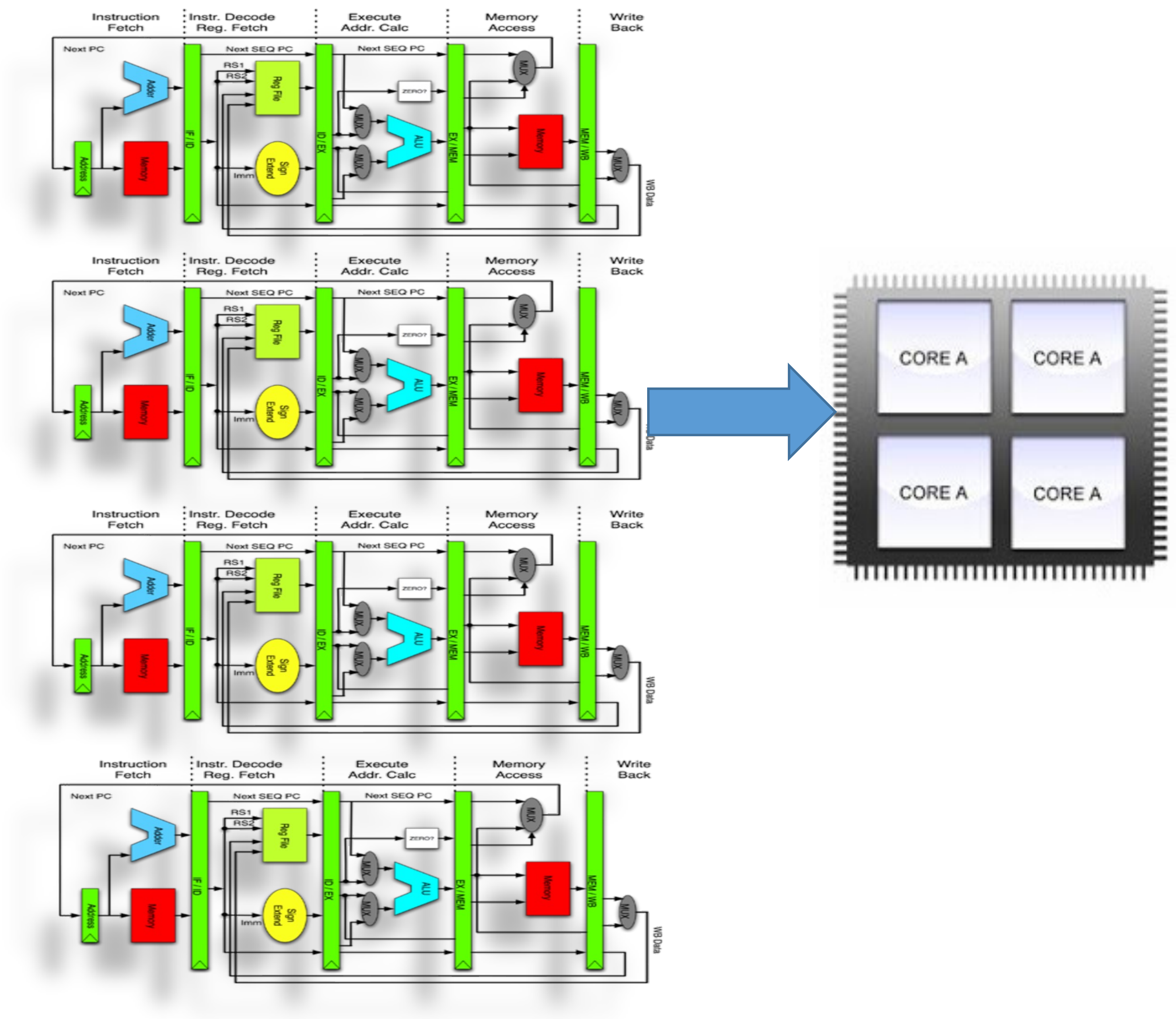

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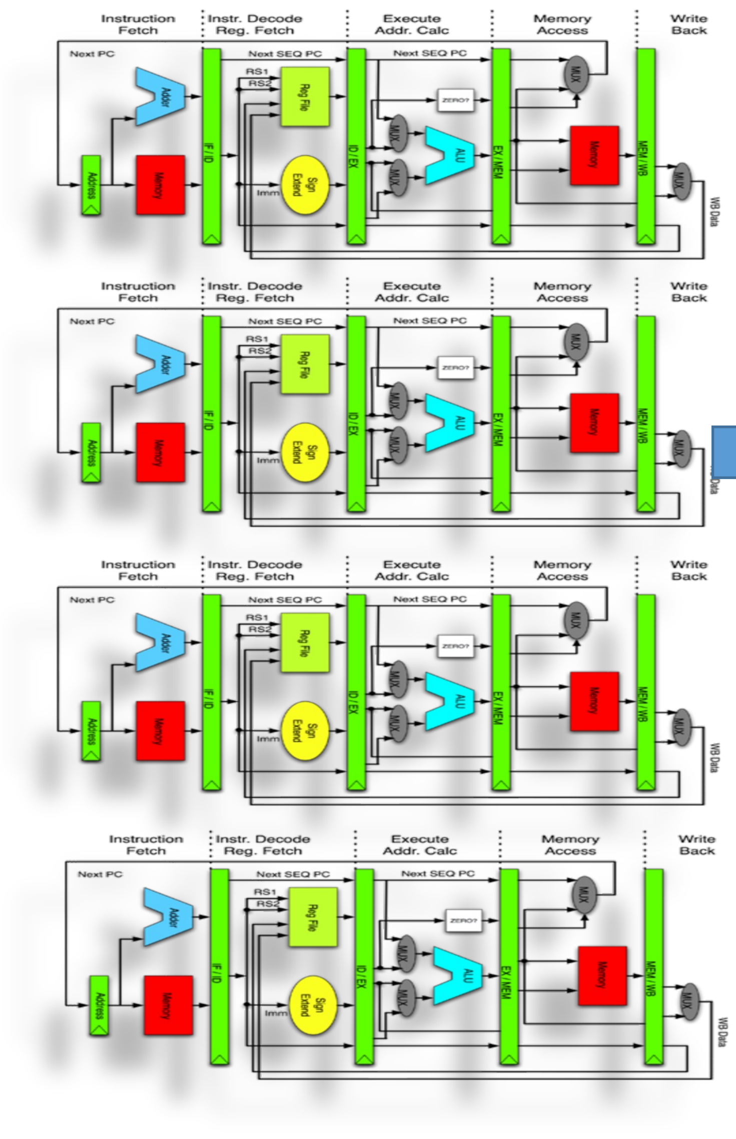
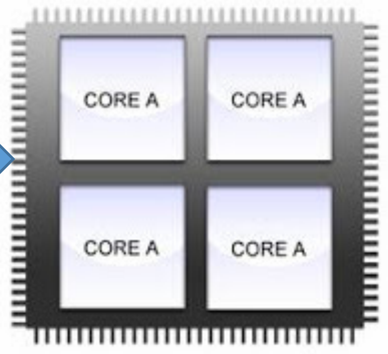
Multi-core/SMPs

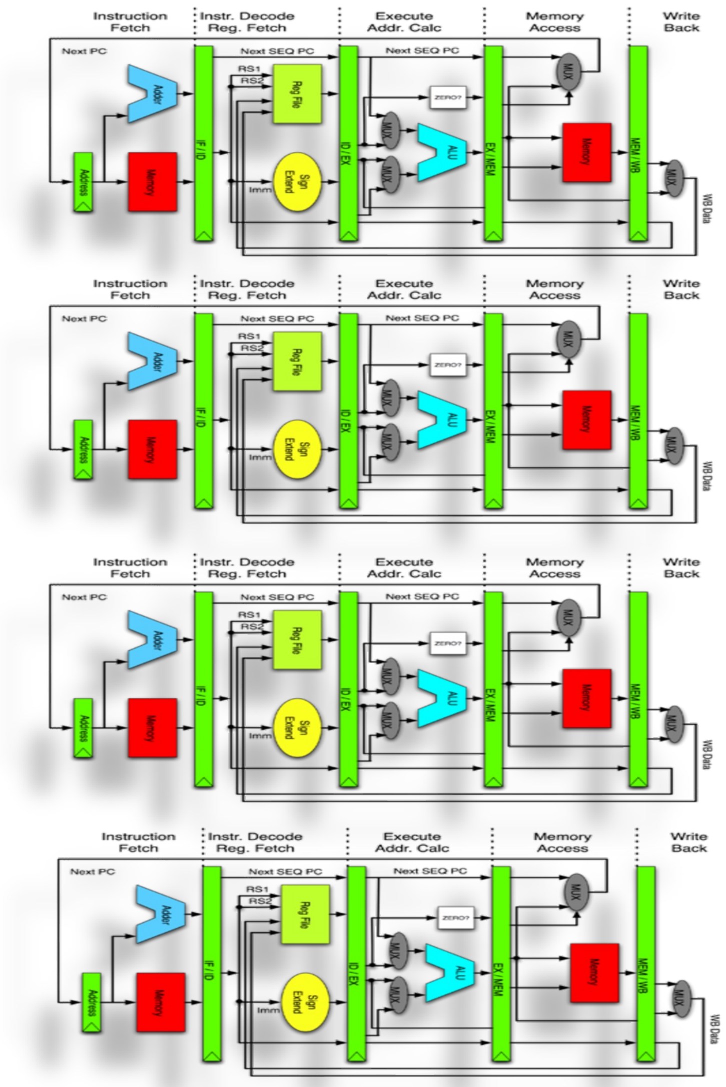




```
main() {
  for(i=0; i<CORES; i++) {
    pthread_create(
        do_instructions());
   }
}
do_instructions() {
  while(true) {
    instruction = fetch();
    ops, regs = decode(instruction);
    execute_calc_addrs(ops, regs);
    access_memory(ops, regs);
    write_back(regs);
}}
```

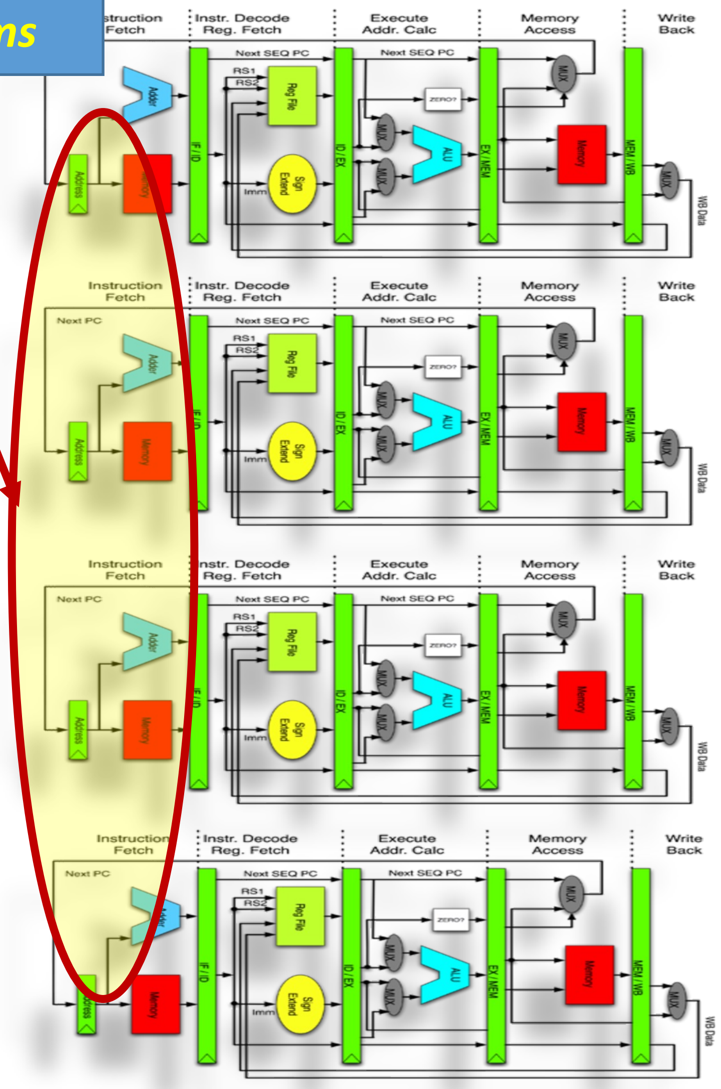
Other techniques extract parallelism here, try to let the machine find parallelism

Superscalar processors



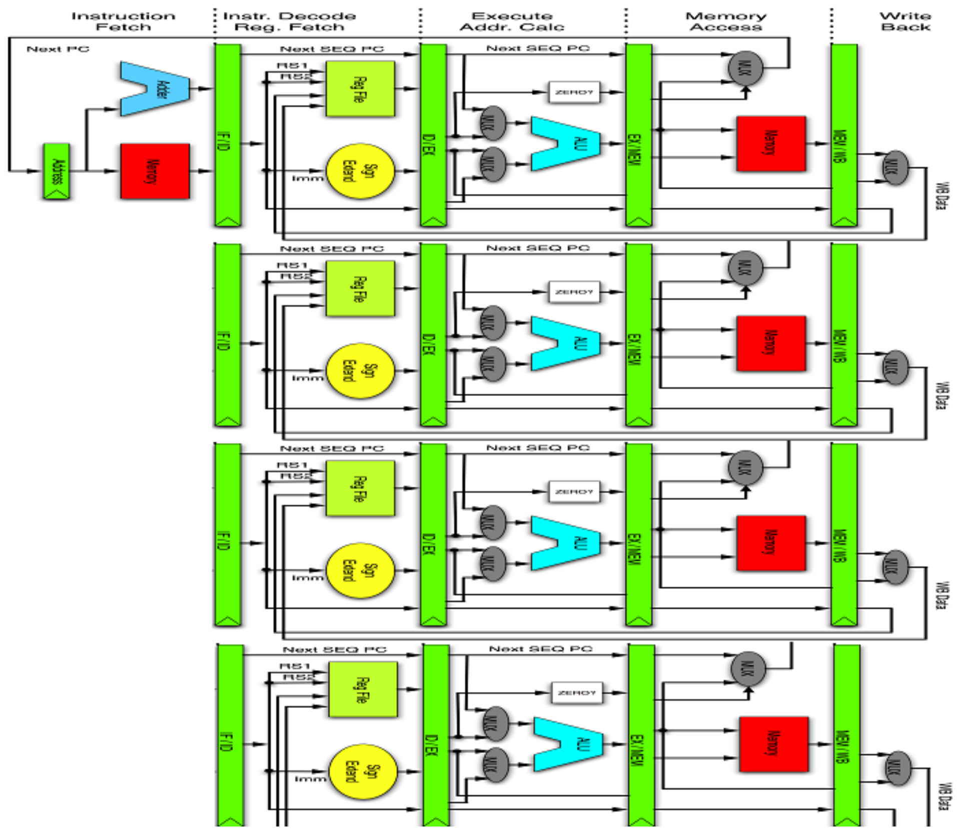
Superscalar processors

Remove extra instruction streams

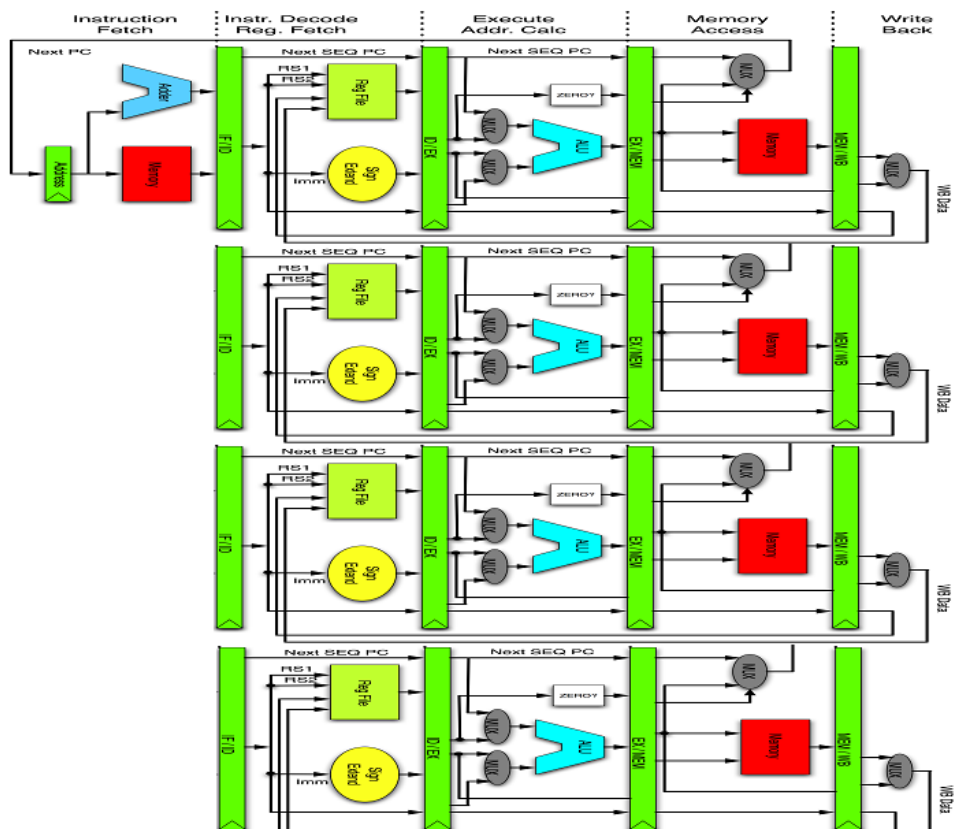


Superscalar processors

Superscalar processors



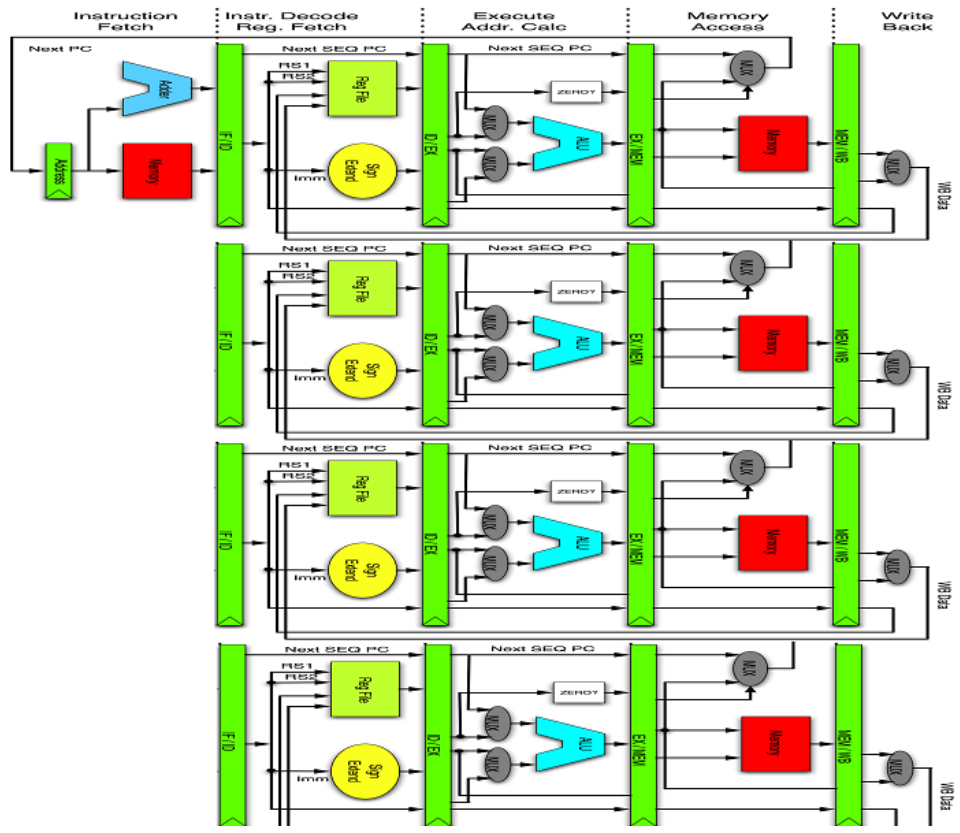
Superscalar processors



```
main() {
 for(i=0; i<CORES; i++)
  pthread_create(decode_exec);
  while(true) {
   instruction = fetch();
   enqueue(instruction);
  }
}

decode_exec() {
  instruction = dequeue();
  ops, regs = decode(instruction);
  execute_calc_addrs(ops, regs);
  access_memory(ops, regs);
  write_back(regs);
}
```

Superscalar processors



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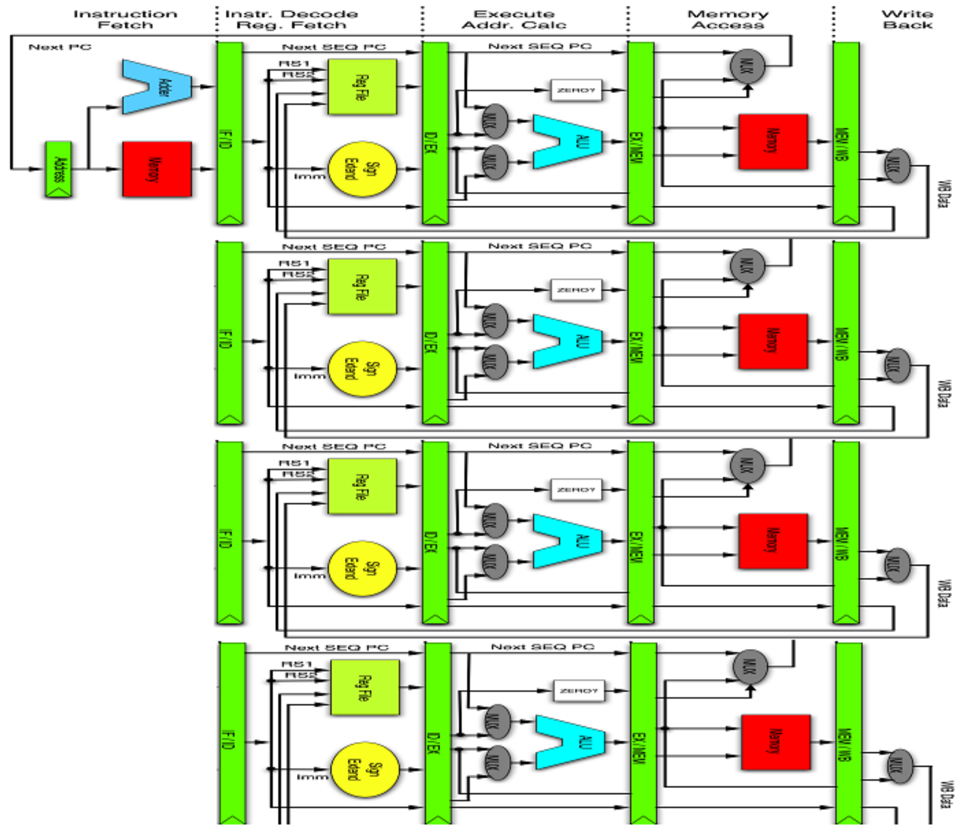
Doesn't look that different does it? Why do it?

Superscalar processors



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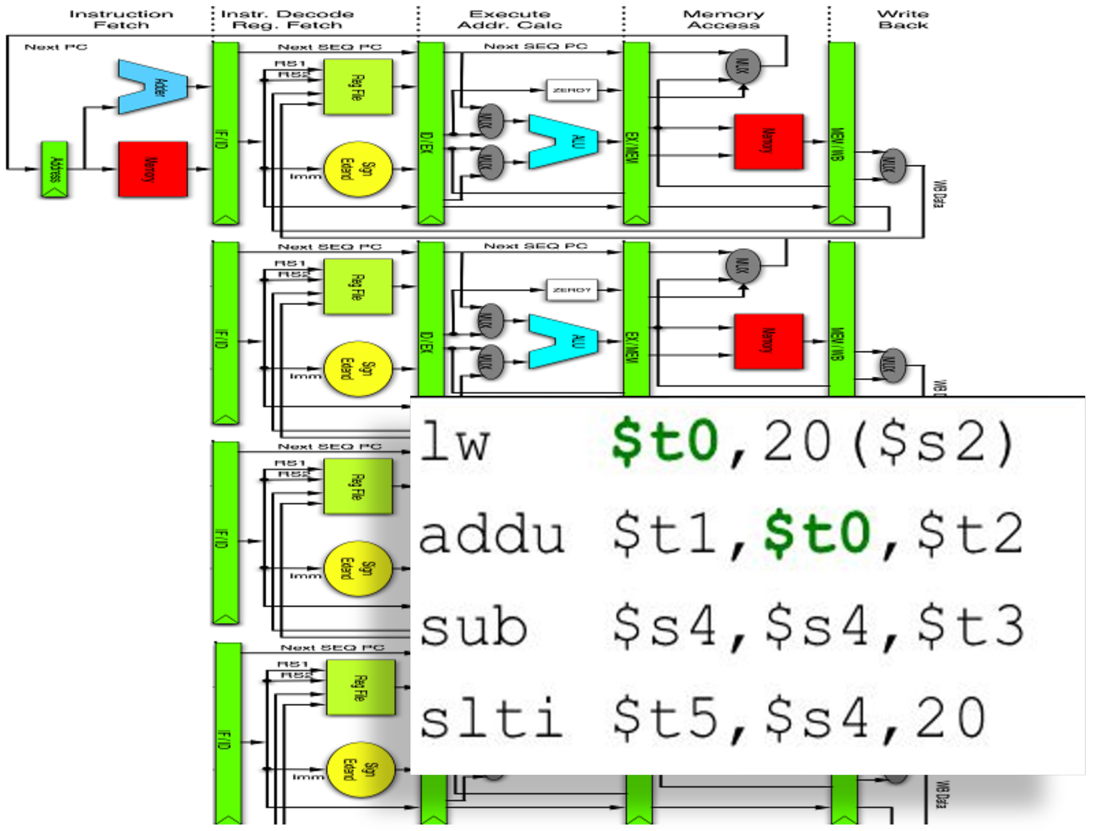
Enables independent instruction parallelism.

Superscalar processors



```
lw    $t0,20($s2)
addu  $t1,$t0,$t2
sub   $s4,$s4,$t3
slti  $t5,$s4,20
```

```
main() {
  for(i=0; i<CORES; i++)
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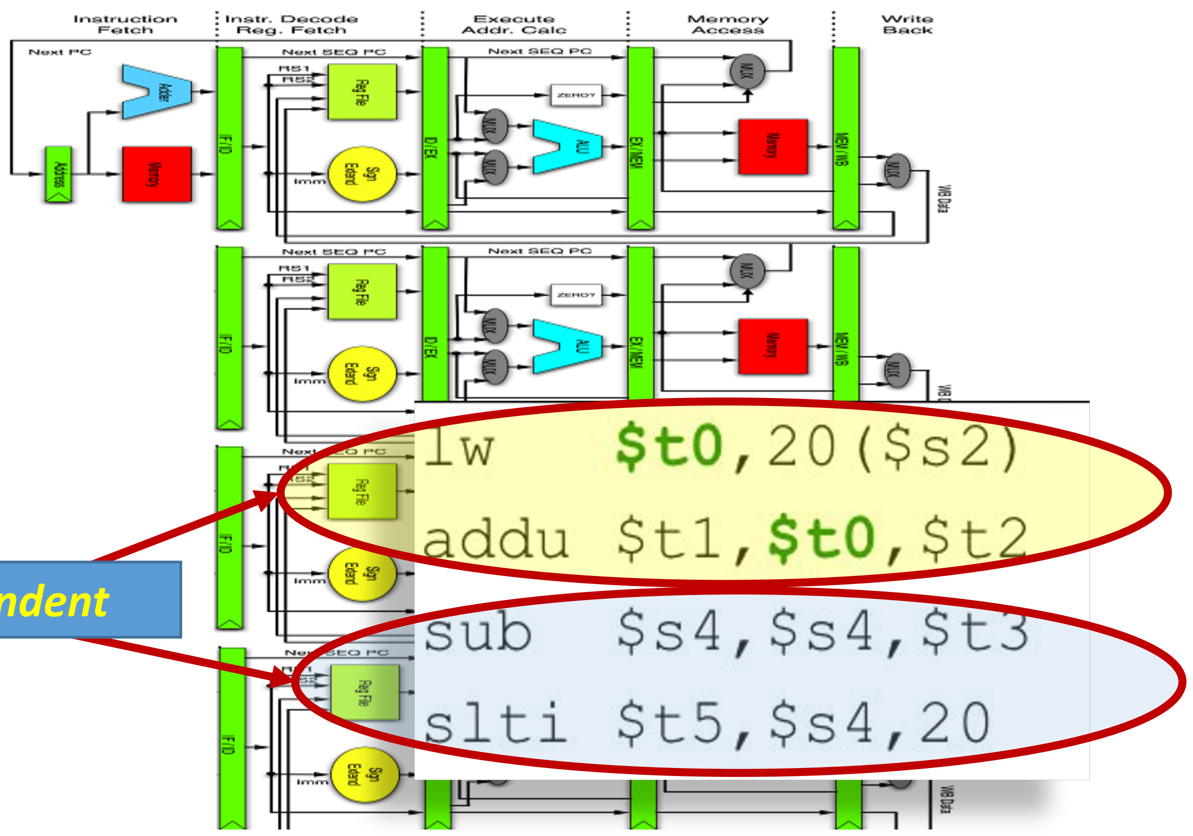
Superscalar processors



```
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independent

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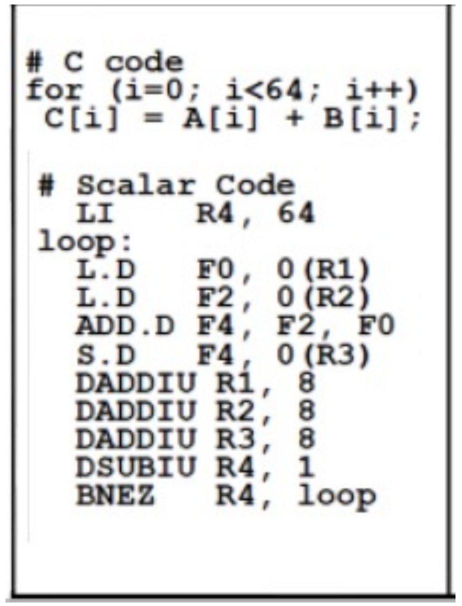
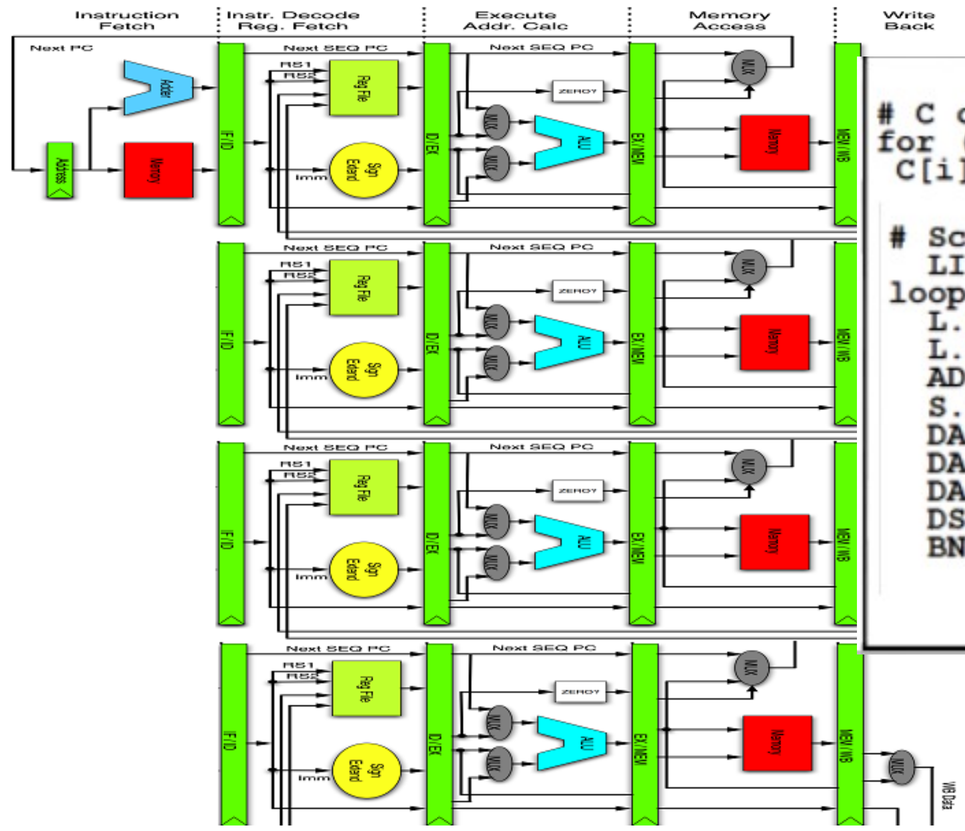
Vector/SIMD processors

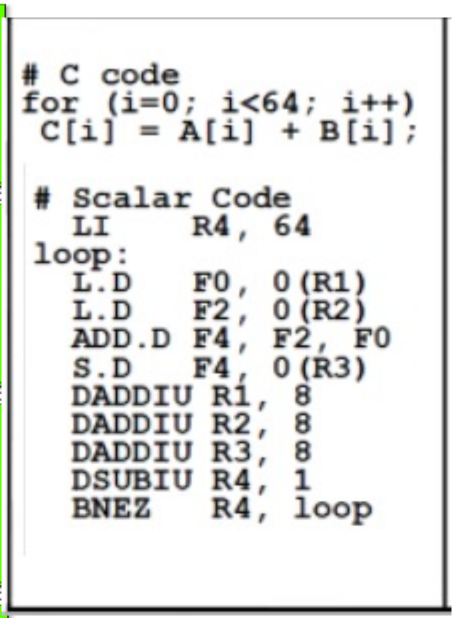


```
# C code
for (i=0; i<64; i++)
 C[i] = A[i] + B[i];

 # Scalar Code
   LI     R4, 64
 loop:
   L.D    F0, 0(R1)
   L.D    F2, 0(R2)
   ADD.D  F4, F2, F0
   S.D    F4, 0(R3)
   DADDIU R1, 8
   DADDIU R2, 8
   DADDIU R3, 8
   DSUBIU R4, 1
   BNEZ   R4, loop
```

Vector/SIMD processors





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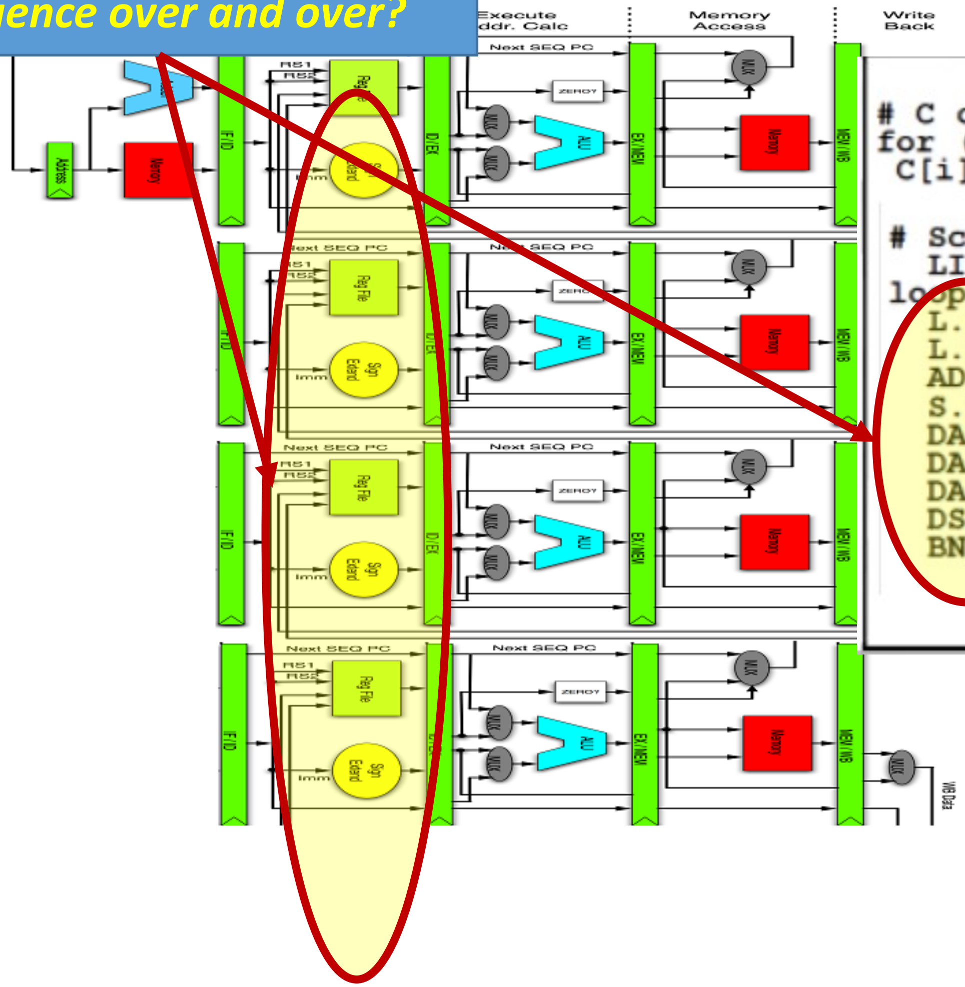
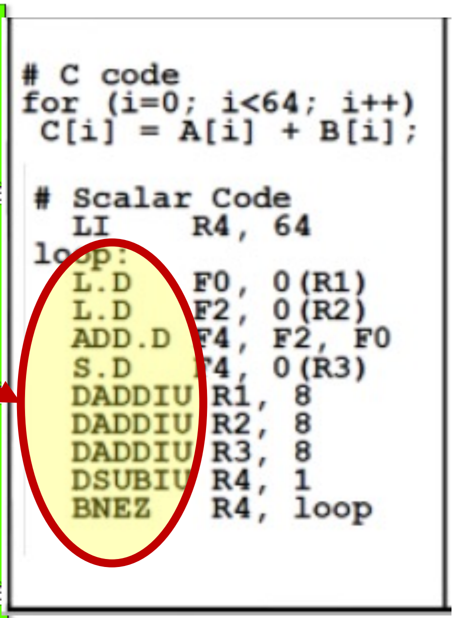
```

Vector/SIMD processors

Why decode same instruction sequence over and over?





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    S.D     F4, 0(R3)
    DADDIU  R1, 8
    DADDIU  R2, 8
    DADDIU  R3, 8
    DSUBIU  R4, 1
    BNEZ    R4, loop
```
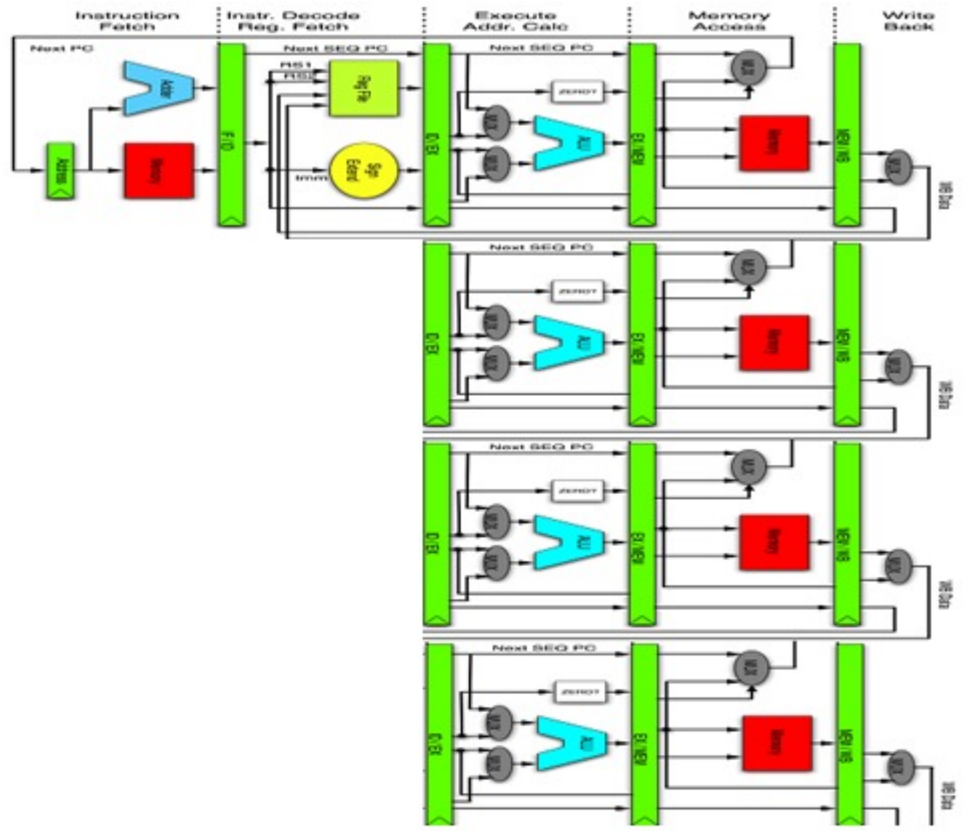
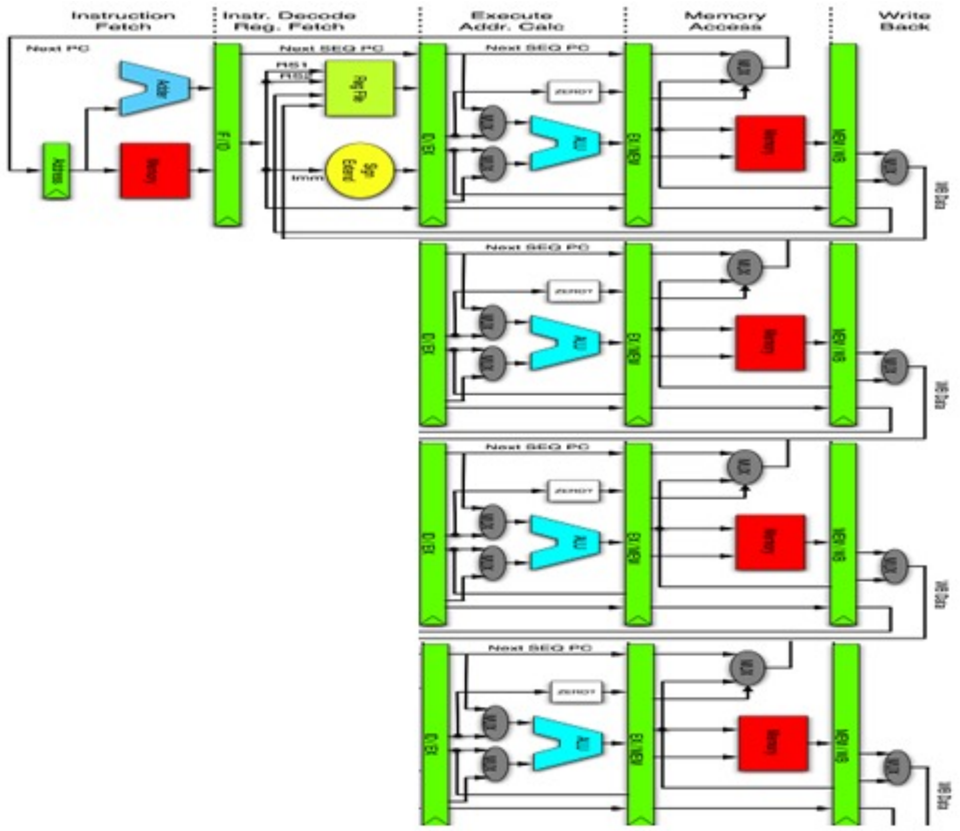

Vector/SIMD processors



Vector/SIMD processors



```
main() {
 for(i=0; i<CORES; i++)
   pthread_create(exec);
   while(true) {
      ops, regs = fetch_decode();
      enqueue(ops, regs);
   }
}


exec() {
  ops, regs = dequeue();
  execute_calc_addrs(ops, regs);
  access_memory(ops, regs);
  write_back(regs);
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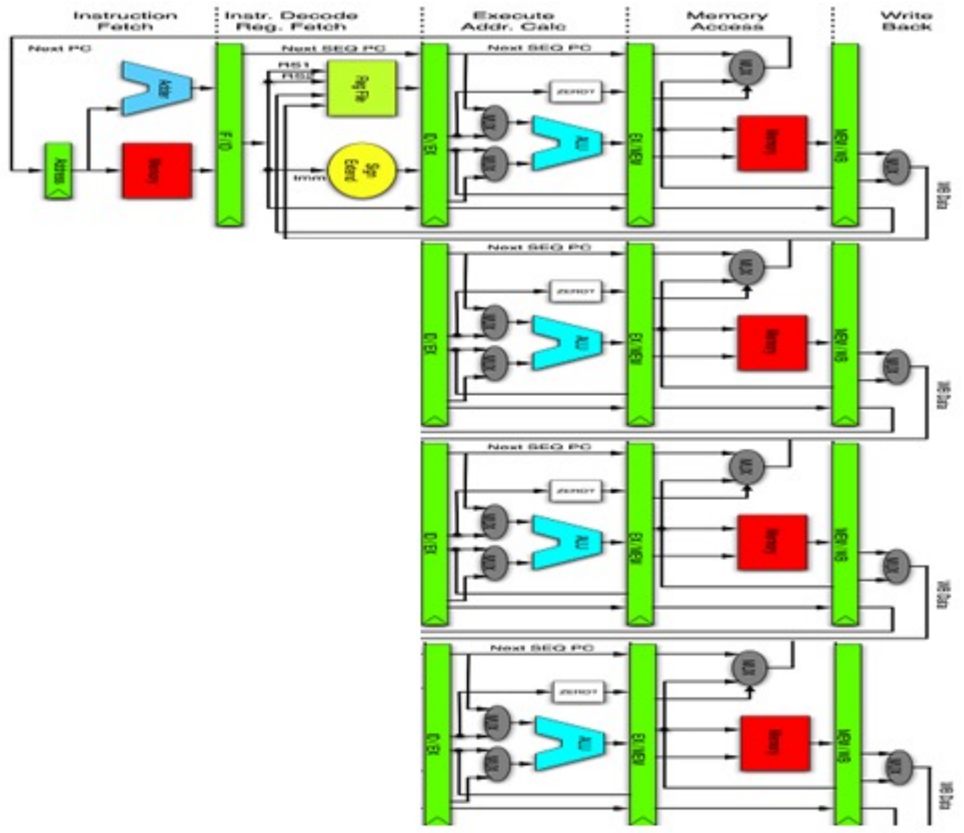
Vector/SIMD processors



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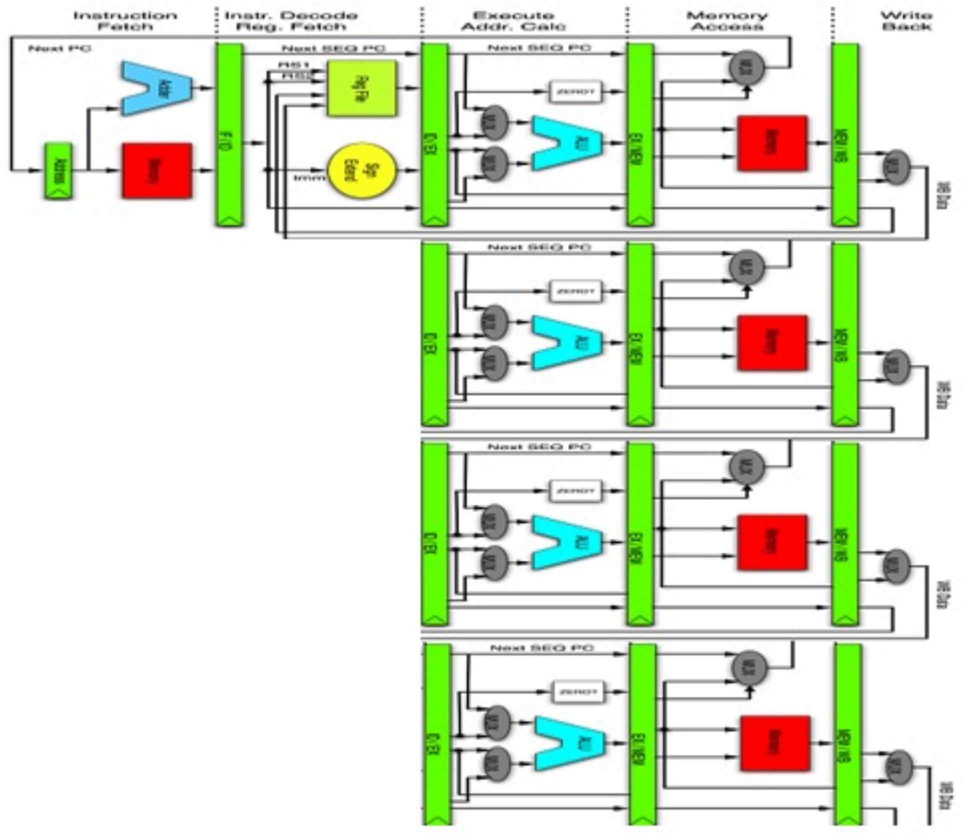
Single instruction stream, multiple computations

Vector/SIMD processors



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  access_memory(ops, regs);
  write_back(regs);
}
```

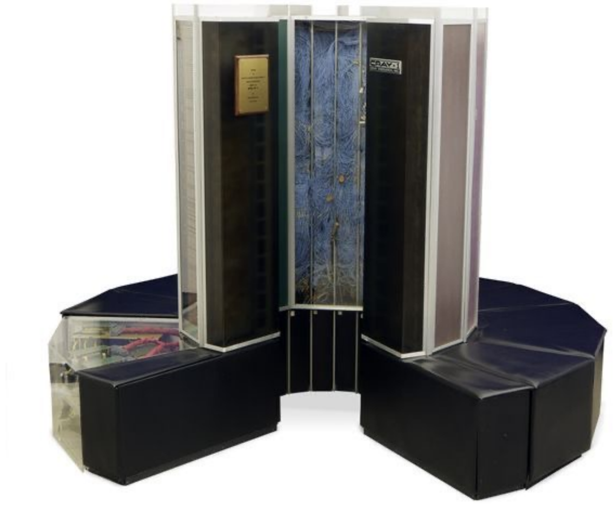
Single instruction stream, multiple computations

But now all my instructions need multiple operands!

Vector Processors

- Process multiple data elements simultaneously.
- Common in supercomputers of the 1970’s 80’s and 90’s.
- Modern CPUs support some vector processing instructions
  - Usually called SIMD
- Can operate on a few vectors elements per clock cycle in a pipeline or,
  - SIMD operate on all per clock cycle

Vector Processors



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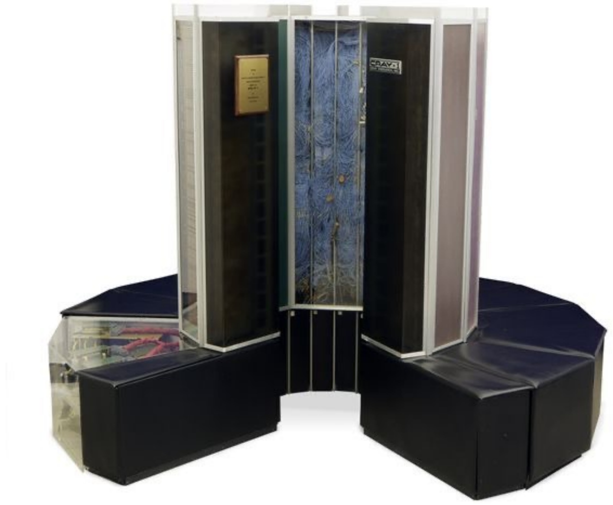
- 1962 University of Illinois Illiac IV - completed 1972 → 64 ALUs 100-150 MFlops
- (1973) TI’s Advance Scientific Computer (ASC) 20-80 MFlops
- (1975) Cray-1 first to have vector registers instead of keeping data in memory

Vector Processors



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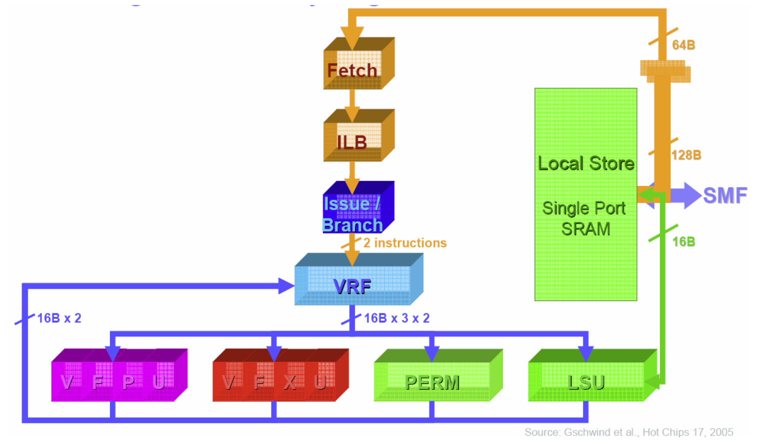
Single instruction stream, multiple data →
Programming model has to change

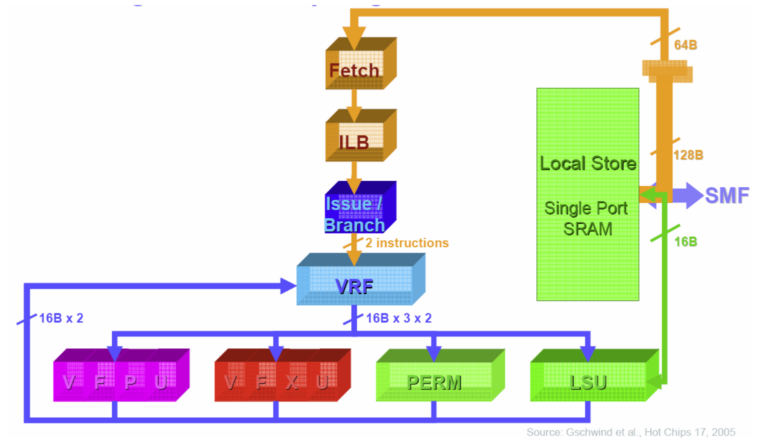
Vector Processors

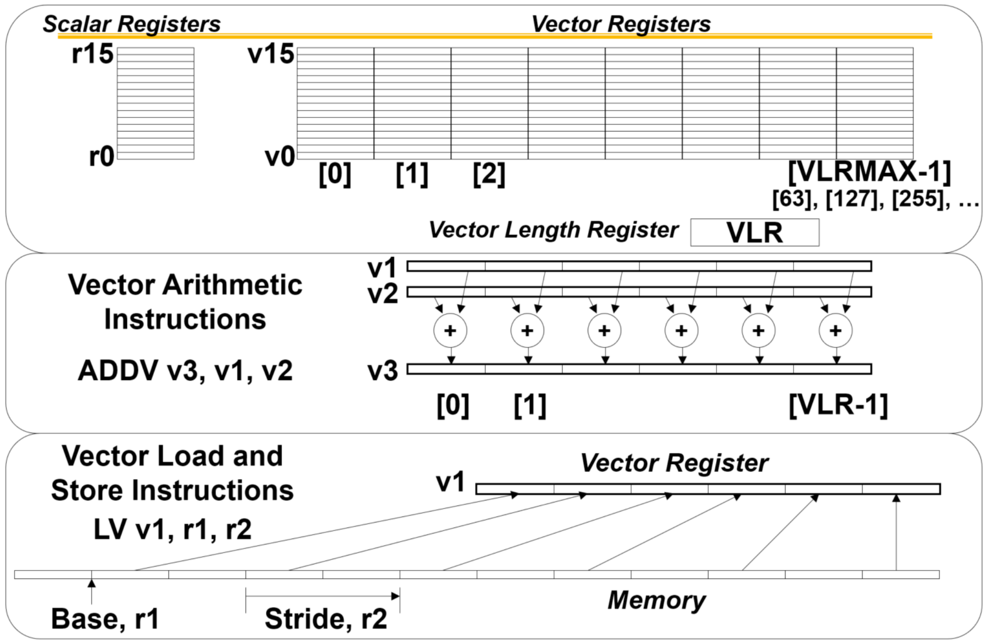


Implementation:

- Instruction fetch control logic shared
- Same instruction stream executed on
- Multiple pipelines
- Multiple different operands in parallel

Vector Processors





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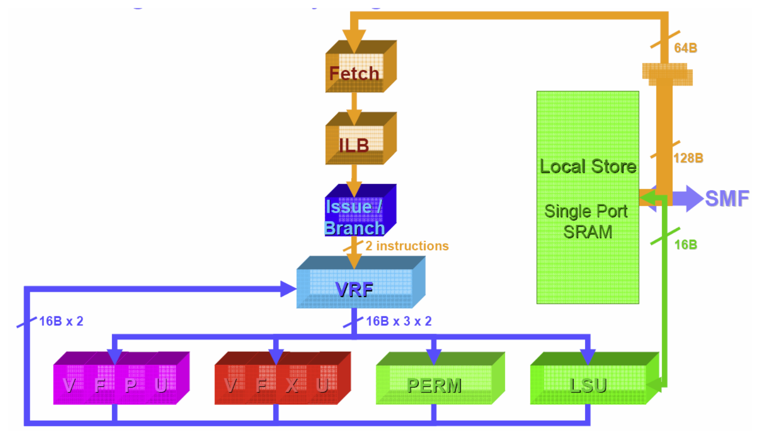
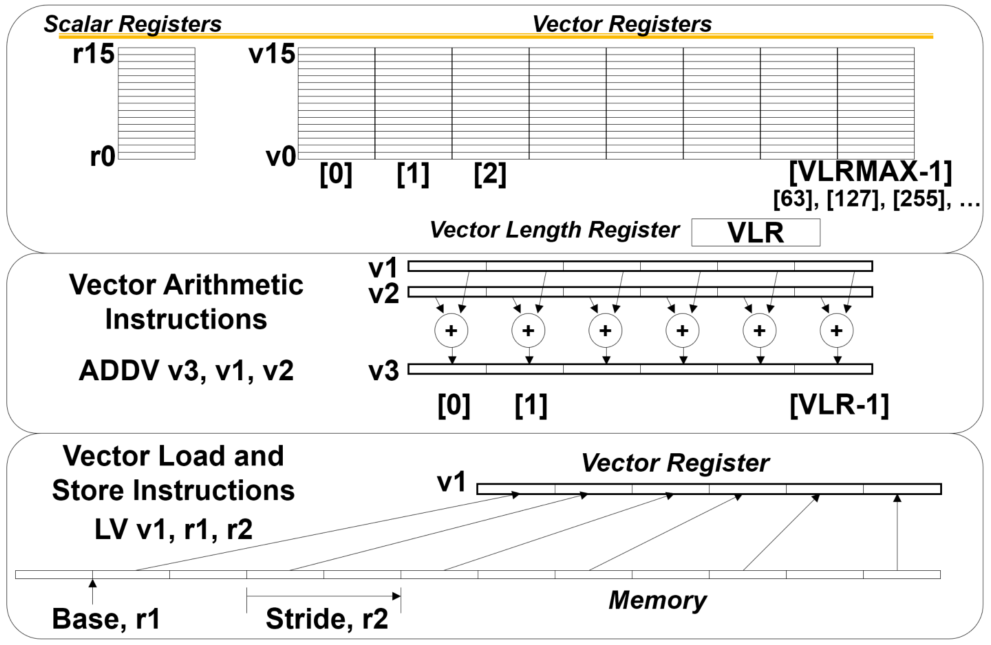
Vector Processors



Source: Gschwind et al., Hot Chips 17, 2005



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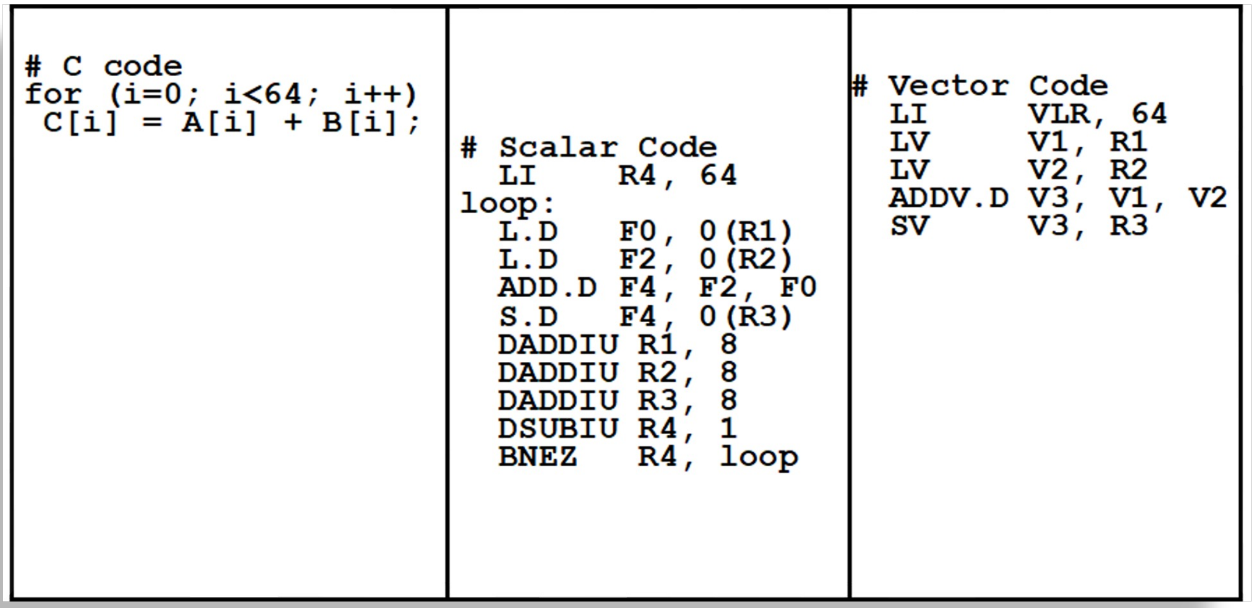

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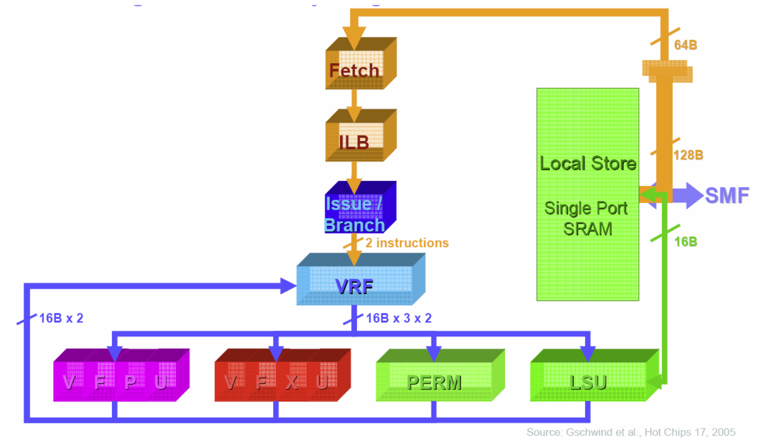
```

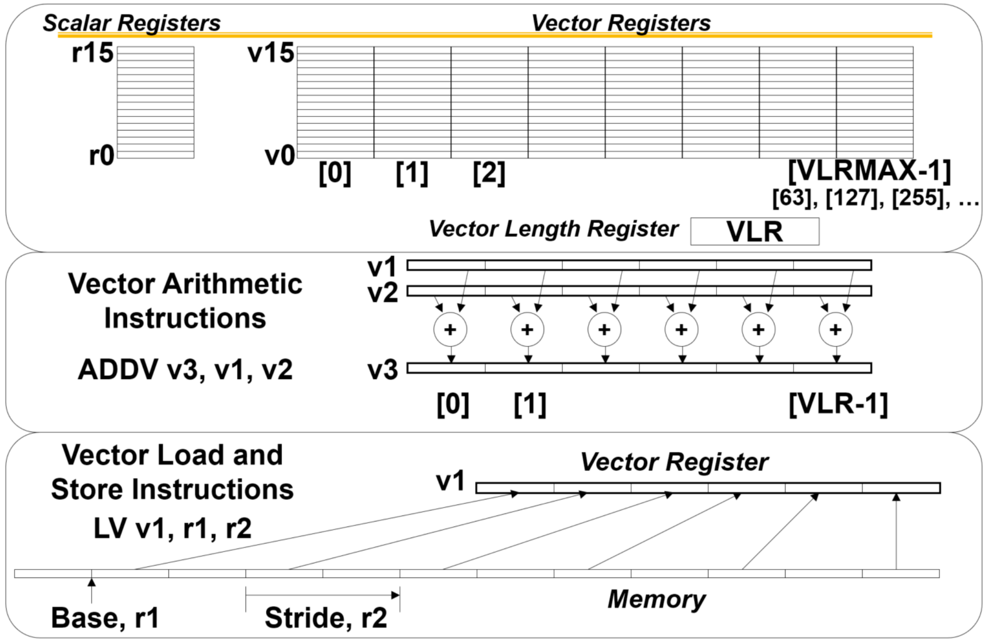
```
# Scalar Code
  LI     R4, 64
loop:
  L.D    F0, 0(R1)
  L.D    F2, 0(R2)
  ADD.D  F4, F2, F0
  S.D    F4, 0(R3)
  DADDIU R1, 8
  DADDIU R2, 8
  DADDIU R3, 8
  DSUBIU R4, 1
  BNEZ   R4, loop
```

```
# Vector Code
  LI     VLR, 64
  LV     V1, R1
  LV     V2, R2
  ADDV.D V3, V1, V2
  SV     V3, R3
```

Vector Processors

GPUs: same basic idea





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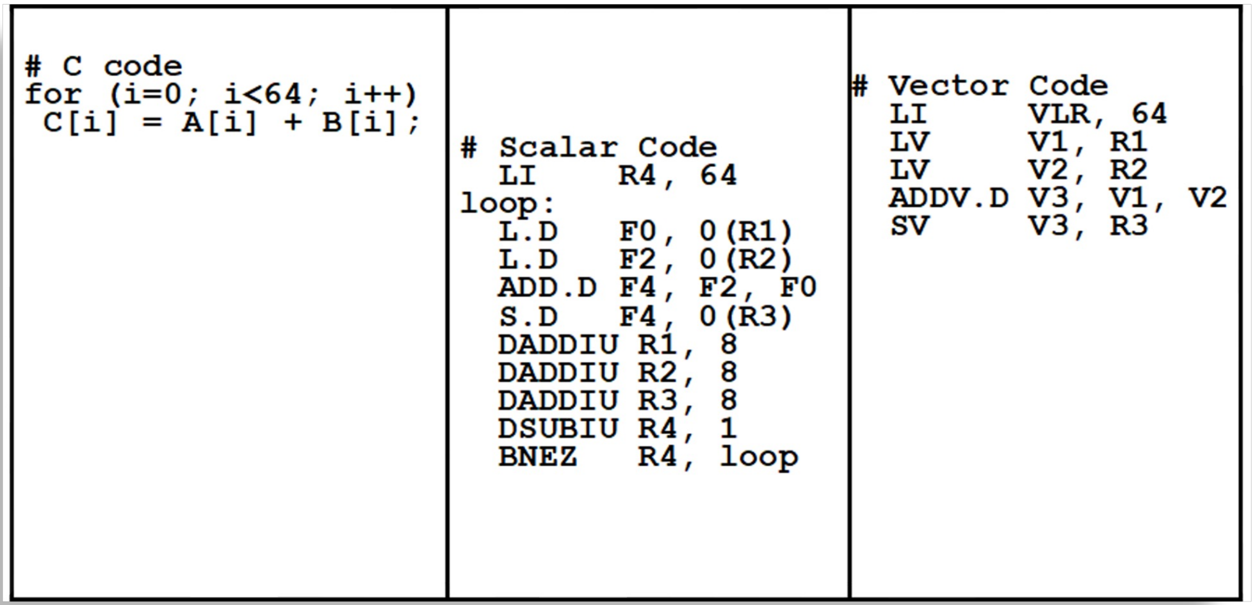

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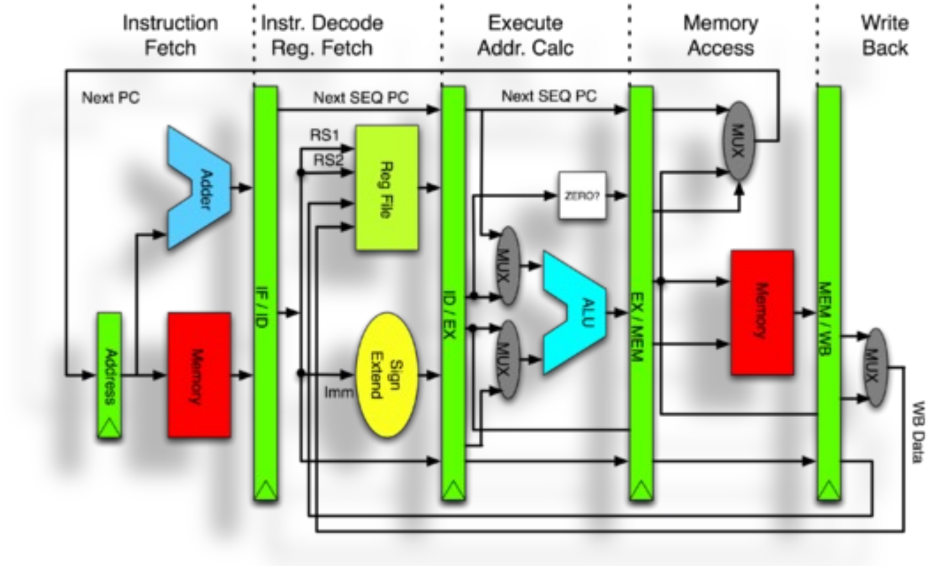
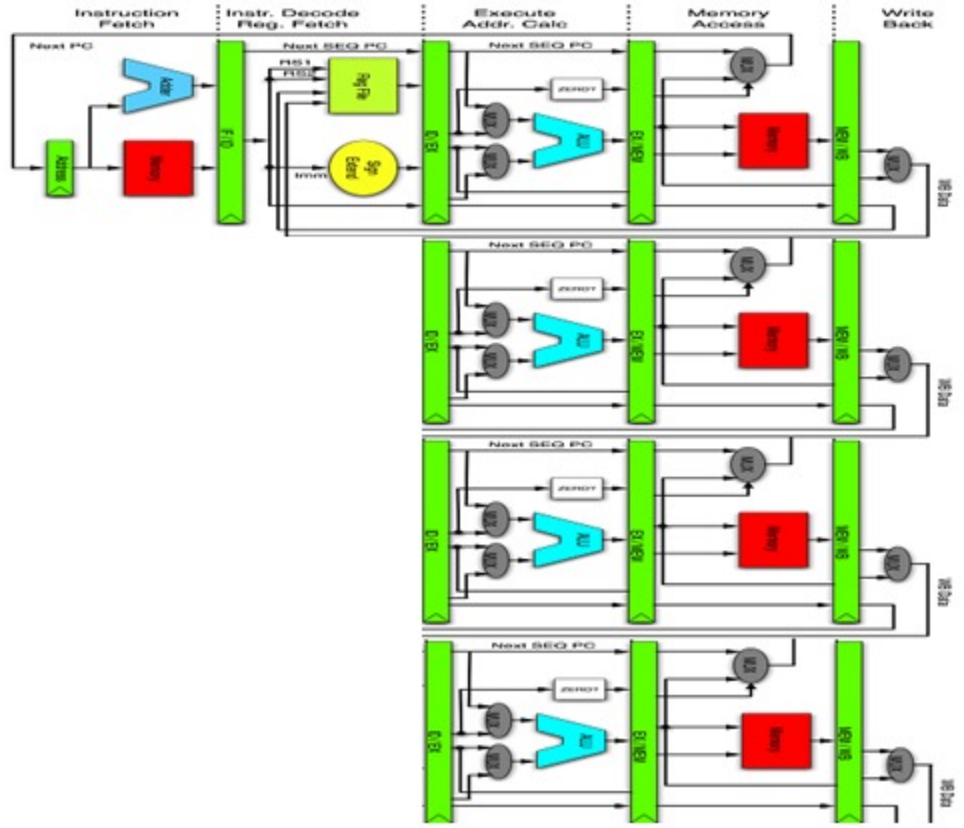
When does vector processing help?





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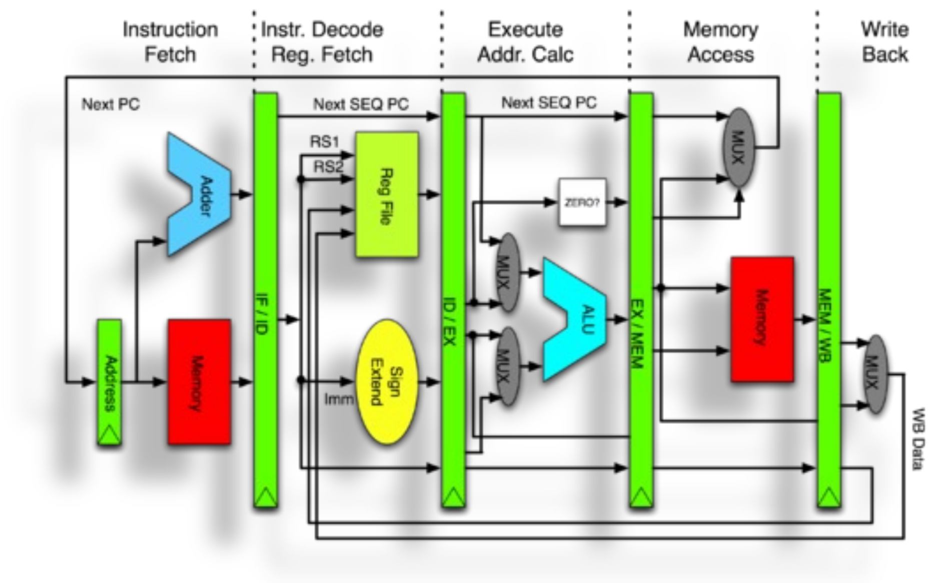
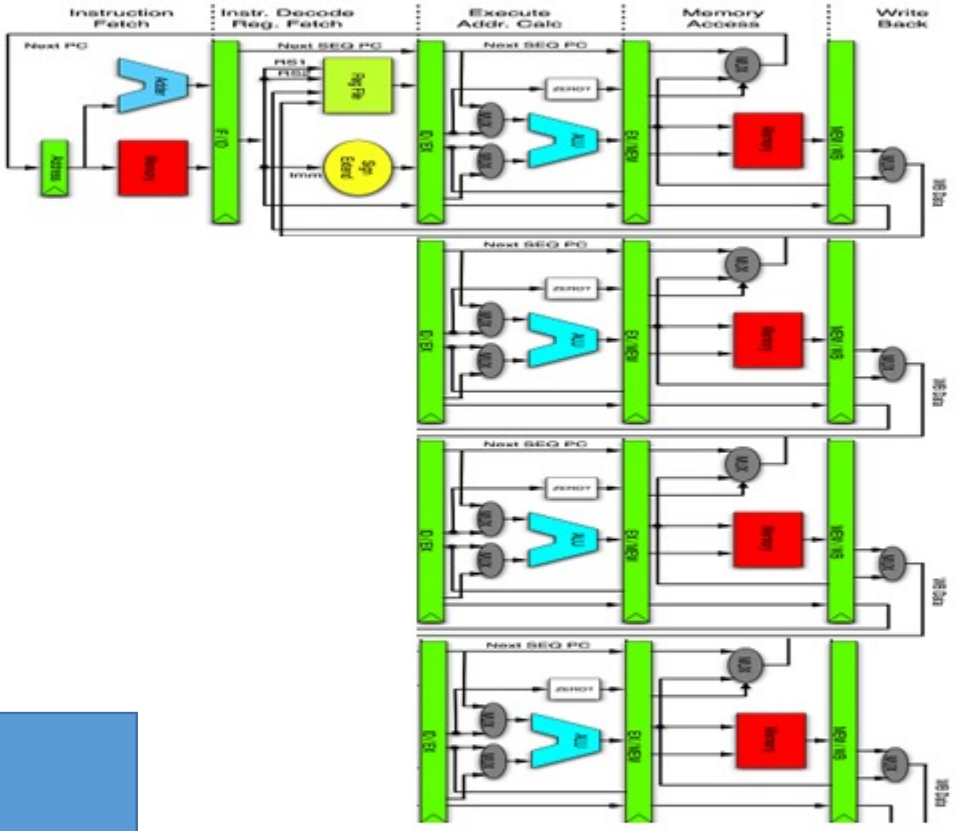
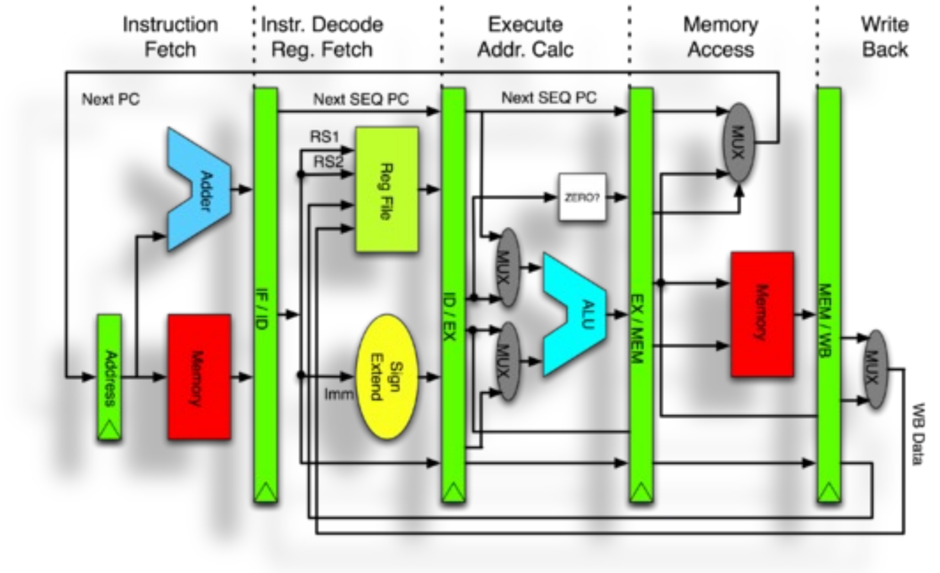
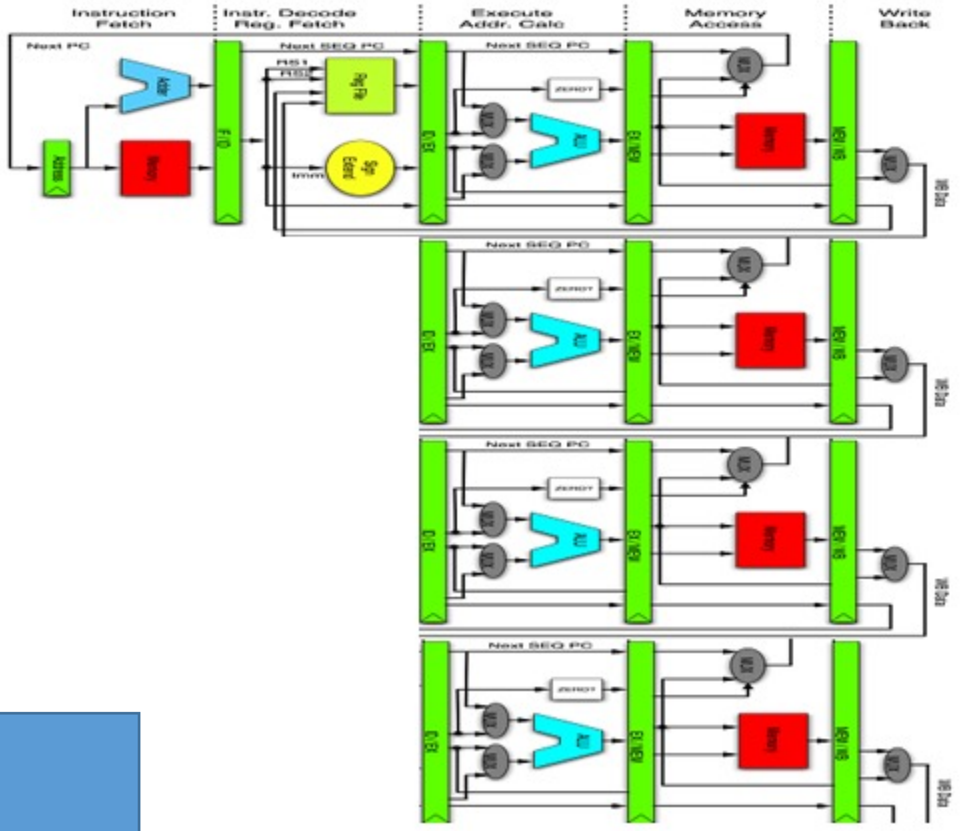




What are the potential bottlenecks here?
When can it improve throughput?

When does vector processing help?





What are the potential bottlenecks here?
When can it improve throughput?

Only helps if memory can keep the pipeline busy!

Hardware multi-threading

Hardware multi-threading

- Address memory bottleneck

Hardware multi-threading

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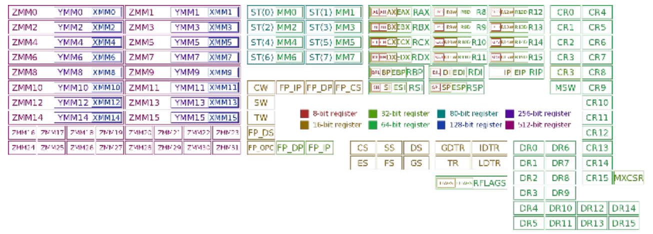
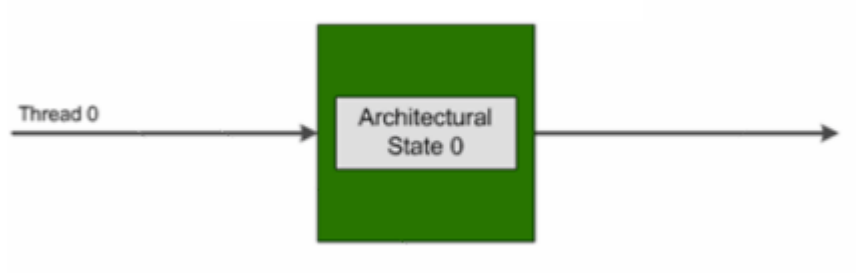
- Share exec unit across
  - Instruction streams
  - Switch on stalls

Hardware multi-threading





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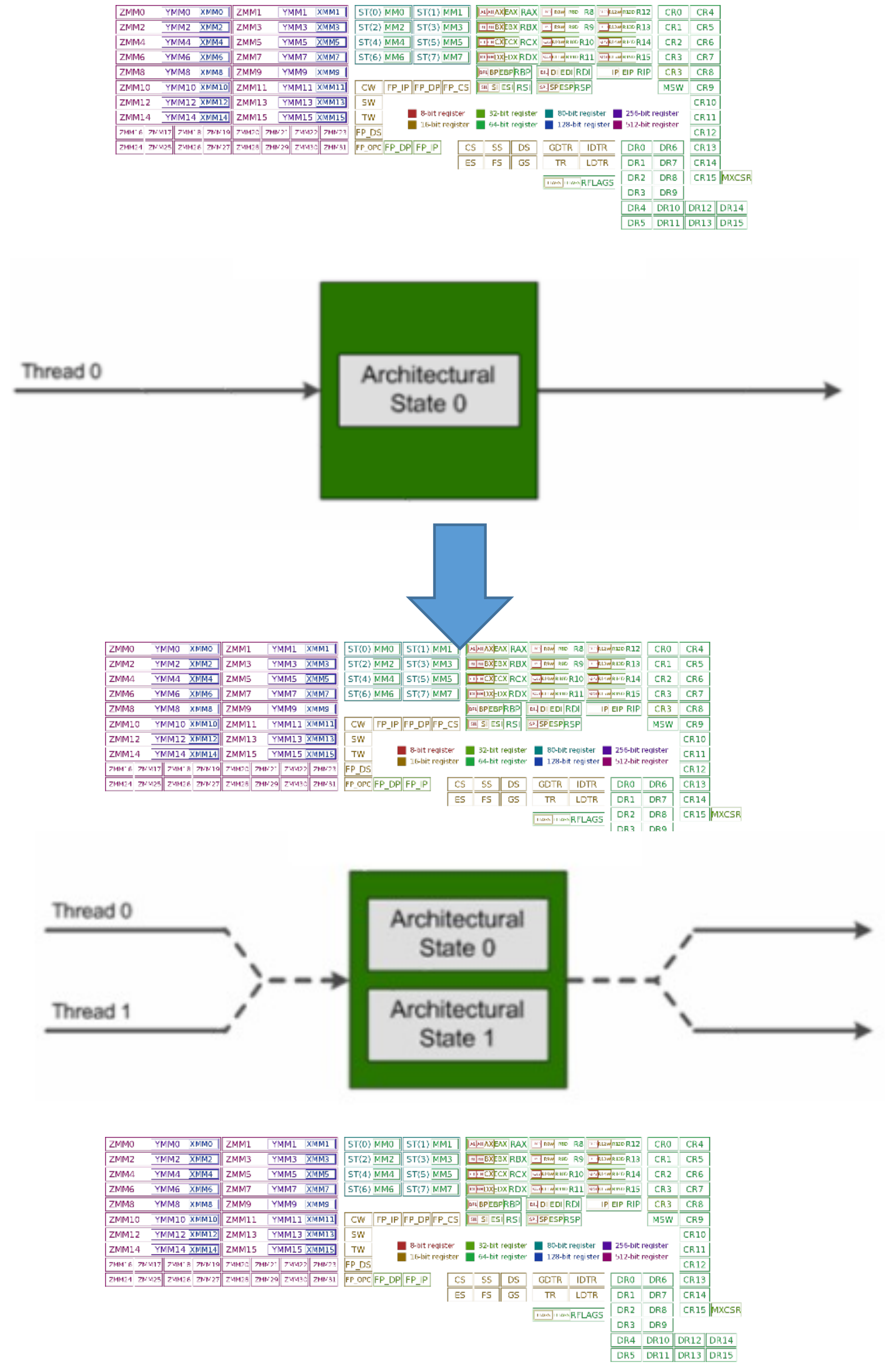

Hardware multi-threading

- Address memory bottleneck
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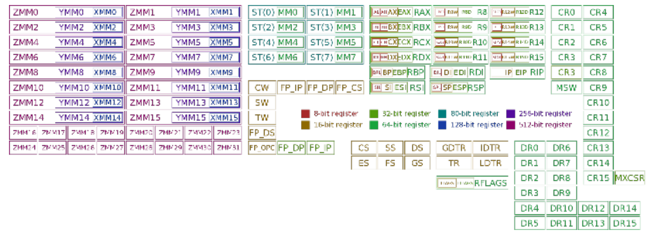
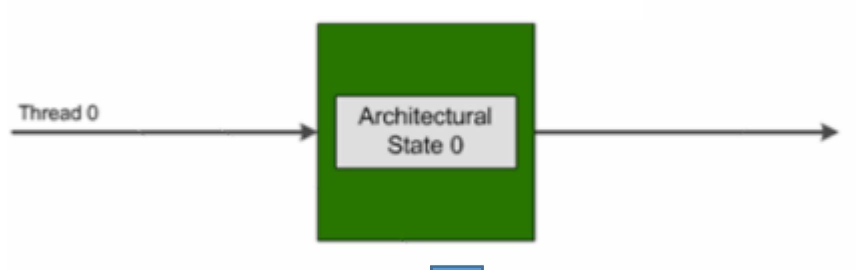
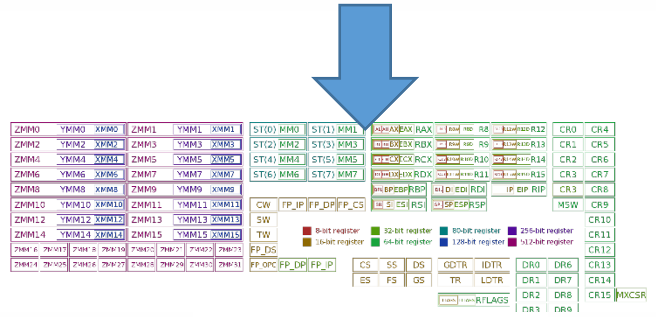
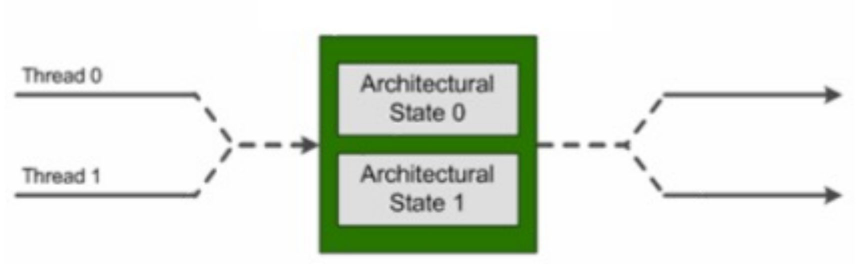
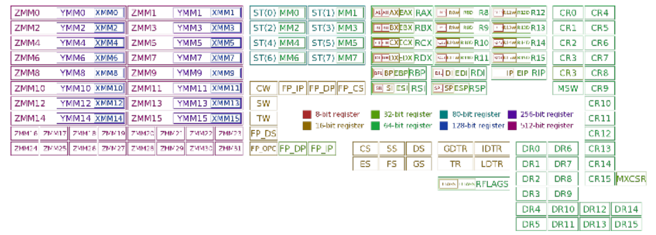
  - Switch on stalls
- Looks like multiple cores to the OS





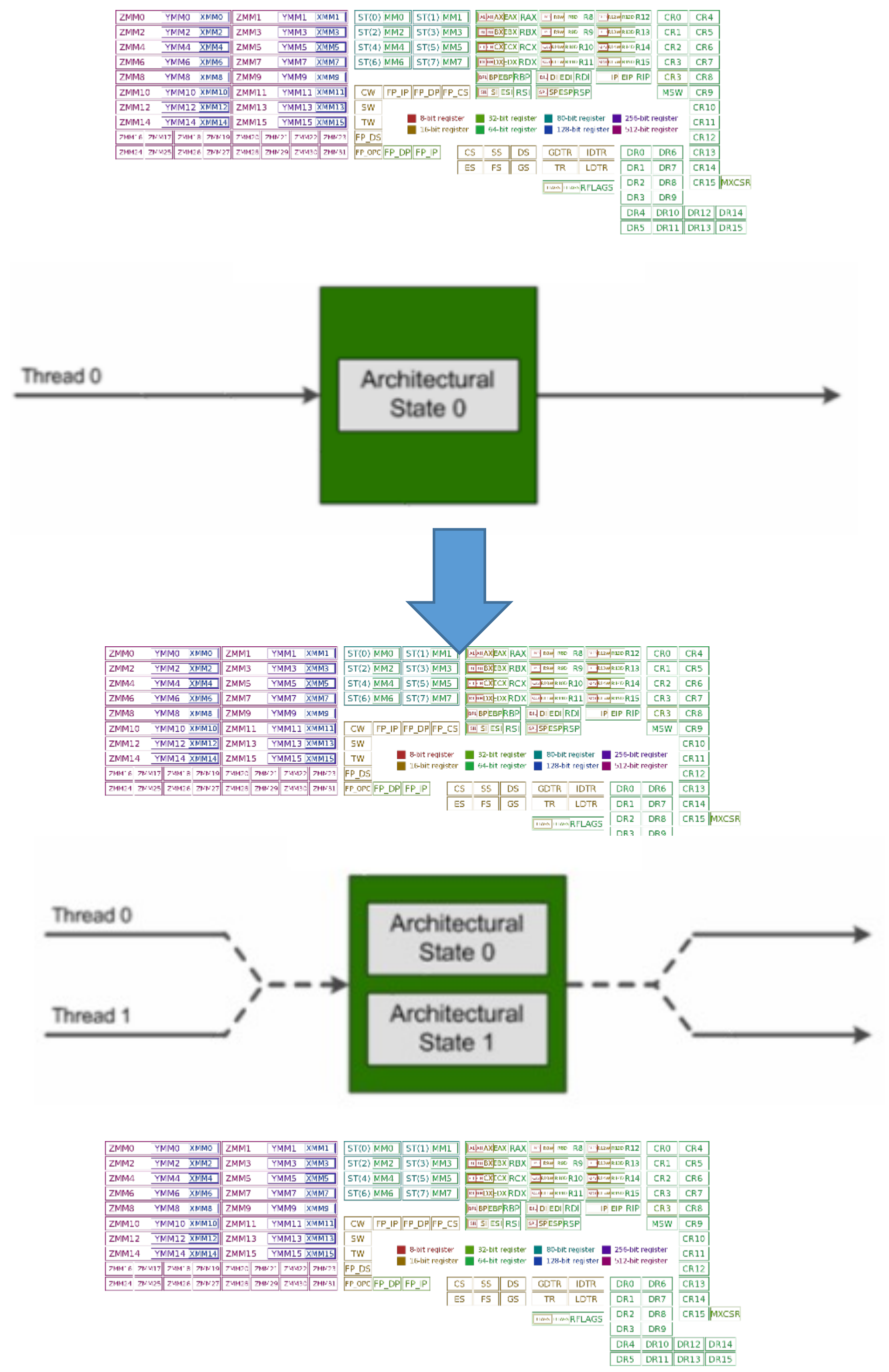




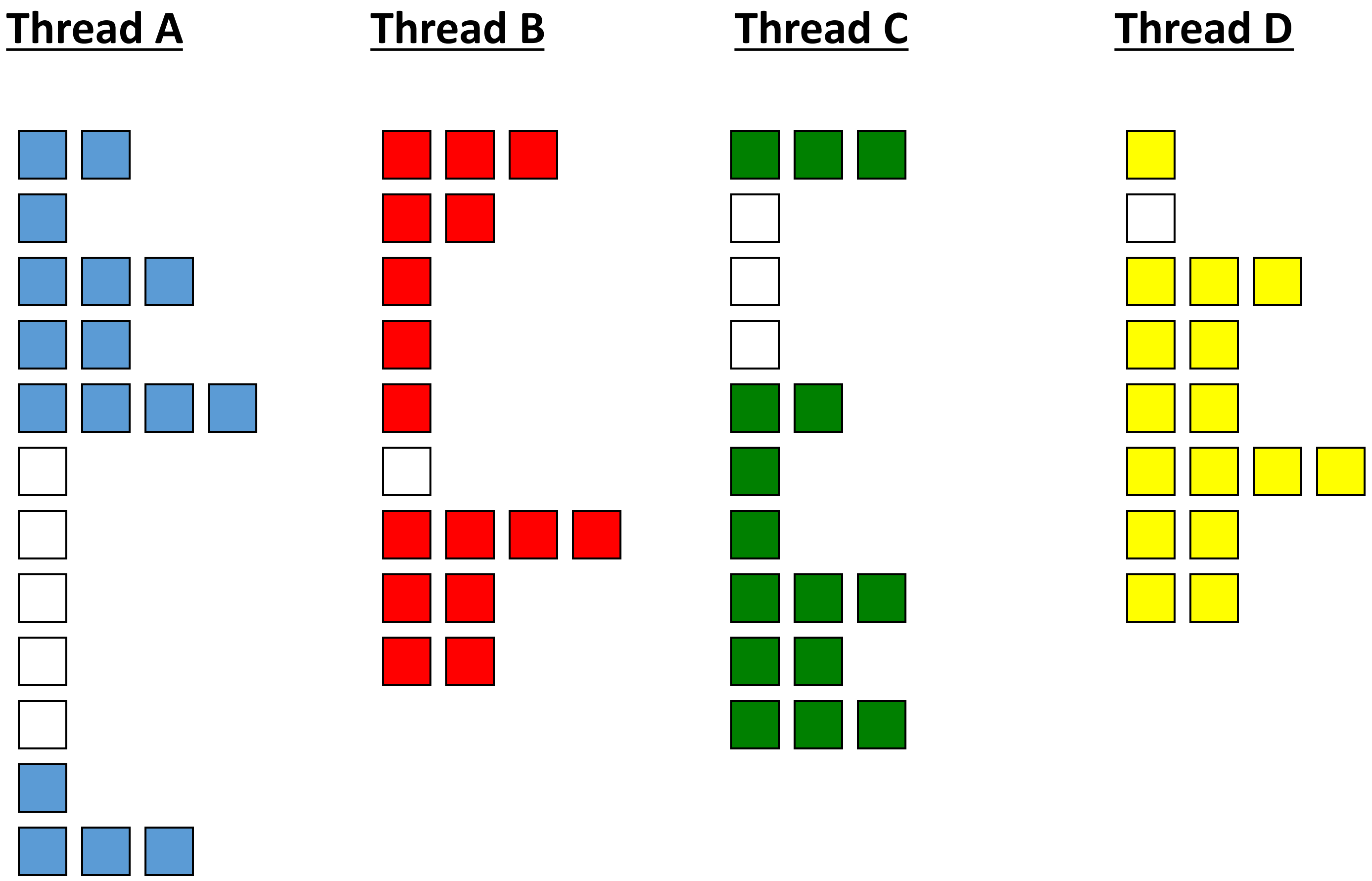


Hardware multi-threading

- Address memory bottleneck
- Share exec unit across
  - Instruction streams
  - Switch on stalls
- Looks like multiple cores to the OS
- Three variants:
  - Coarse
  - Fine-grain
  - Simultaneous



Running example



- Colors → pipeline full
- White → stall

Coarse- grained multithreading

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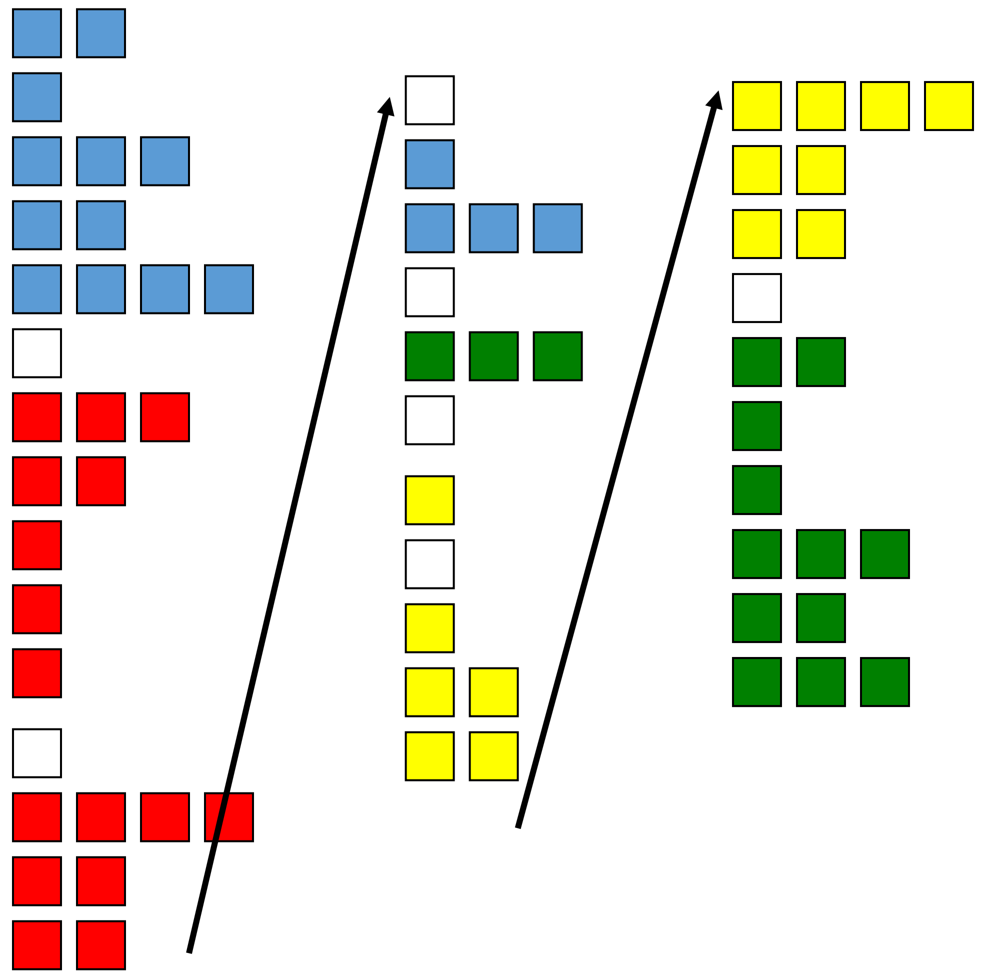

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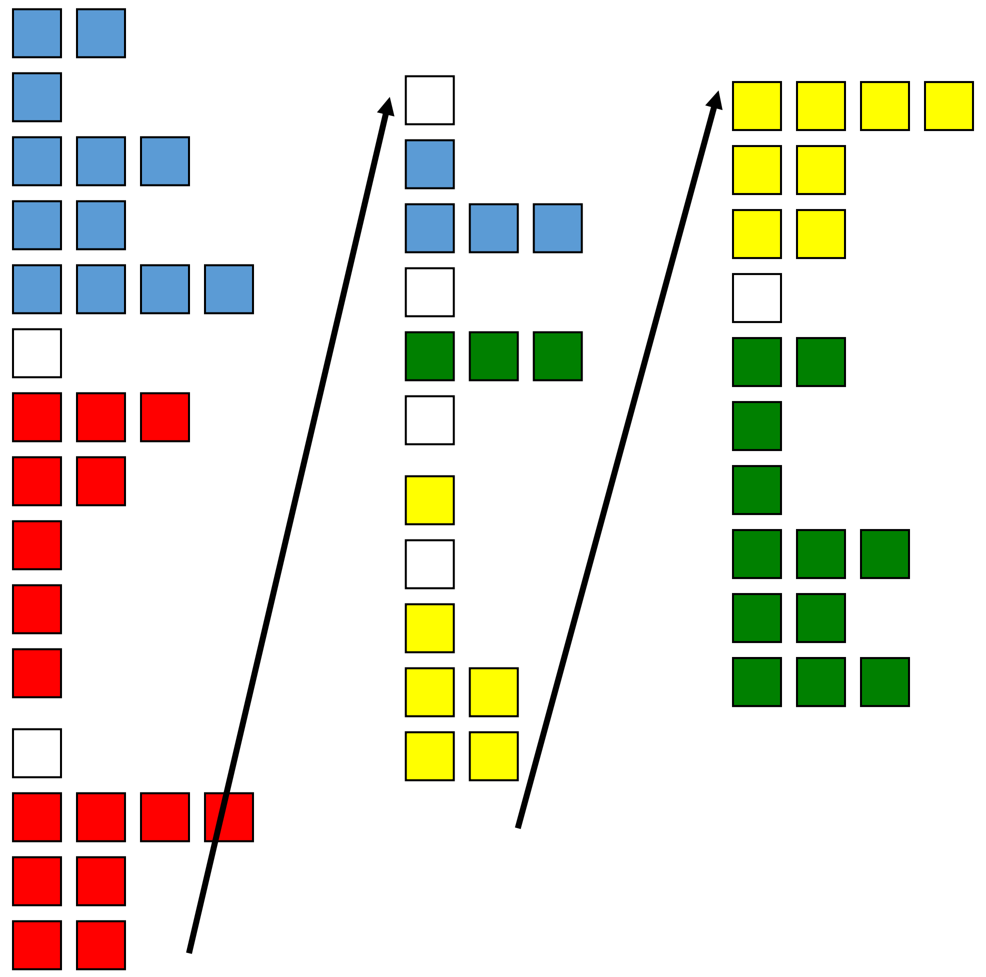

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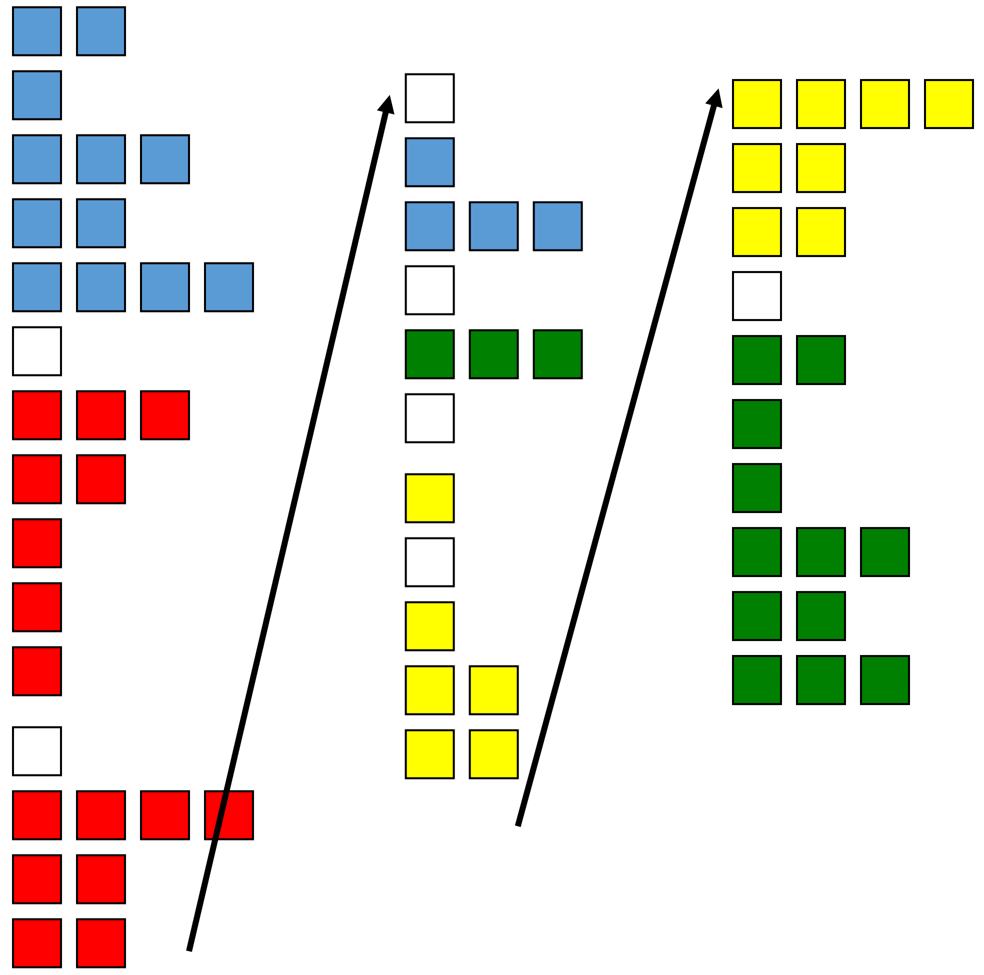

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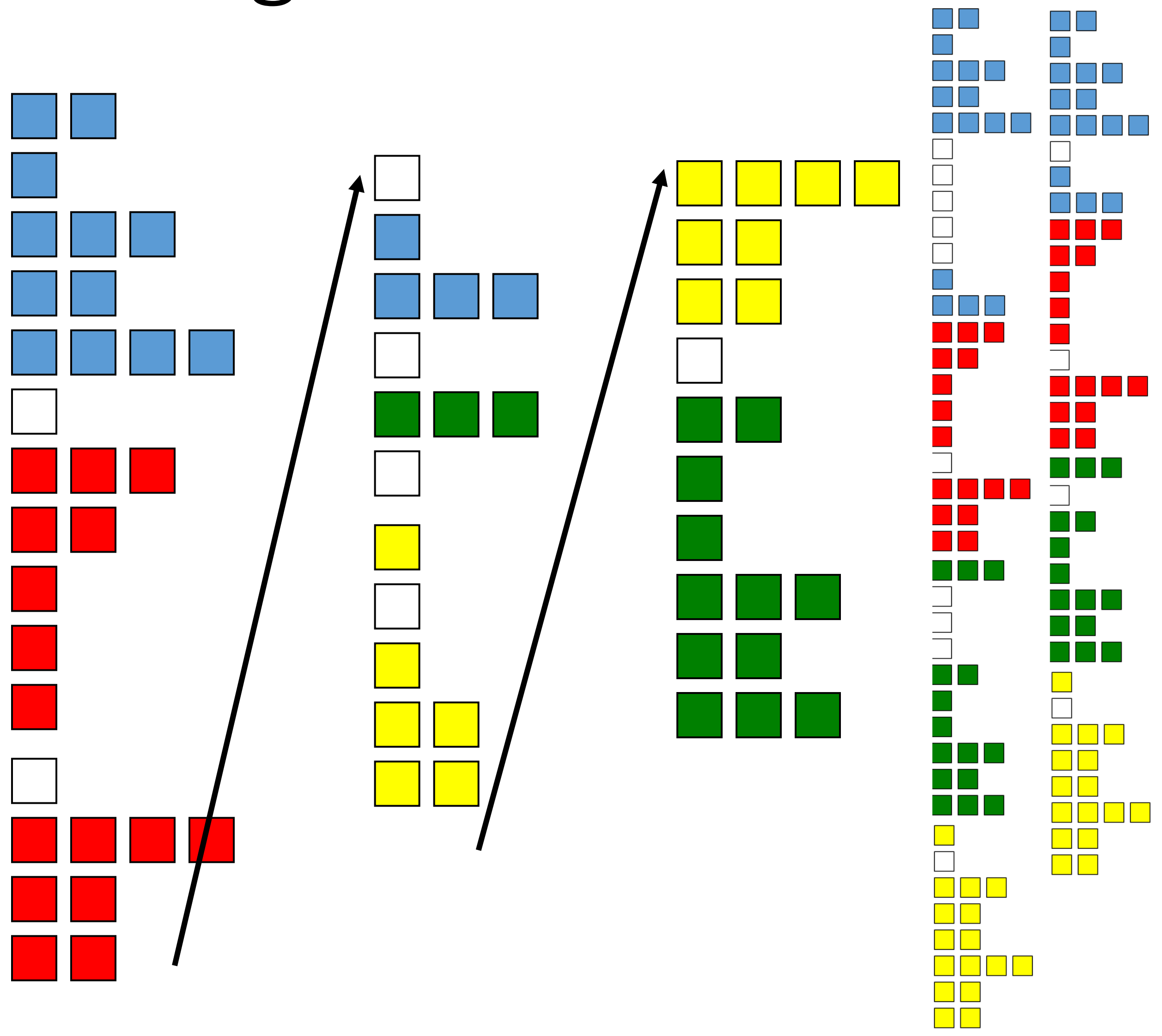

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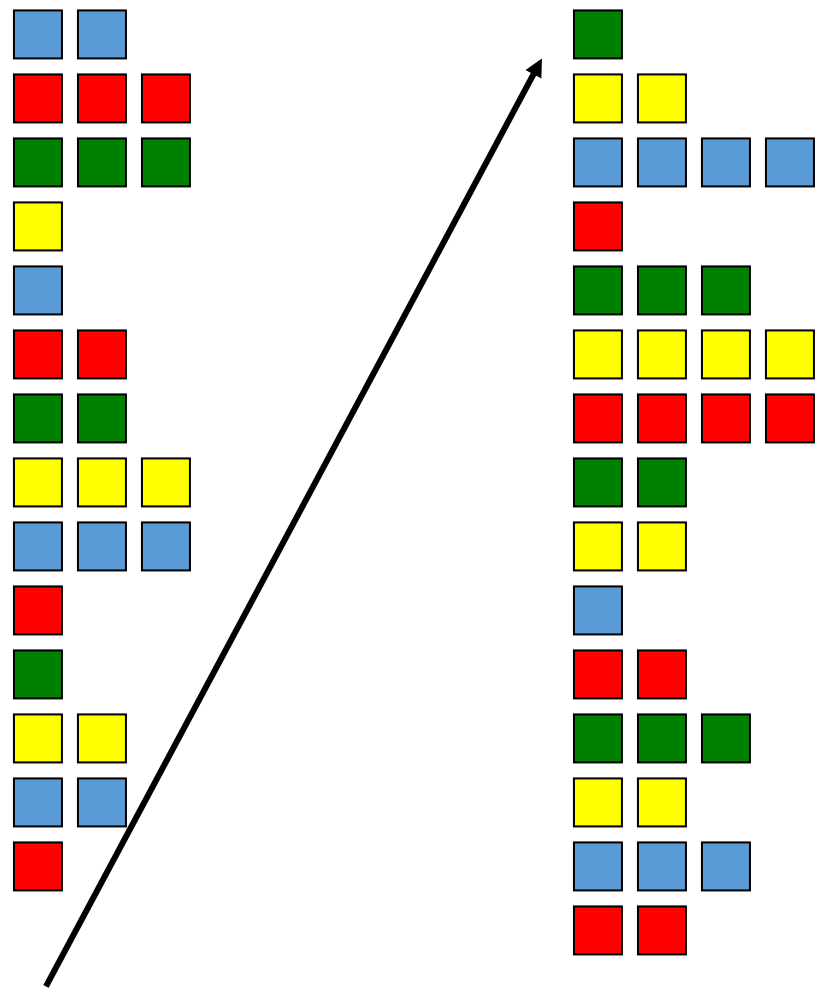

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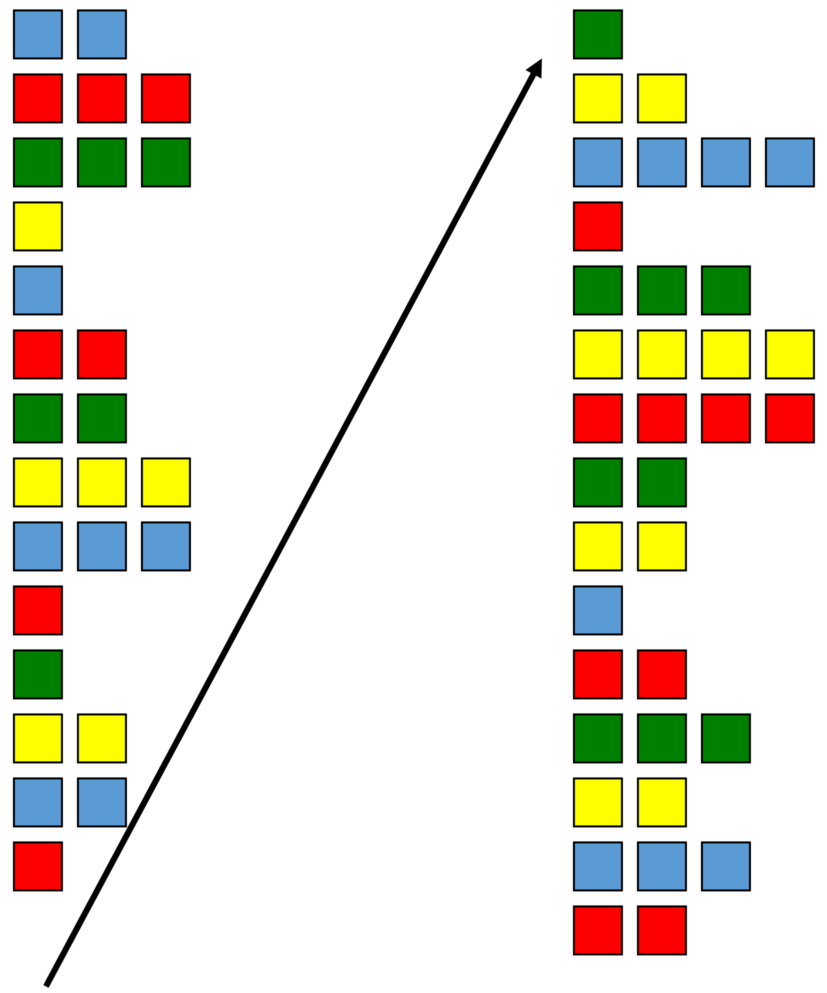

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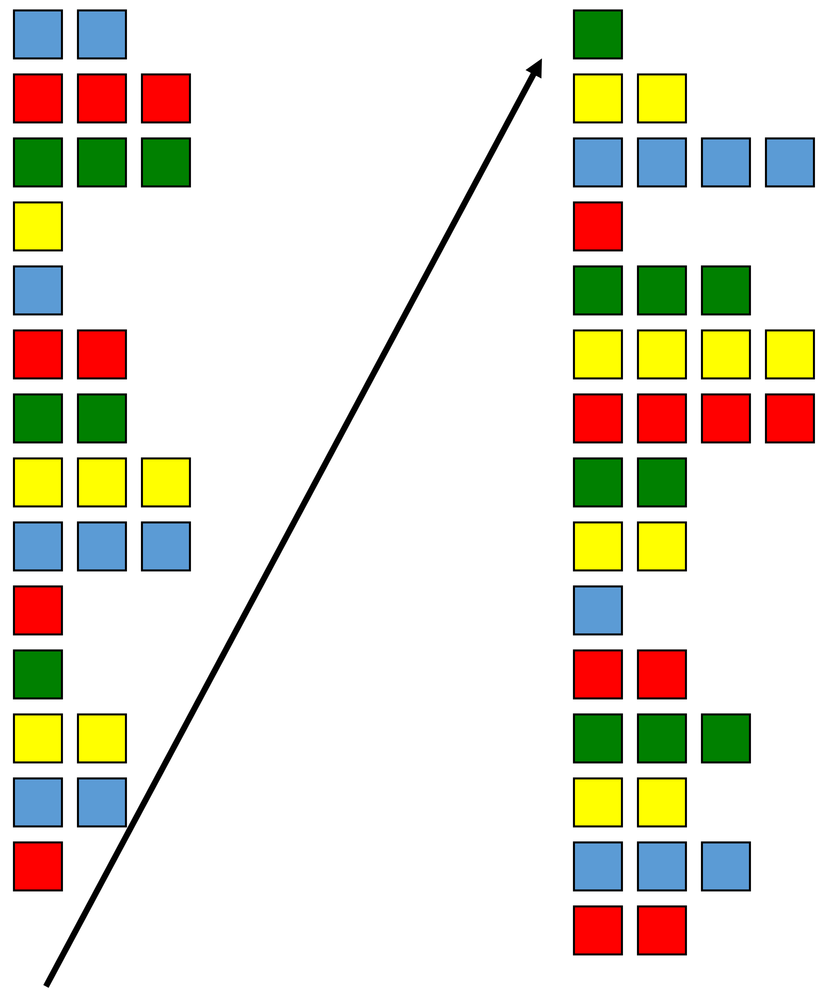

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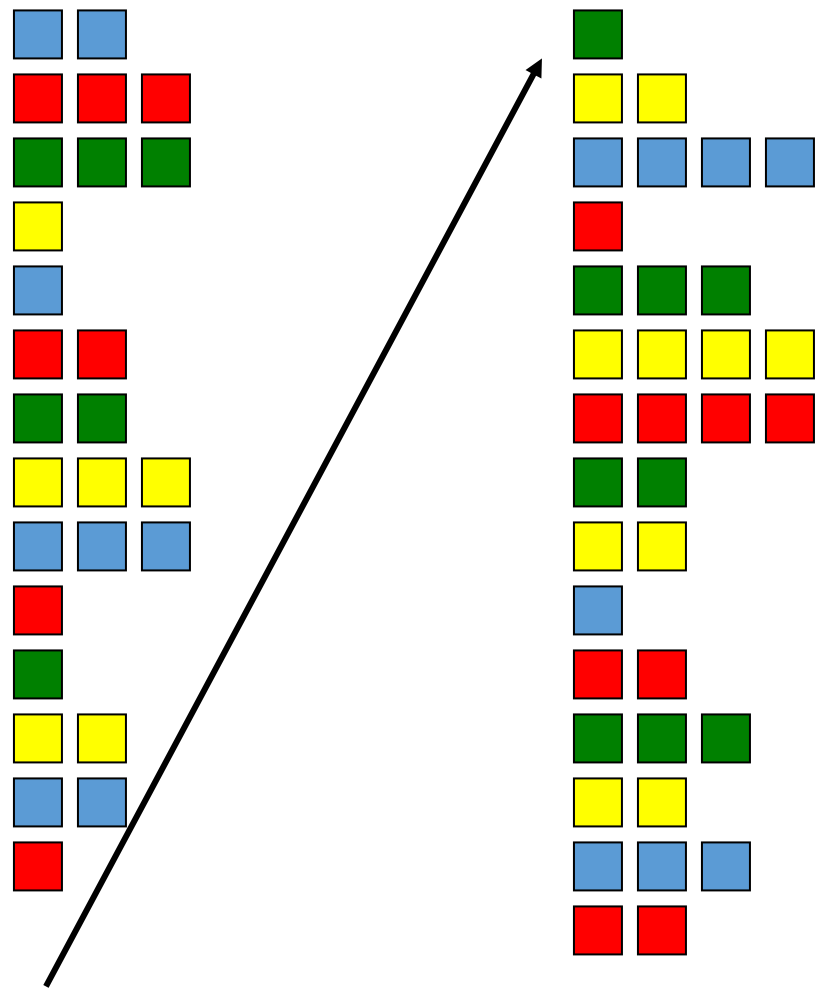

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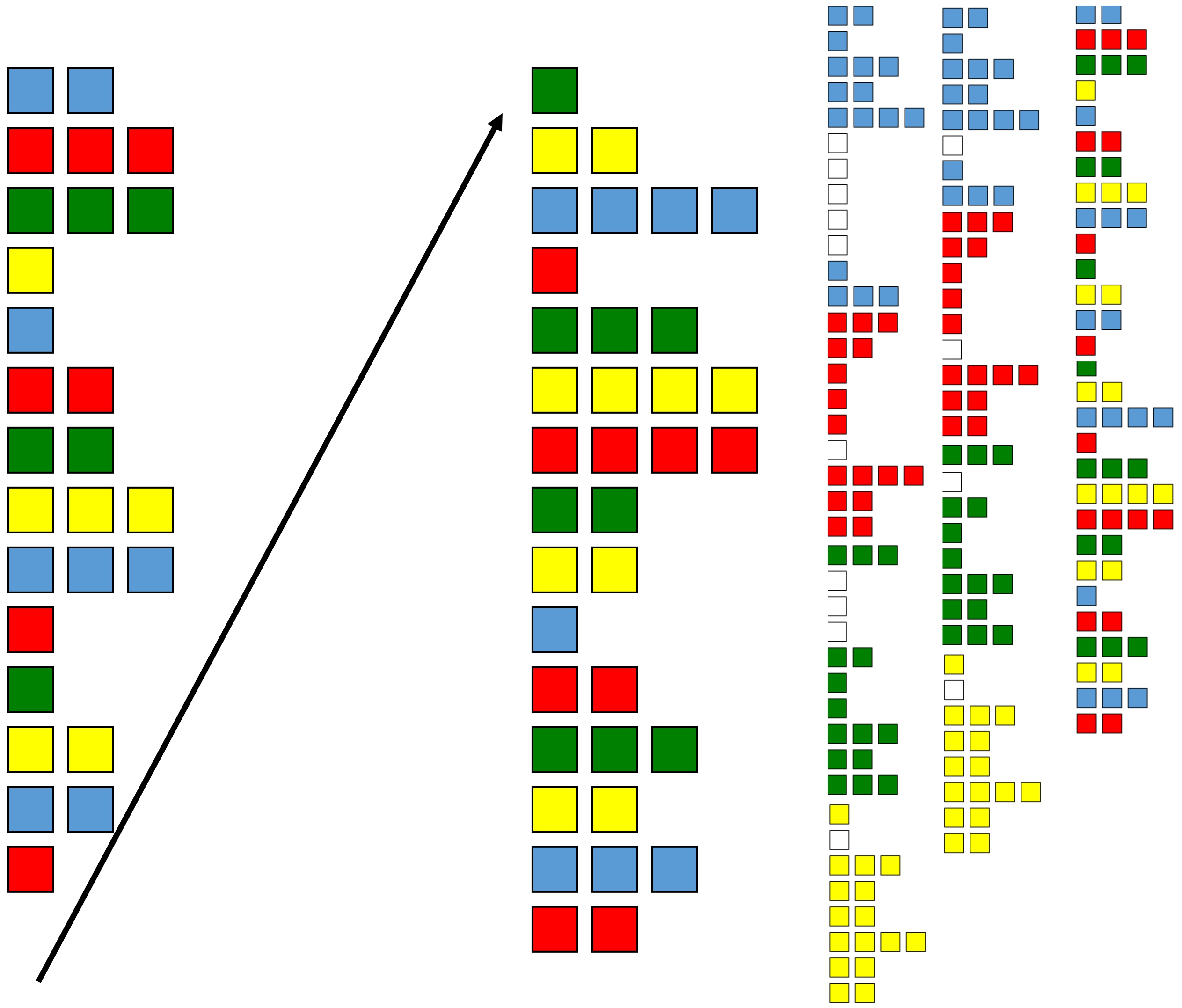

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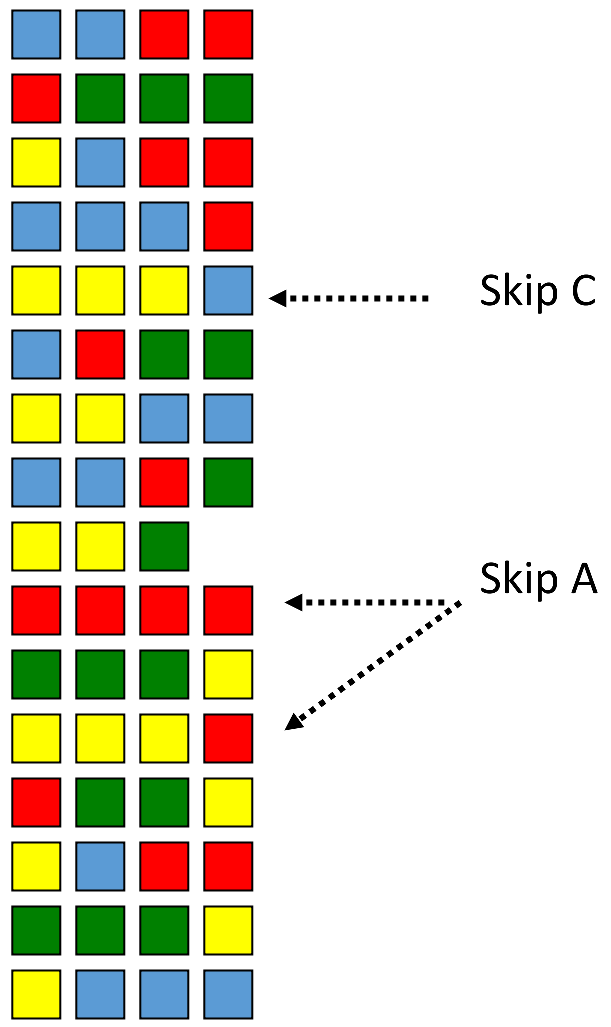

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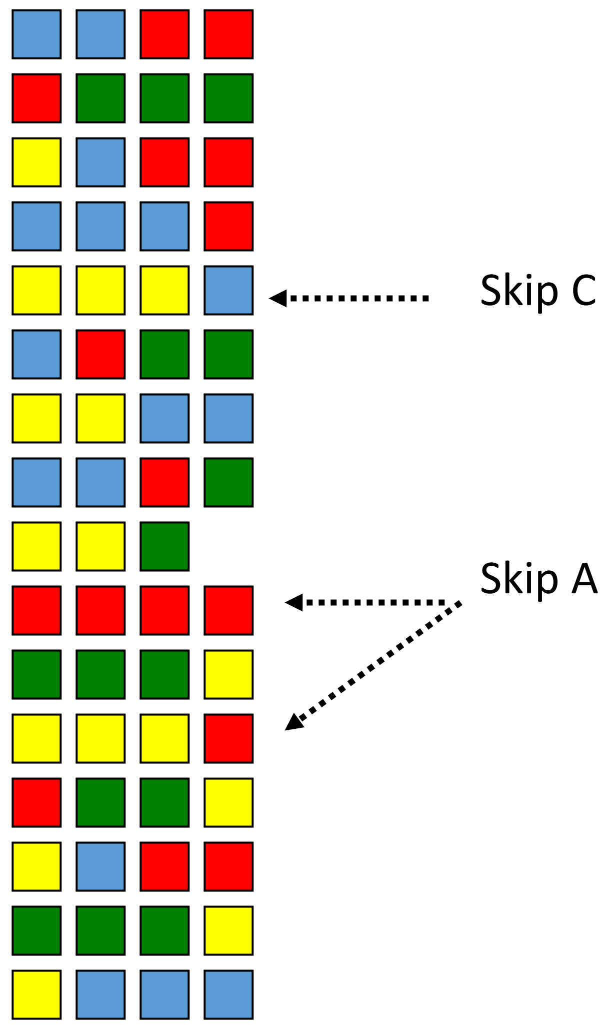

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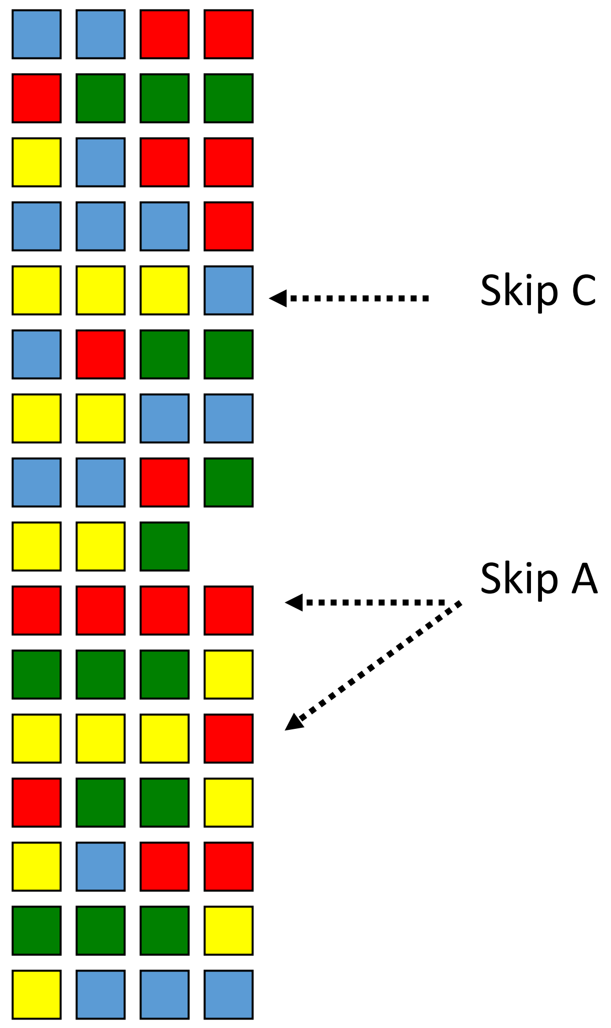

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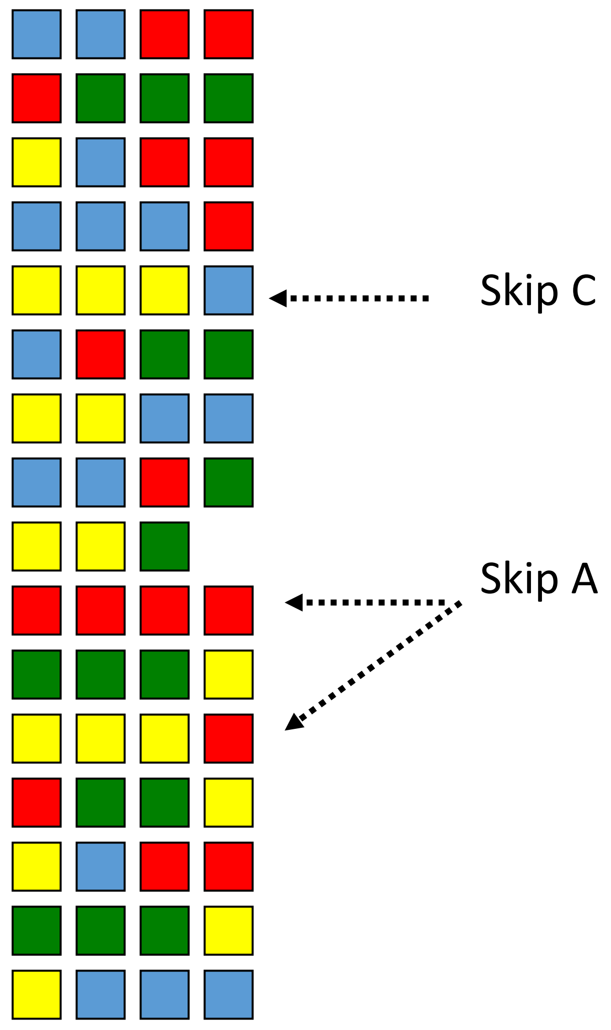

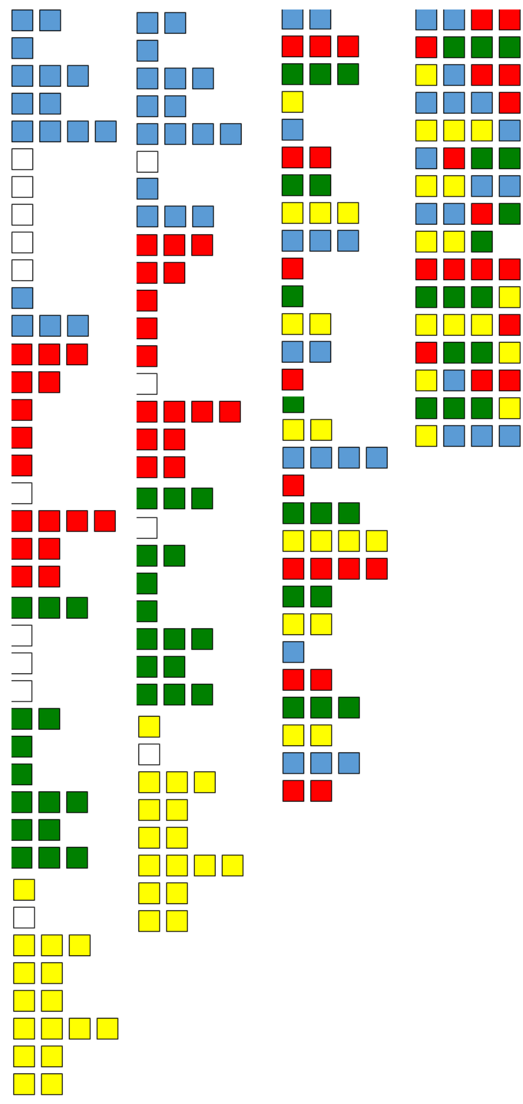

Why Vector and Multithreading Background?

GPU:

- A very wide vector machine
- Massively multi-threaded to hide memory latency
- Originally designed for graphics pipelines…

Graphics ~= Rendering

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Inputs

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  - Geometry modeled w triangle meshes, surface normals
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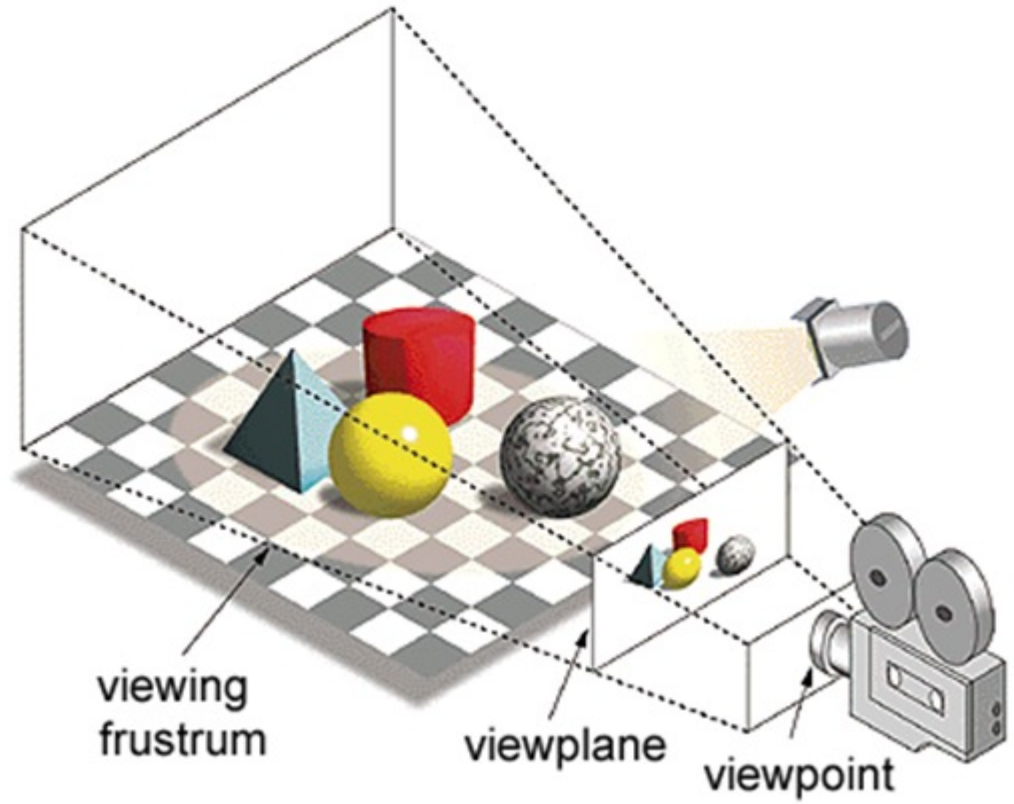

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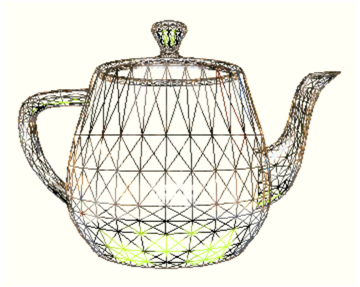

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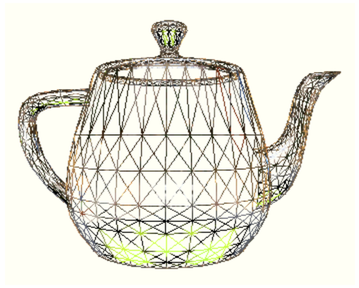

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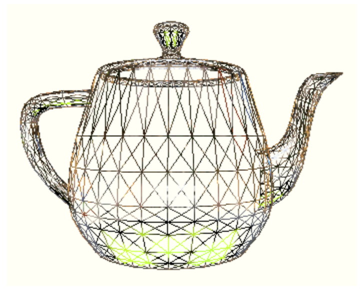

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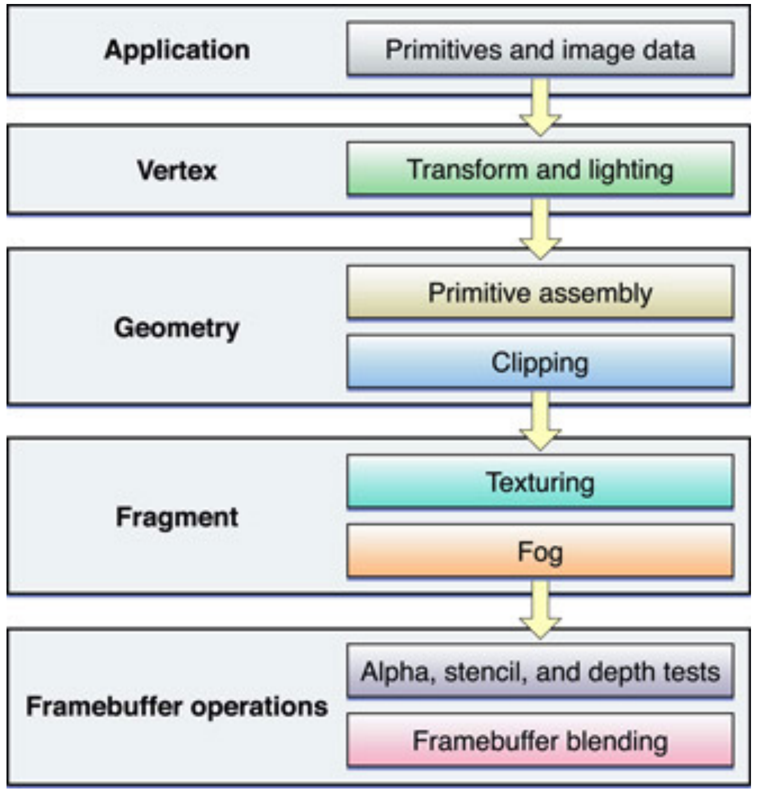

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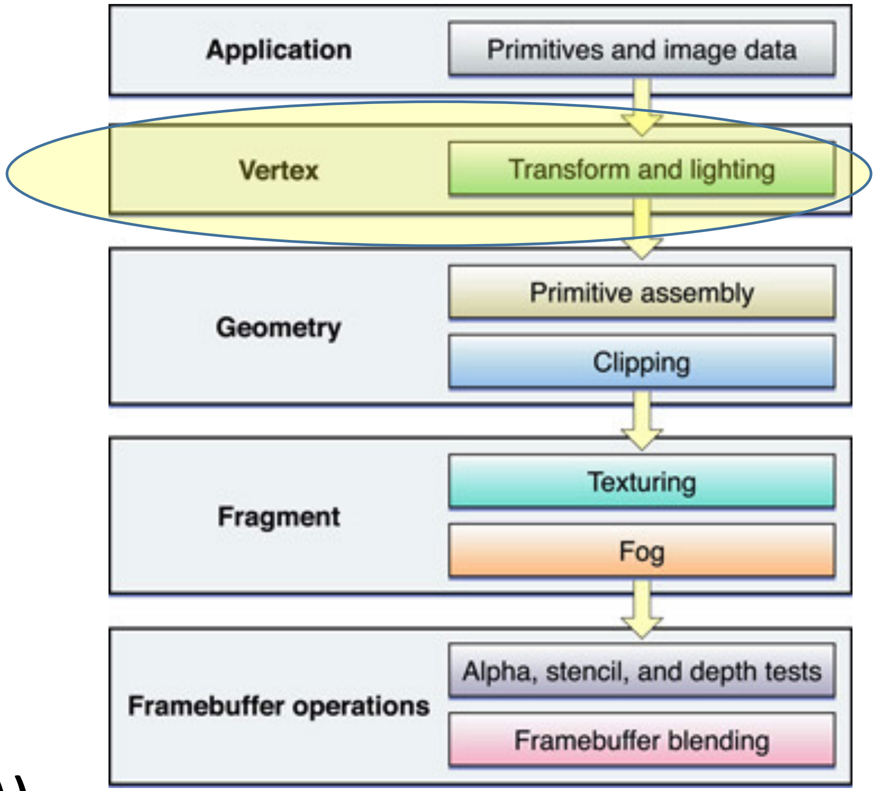

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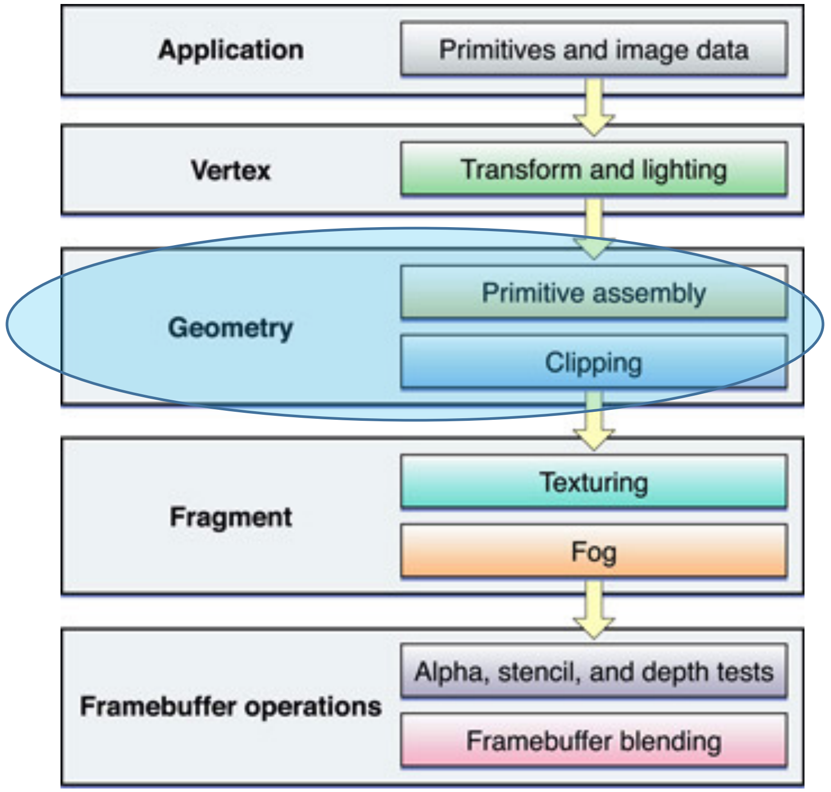

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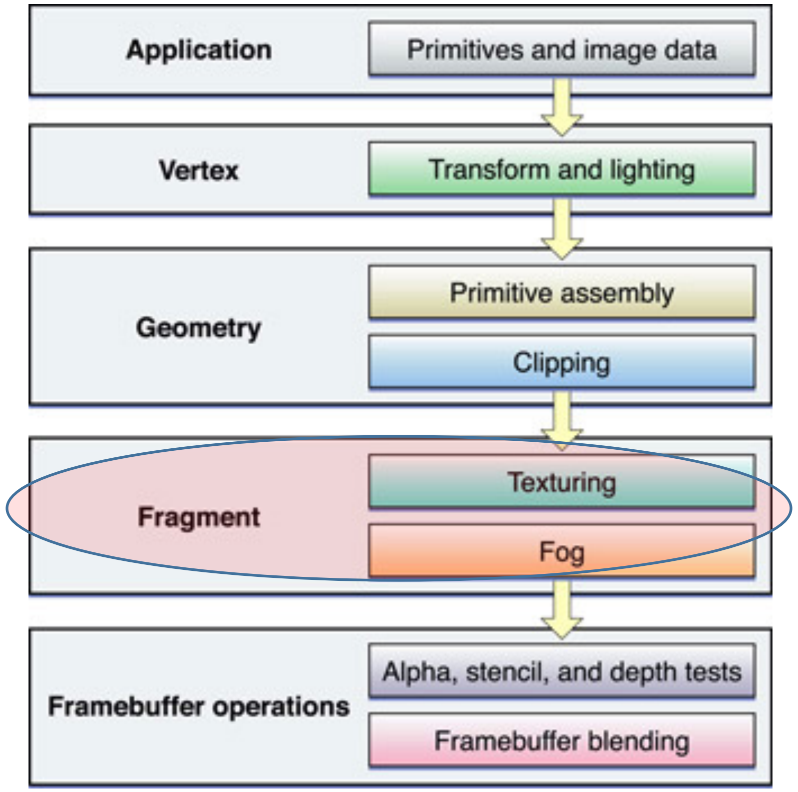

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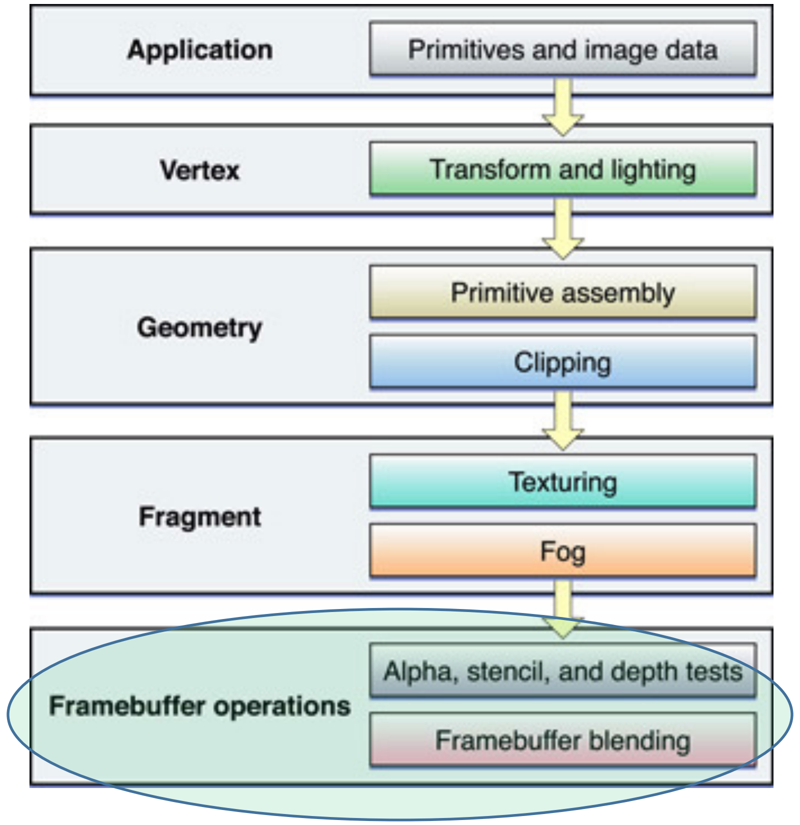

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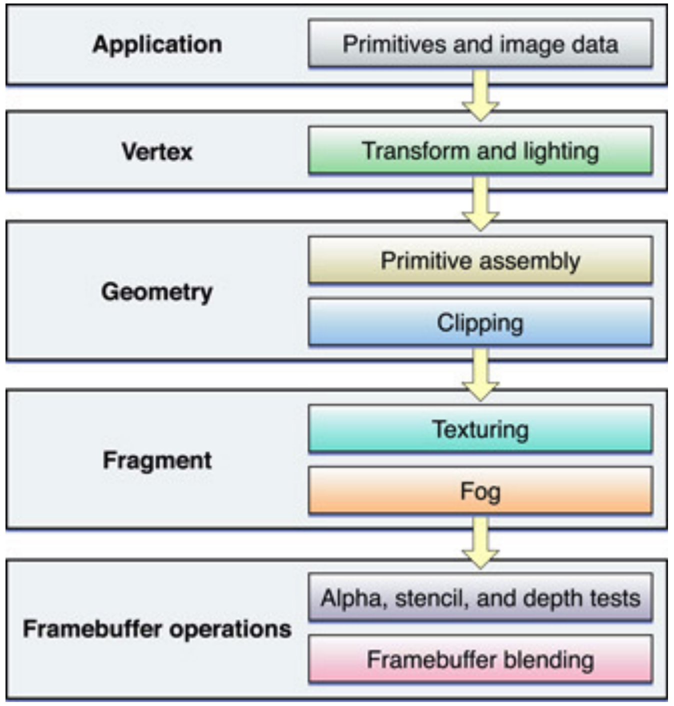
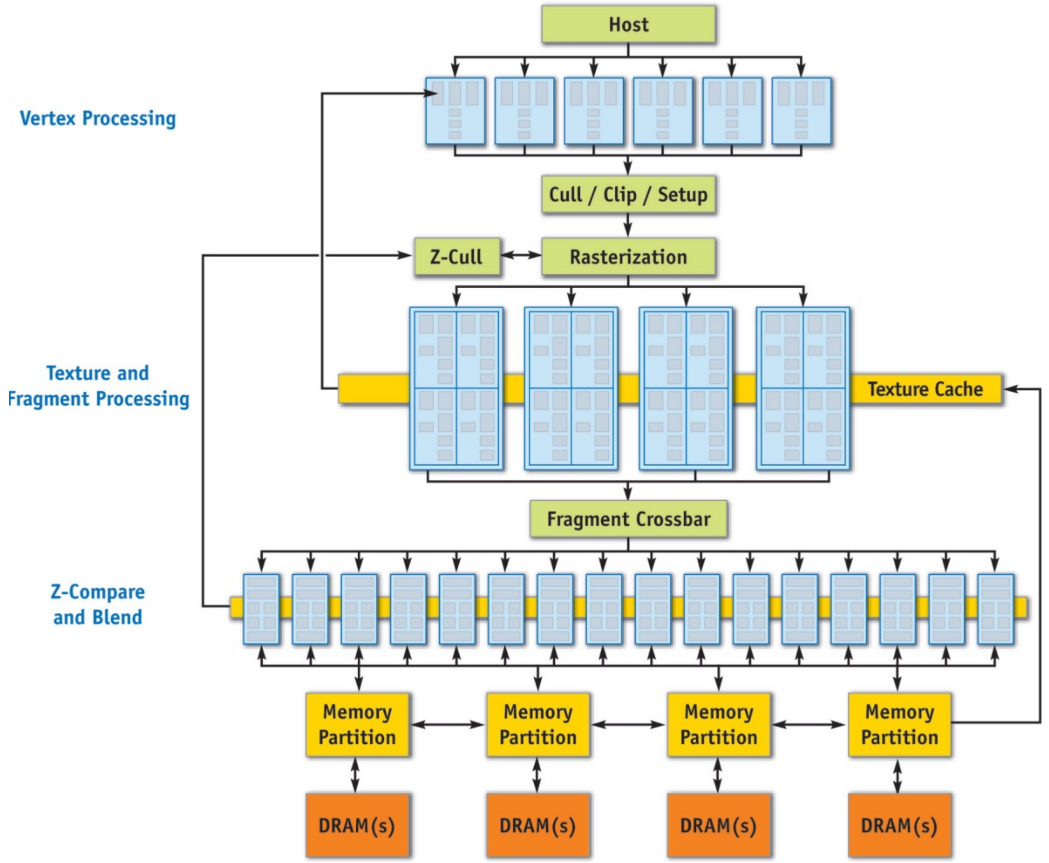
Graphics pipeline → GPU architecture

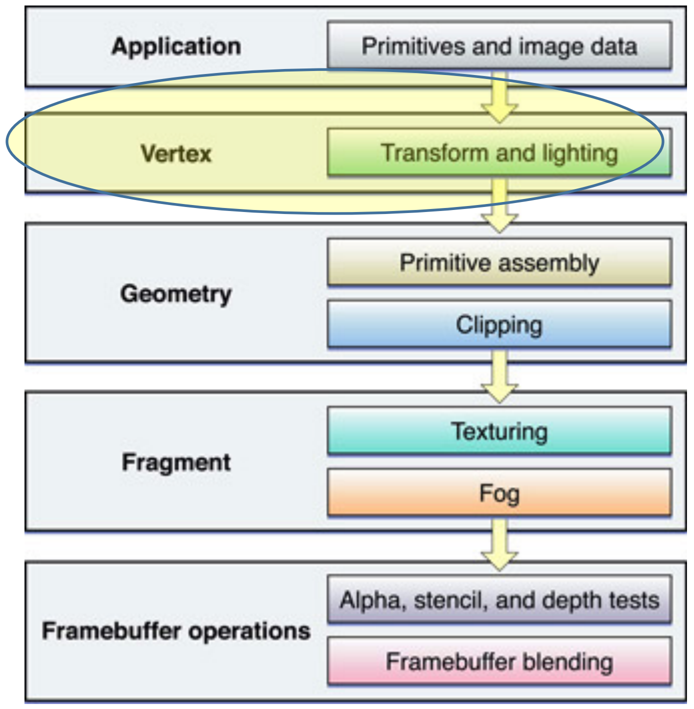


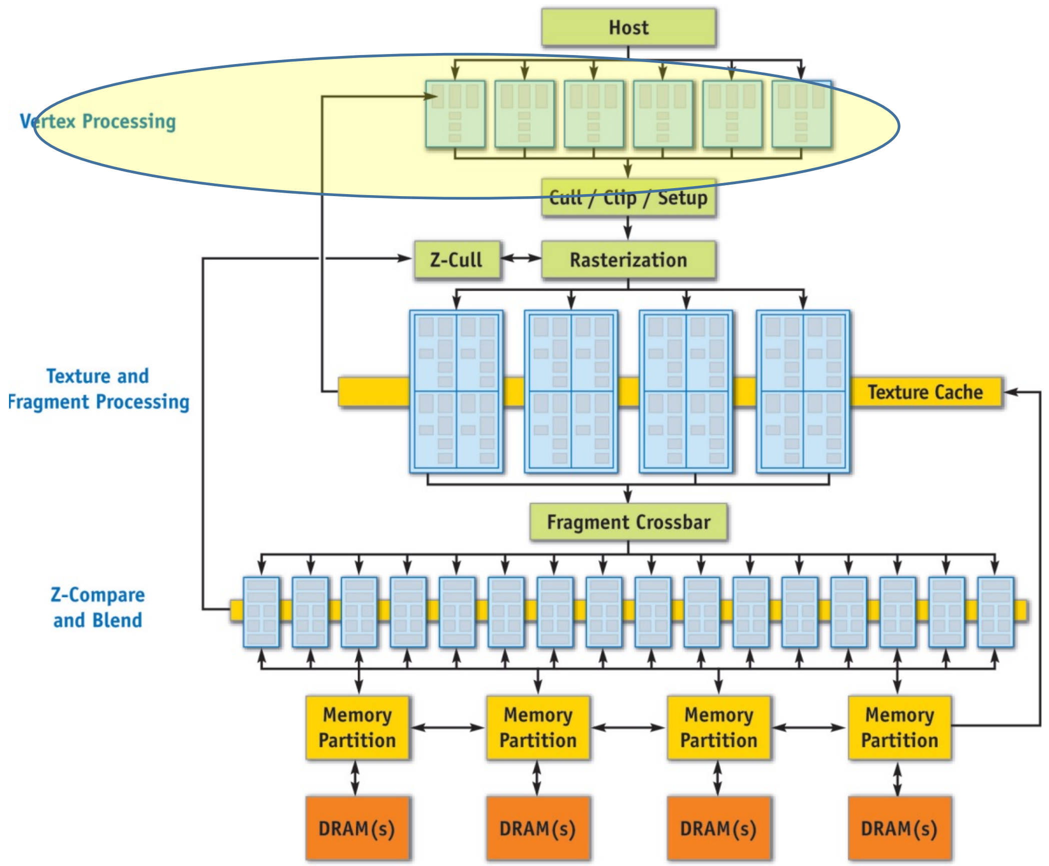


Limited "programmability" of shaders:
Minimal/no control flow
Maximum instruction count

GeForce 6 series

Graphics pipeline → GPU architecture





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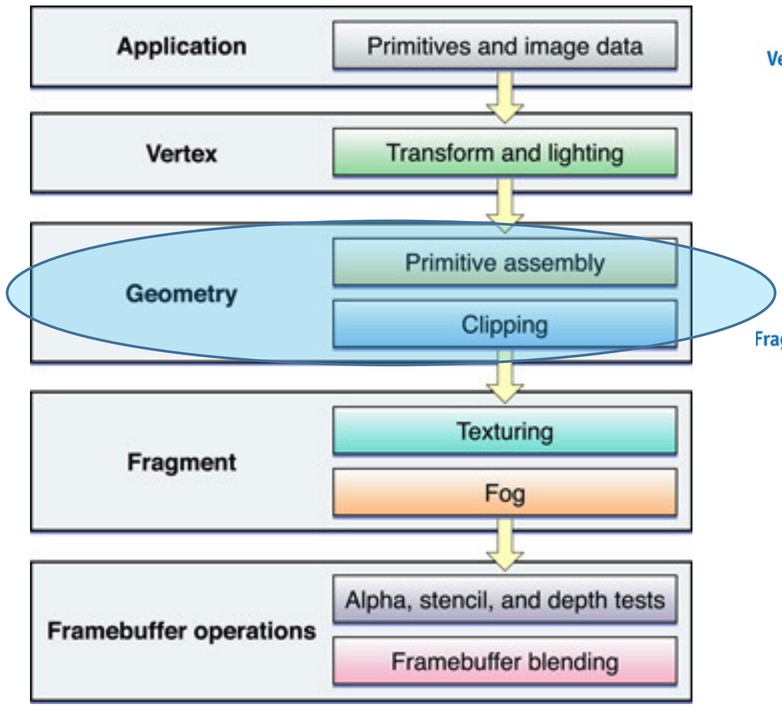

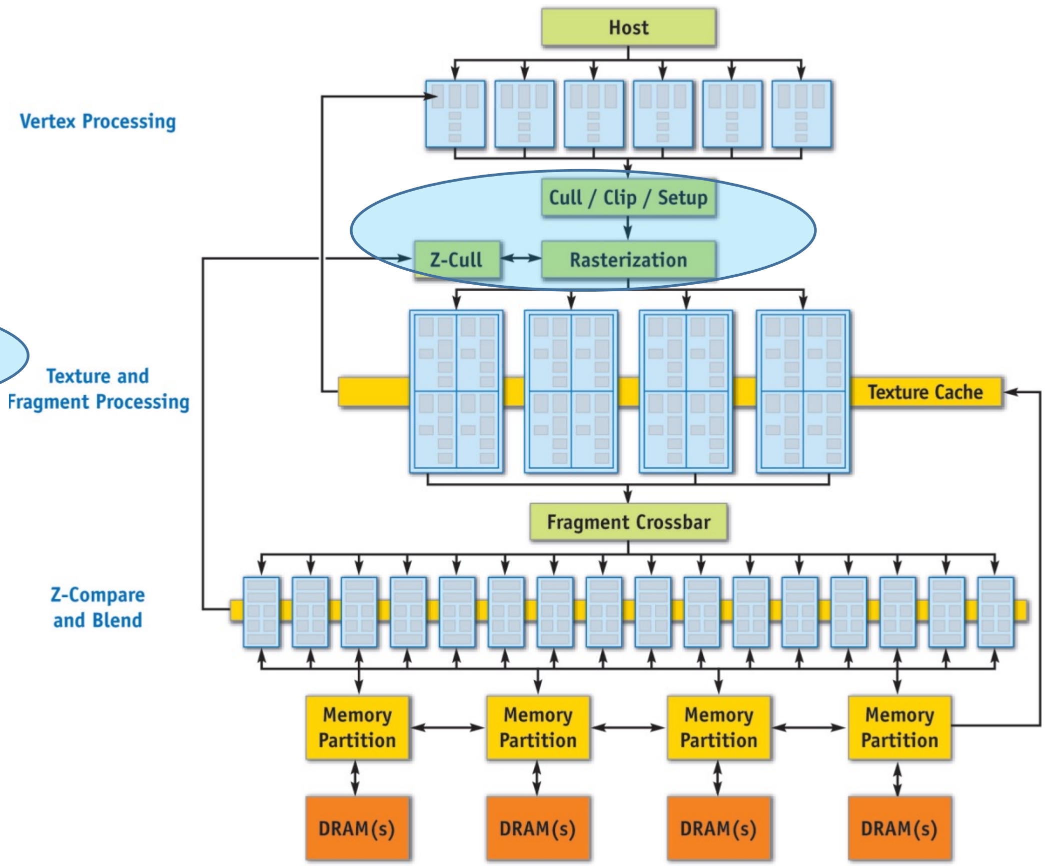

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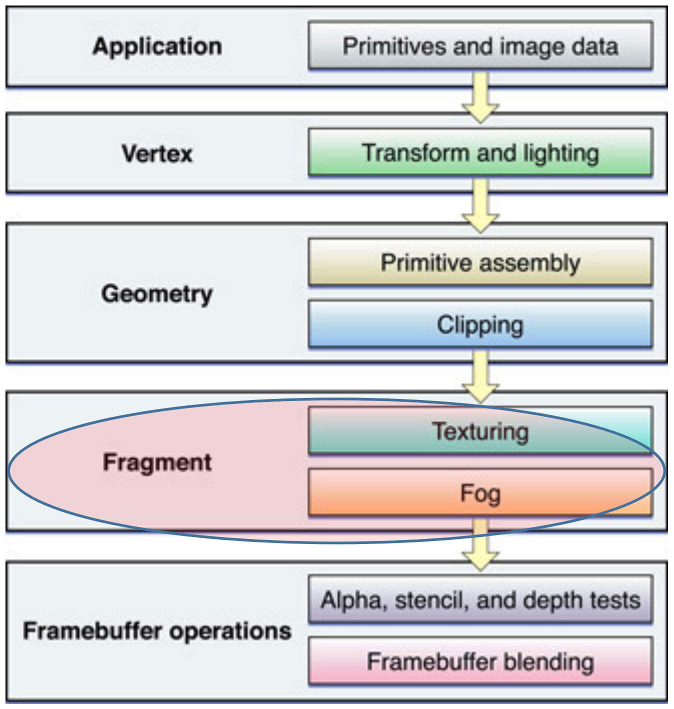

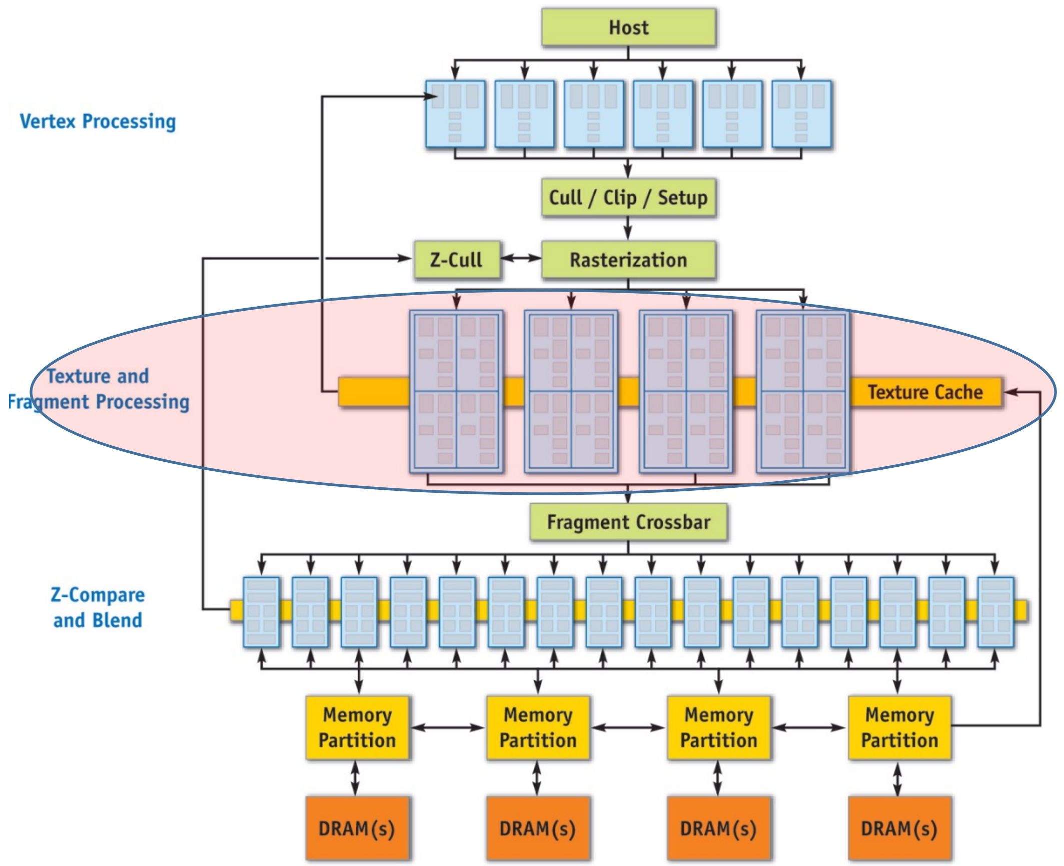

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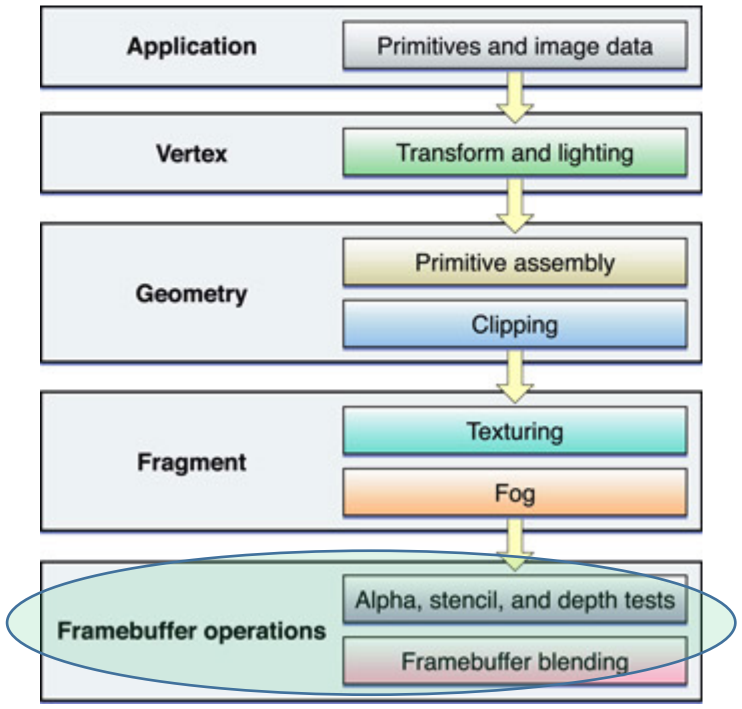

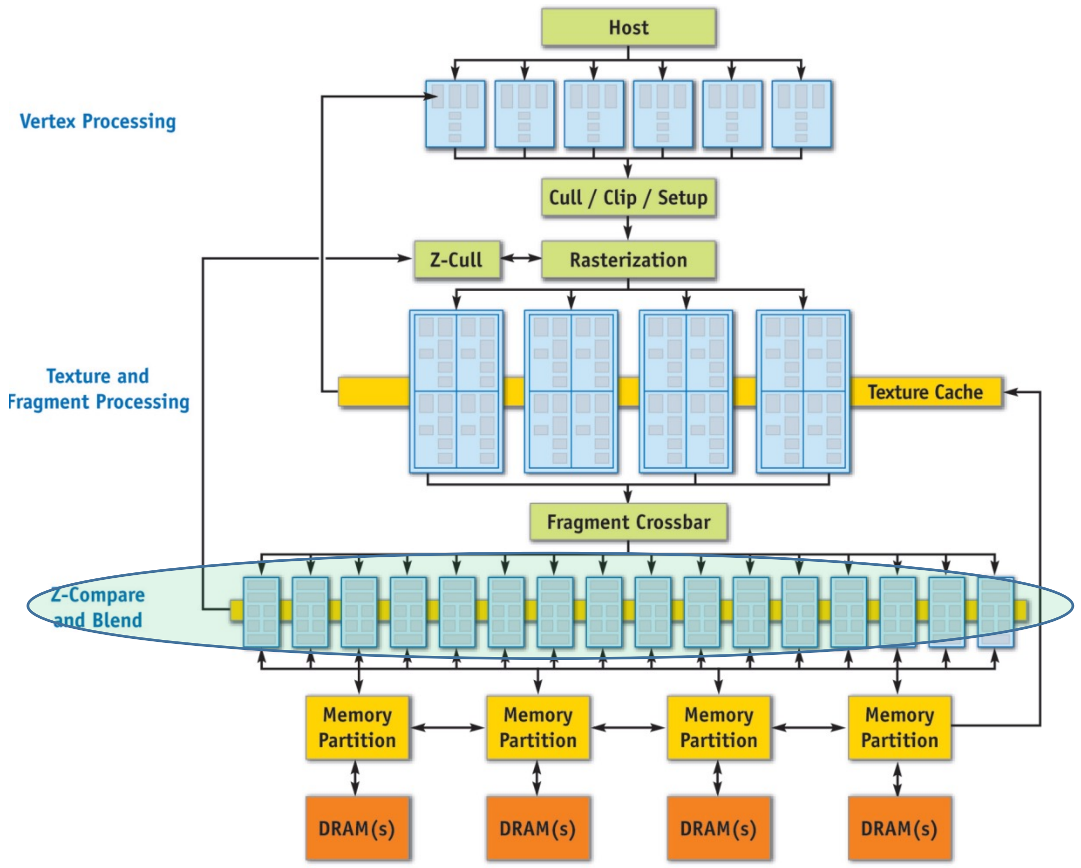

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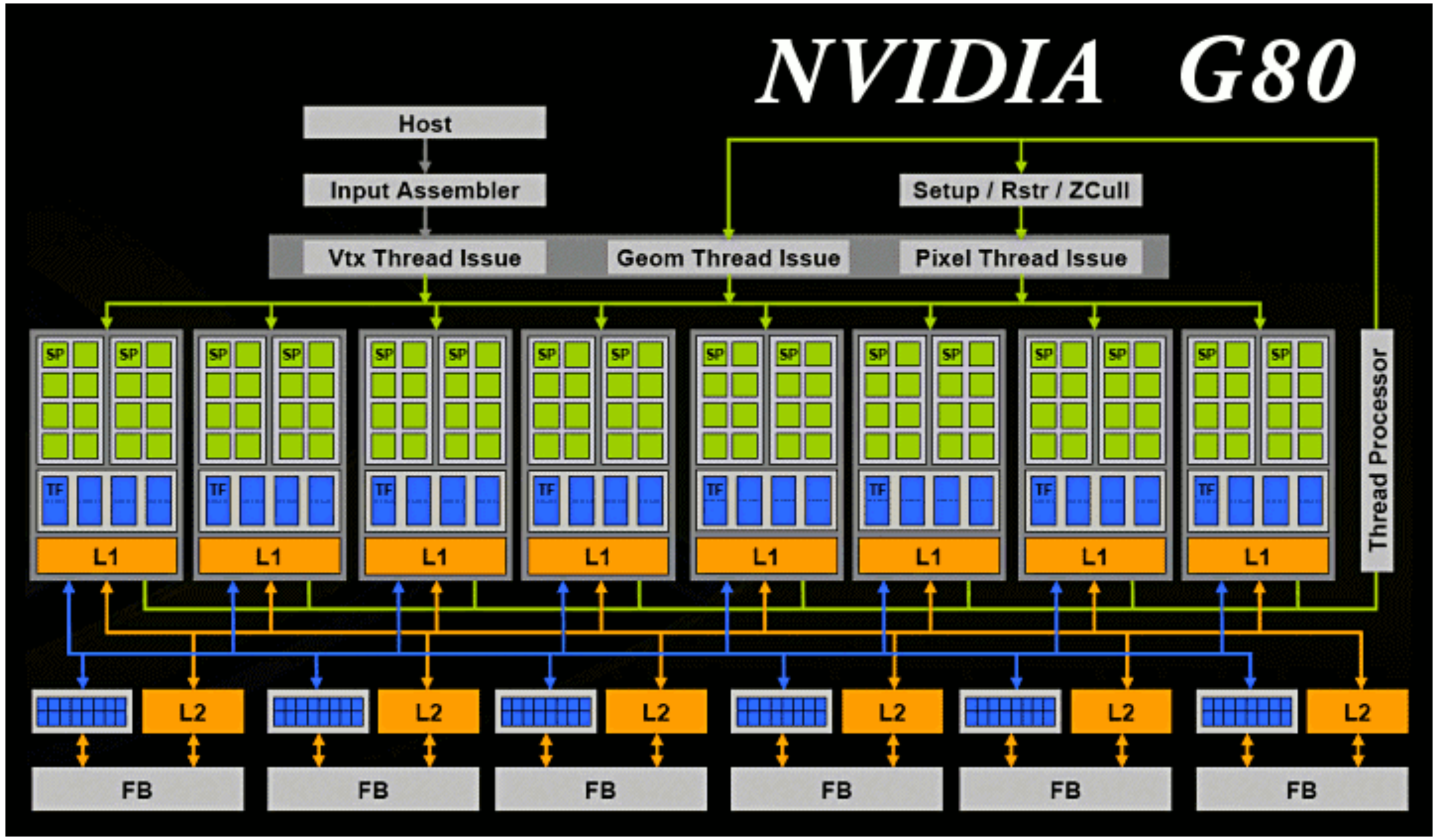
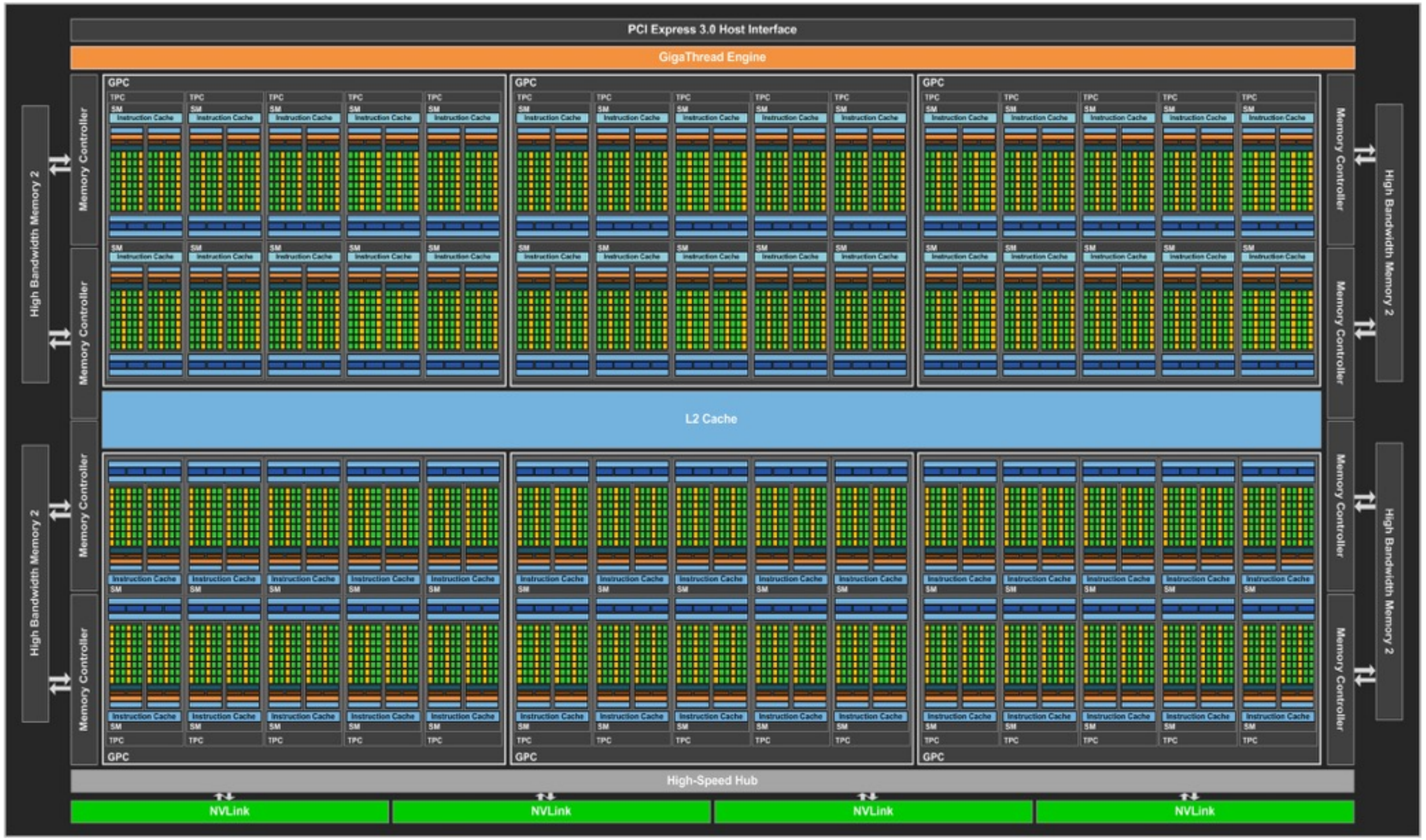
Late Modernity: unified shaders

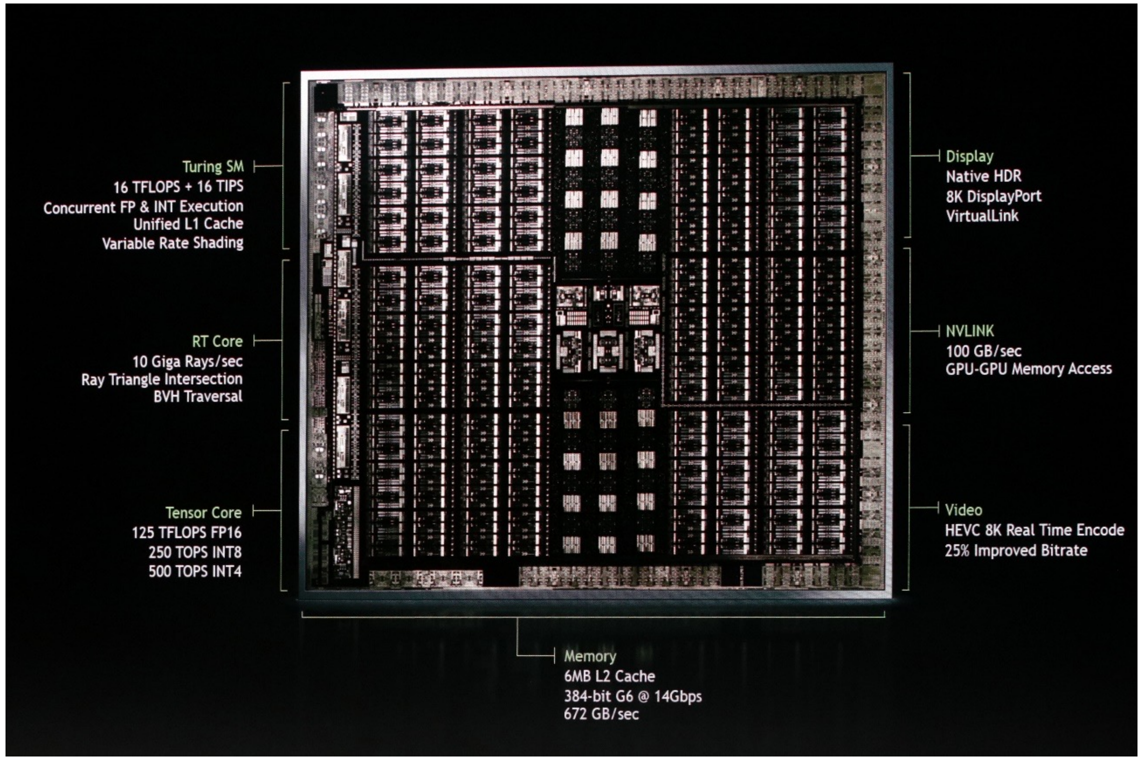


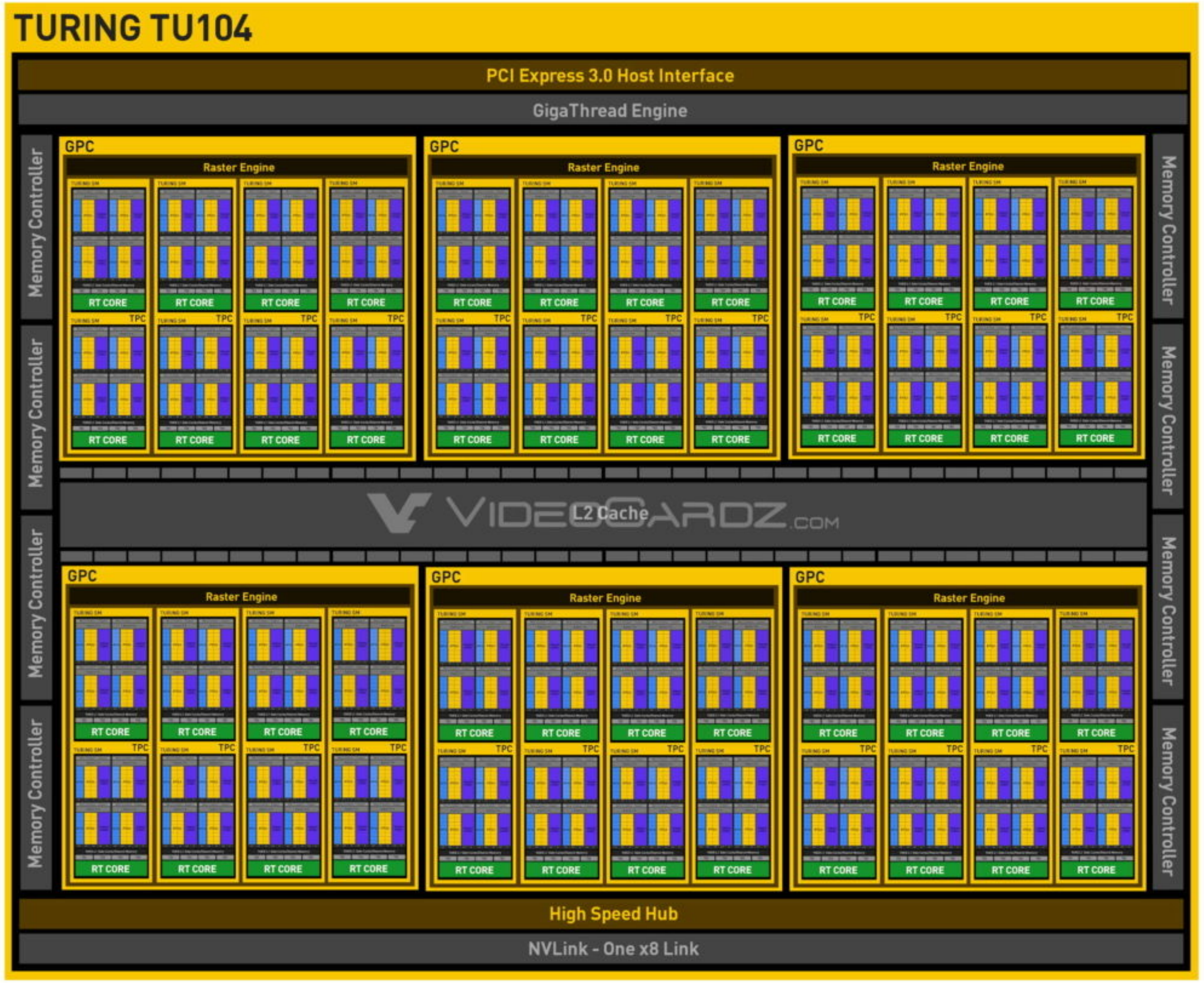
Mapping to Graphics pipeline no longer apparent
Processing elements no longer specialized to a particular role
Model supports *real* control flow, larger instr count

Mostly Modern: Pascal

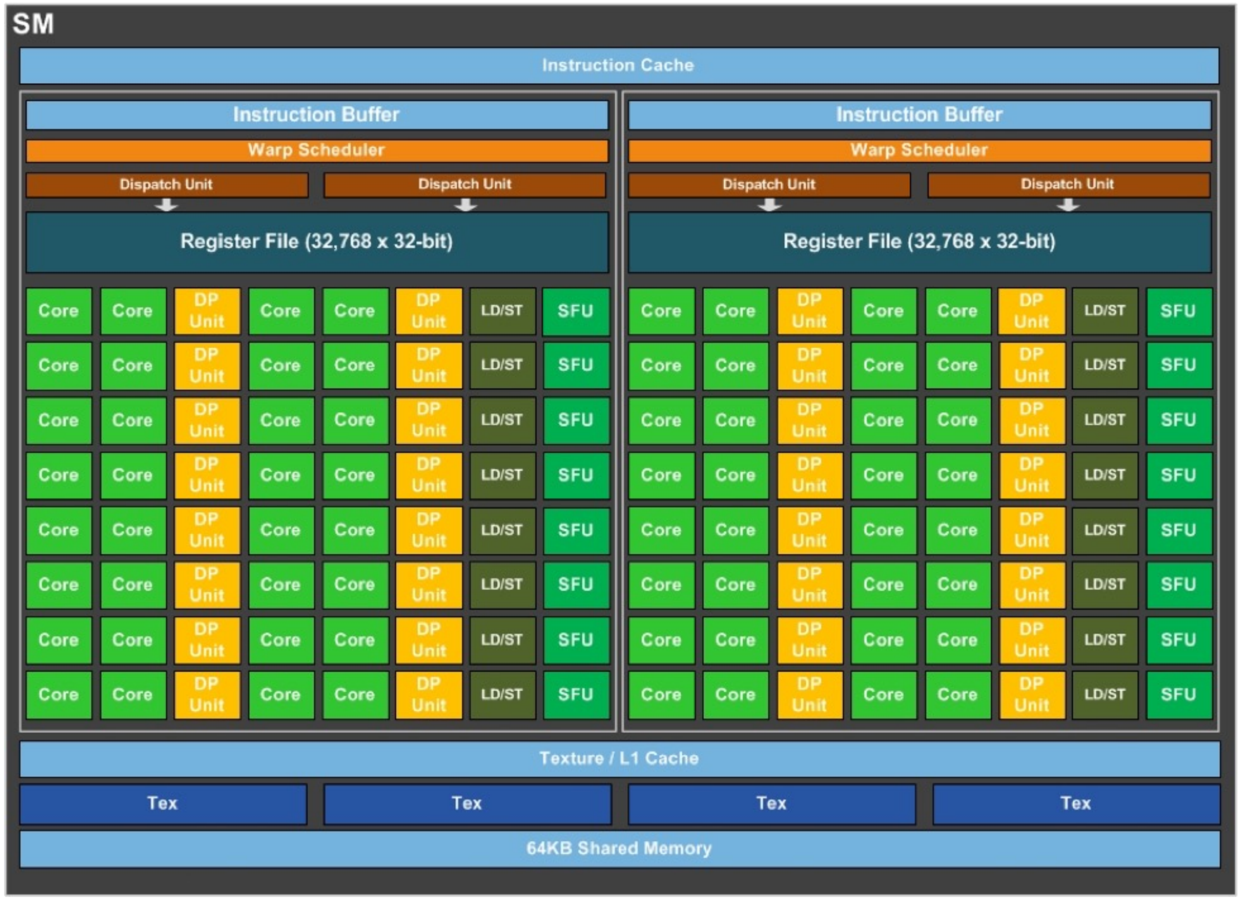


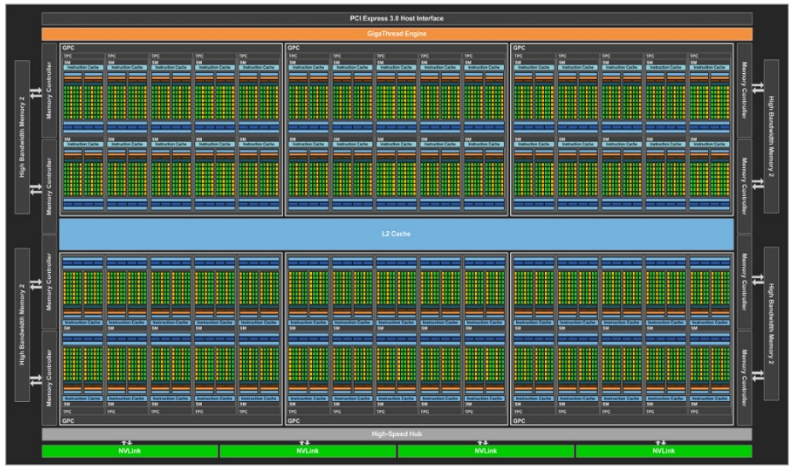
Definitely Modern: Turing





Modern Enough: Pascal SM





Cross-generational observations

GPUs designed for parallelism in graphics pipeline:

- Data
    - Per-vertex
    - Per-fragment
    - Per-pixel
- Task
    - Vertex processing
    - Fragment processing
    - Rasterization
    - Hidden-surface elimination
- MLP
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Even as GPU architectures become more general, certain assumptions persist:

1. Data parallelism is ***trivially*** exposed
2. **All** problems look like painting a box with colored dots

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    - Hidden-surface elimination
- MLP
    - HW multi-threading for hiding memory latency

Even as GPU architectures become more general, certain assumptions persist:

1. Data parallelism is ***trivially*** exposed
2. **All** problems look like painting a box with colored dots

But what if my problem isn't painting a box?!!?!

The big ideas still present in GPUs

- Simple cores
- Single instruction stream
  - Vector instructions (SIMD) OR
  - Implicit HW-managed sharing (SIMT)
- Hide memory latency with HW multi-threading

Programming Model

- ***GPUs are I/O devices, managed by user-code***
- “kernels” == “shader programs”
- 1000s of HW-scheduled threads per kernel
- Threads grouped into independent blocks.
    - Threads in a block can synchronize (barrier)
    - This is the *only* synchronization
- “Grid” == “launch” == “invocation” of a kernel
    - a group of blocks (or warps)

Parallel Algorithms

- Sequential algorithms often do not permit easy parallelization
  - Does not mean there work has no parallelism
  - A different approach can yield parallelism
  - but often changes the algorithm
  - Parallelizing != just adding locks to a sequential algorithm
- Parallel Patterns
  - Map
  - Scatter, Gather
  - Reduction
  - Scan
  - Search, Sort

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  - Map
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  - Scan
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If you can express your algorithm using these patterns, an apparently fundamentally sequential algorithm can be made parallel

Map

- Inputs
  - Array A
  - Function f(x)
- map(A, f) → apply f(x) on all elements in A
- Parallelism trivially exposed
  - f(x) can be applied in parallel to all elements, in principle

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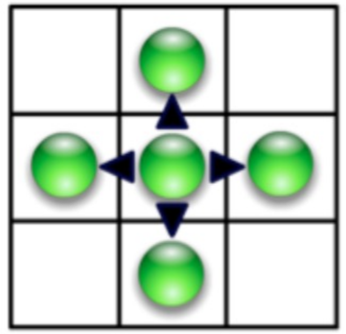
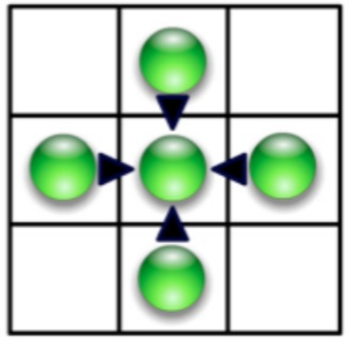
```
for(i=0; i<numPoints; i++) {
   labels[i] = findNearestCenter(points[i]);
}
```

```
map(points, findNearestCenter)
```

Scatter and Gather

- Gather:
  - Read multiple items to single location
- Scatter:
  - Write single data item to multiple locations


Scatter


Gather

Scatter and Gather

- Gather:
  - Read multiple items to single location
- Scatter:
  - Write single data item to multiple locations

```
for (i=0; i<N; ++i)
  x[i] = y[idx[i]];
```

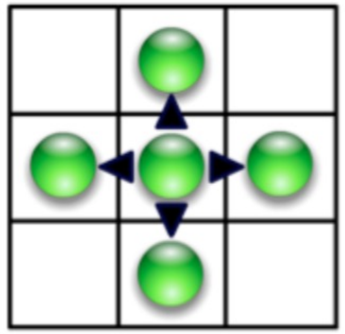
$\Rightarrow$

```
gather(x, y, idx)
```

```
for (i=0; i<N; ++i)
  y[idx[i]] = x[i];
```

$\Rightarrow$

```
scatter(x, y, idx)
```



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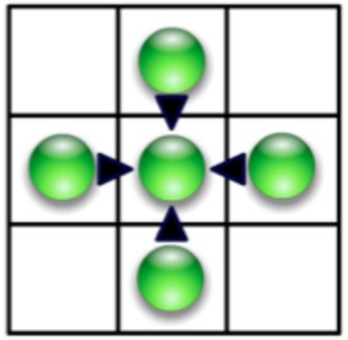

Gather

Reduce

- Input
  - Associative operator op
  - Ordered set s = [a, b, c, … z]
- Reduce(op, s) returns a op b op c … op z

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```
for(i=0; i<N; ++i) {
    accum += (map(sqr, point[i]))
}
```

```
accum = reduce(+, map(sqr, point))
```

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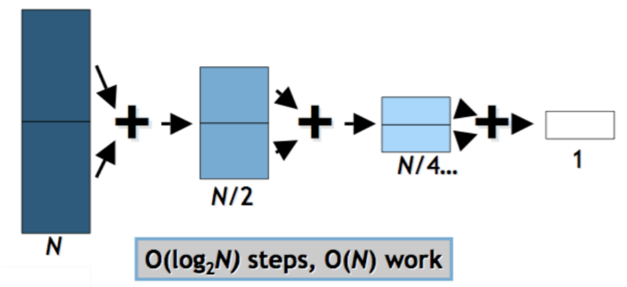
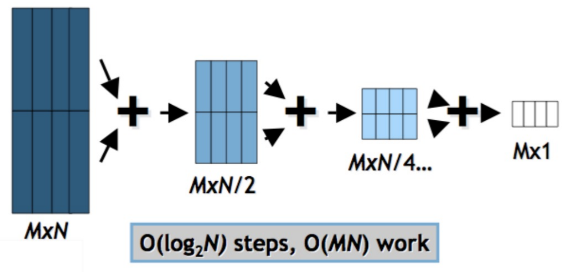
Why must op be associative?

Reduce





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```

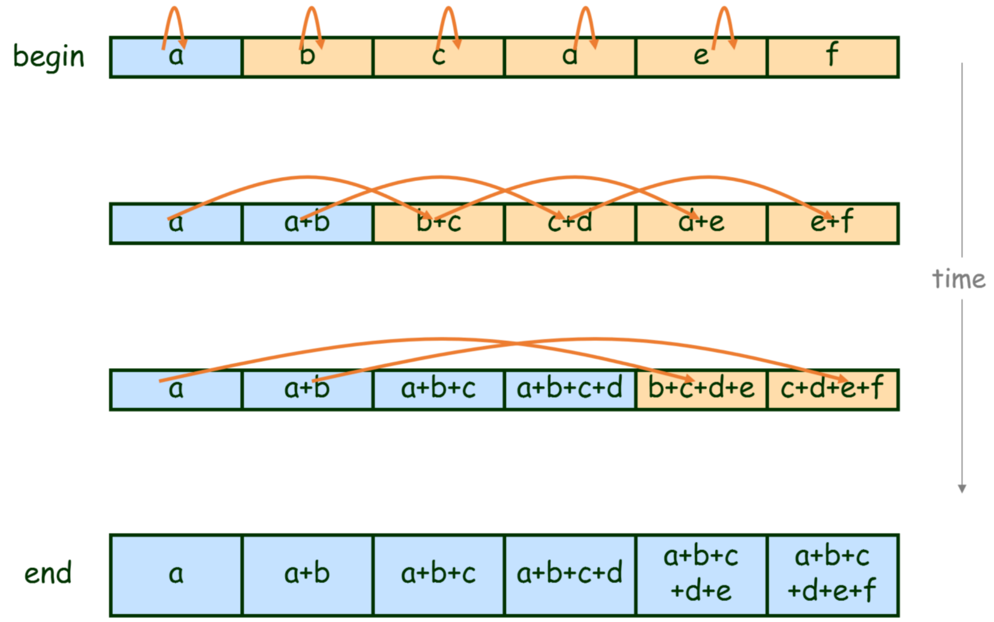
Why must op be associative?

Scan (prefix sum)

- Input
  - Associative operator op
  - Ordered set s = [a, b, c, … z]
  - Identity I

- scan(op, s) = [I, a, (a op b), (a op b op c) …]

- Scan is the workhorse of parallel algorithms:
  - Sort, histograms, sparse matrix, string compare, …



Summary

- Re-expressing apparently sequential algorithms as combinations of parallel patterns is a common technique when targeting GPUs