Concurrency: Honors Welcome to cs378h

Chris Rossbach

Outline for Today

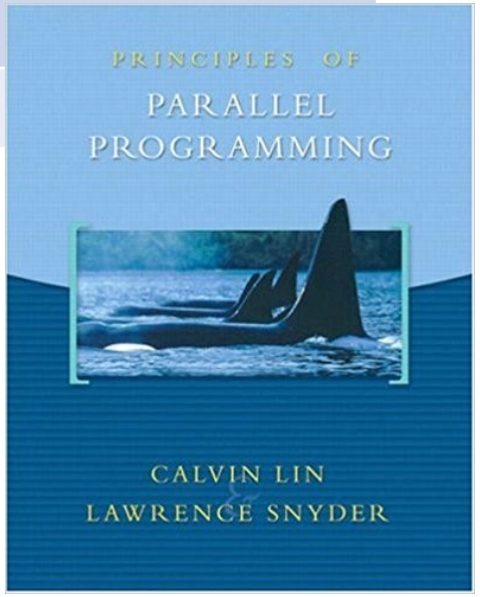
- Questions?
- Administrivia
- Course Overview
- Course Details and Logistics
- Concurrency & Parallelism Basics

Acknowledgments: some materials in this lecture borrowed from:

- *Emmett Witchel, who borrowed them from: Kathryn McKinley, Ron Rockhold, Tom Anderson, John Carter, Mike Dahlin, Jim Kurose, Hank Levy, Harrick Vin, Thomas Narten, and Emery Berger*
- *Mark Silberstein, who borrowed them from: Blaise Barney, Kunle Olukoton, Gupta*

Course Details

Course Name:	CS378H – Concurrency: Honors
Unique Number:	52670
Lectures:	T-Th 9:30-11:00AM Zoom
Class Web Page:	http://www.cs.utexas.edu/users/rossbach/cs378h
Instructor:	Chris Rossbach
TA:	Karthik Velayutham
Text:	Principles of Parallel Programming (ISBN-10: 0321487907)



Please read the syllabus!

…More on this shortly…

Why you should take this course

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  - GPUs! (optionally) FGPAs!
  - Modern Programming languages: Go! Rust!
  - Interesting synchronization primitives (not just boring old locks)
  - Programming tools people use to program *super-computers (ooh…)*

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Two perspectives:
- The "just eat your kale and quinoa" argument
- The "it's going to be fun" argument

My first computer

My first computer

My first computer

CPU

My first computer

CPU

Storage

My first computer

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Storage

Tape drive!

(also good for playing heavy metal music)

My first computer

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screen

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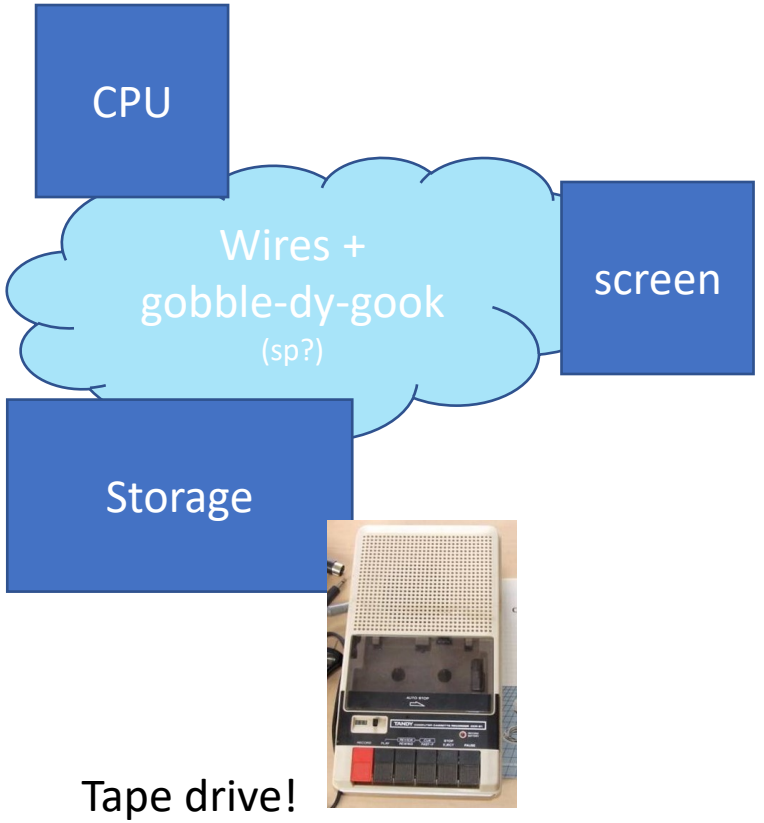

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My current computer

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Too boring…

Another of my current computers

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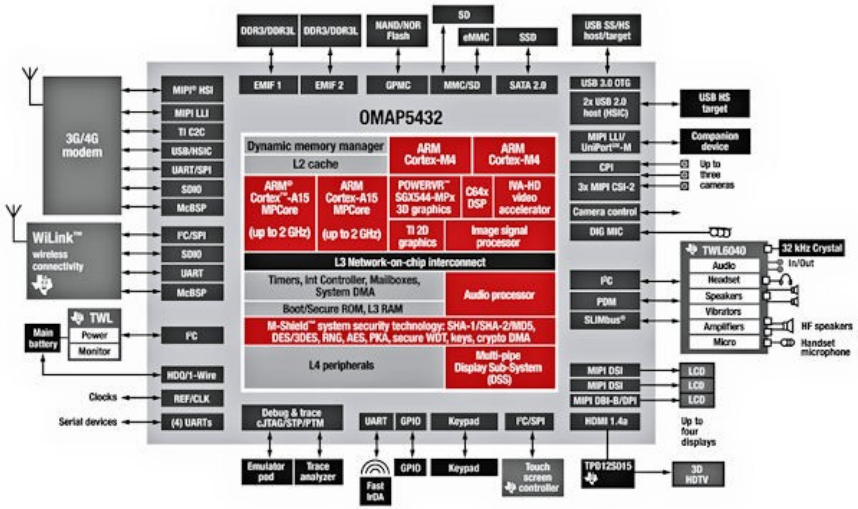

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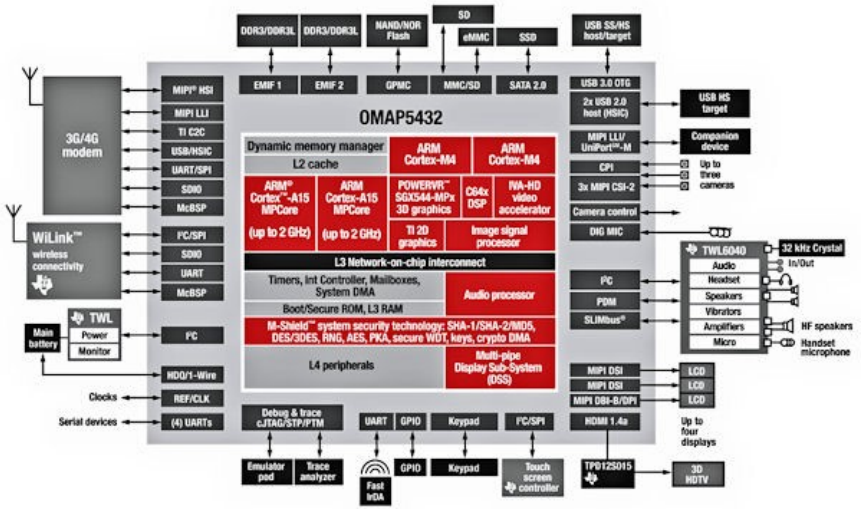

- CPU
- CPU
- GPU
- Image DSP
- Crypto
- …

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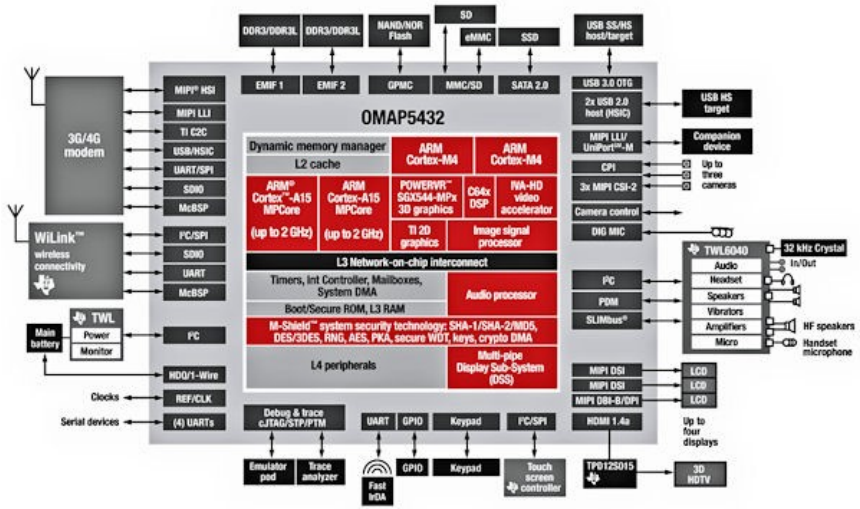

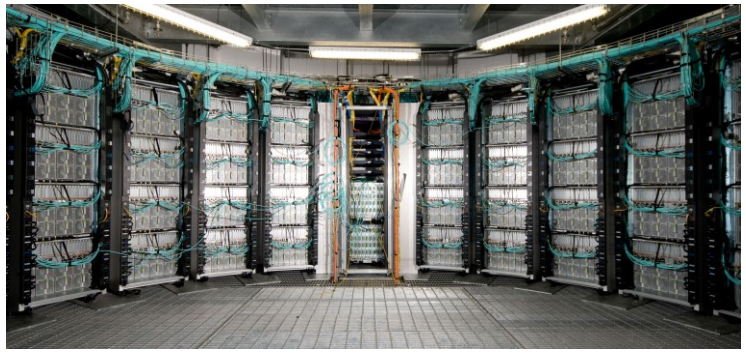

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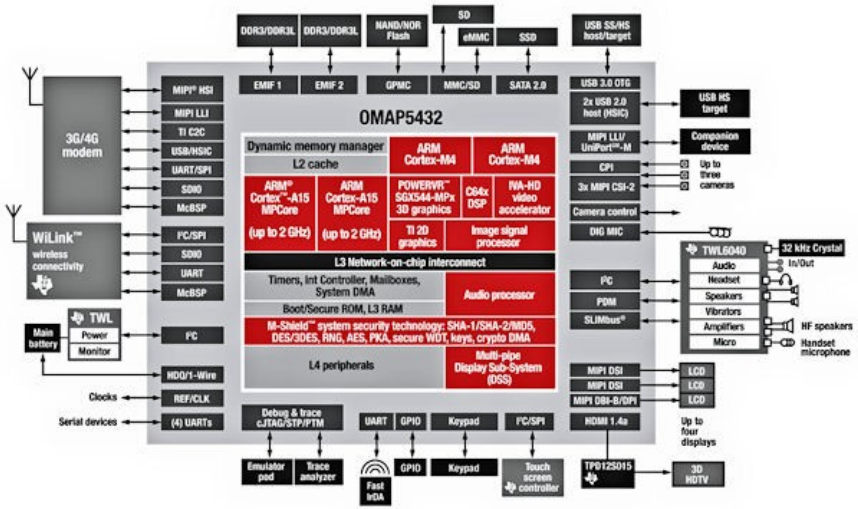
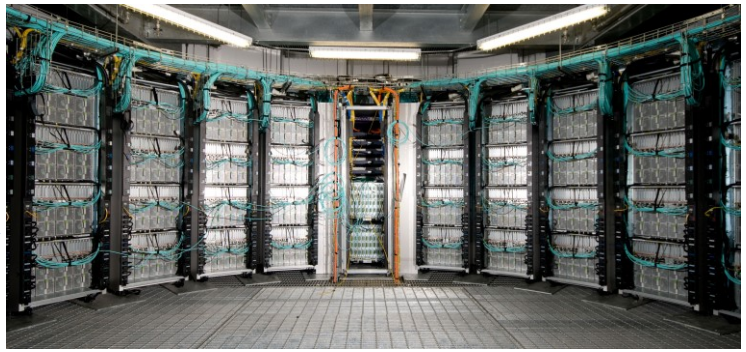
Another of my current computers

A lot has changed but…
the common theme is…??





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Modern Technology Stack

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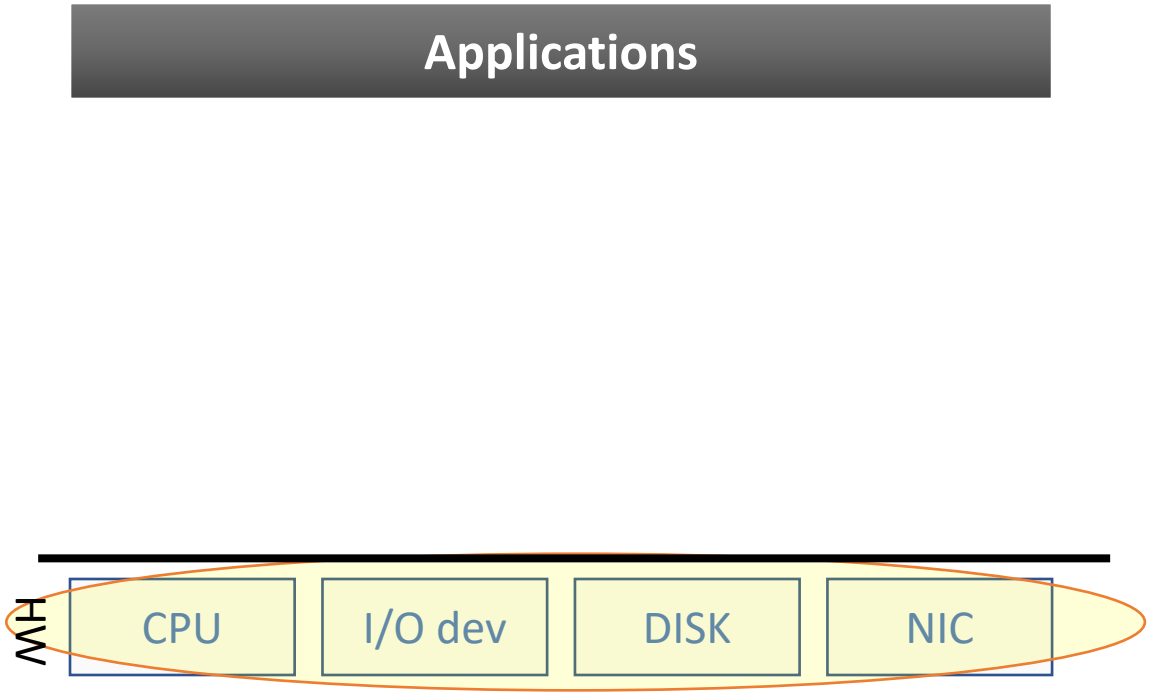

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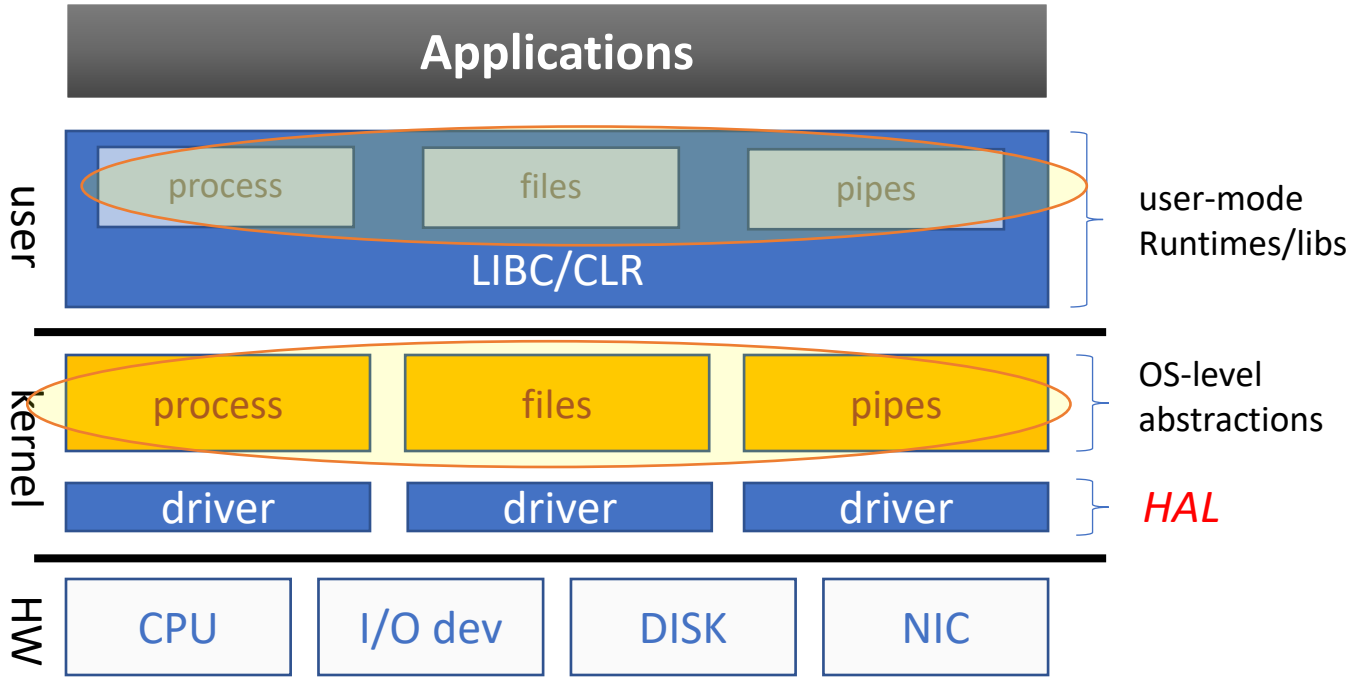

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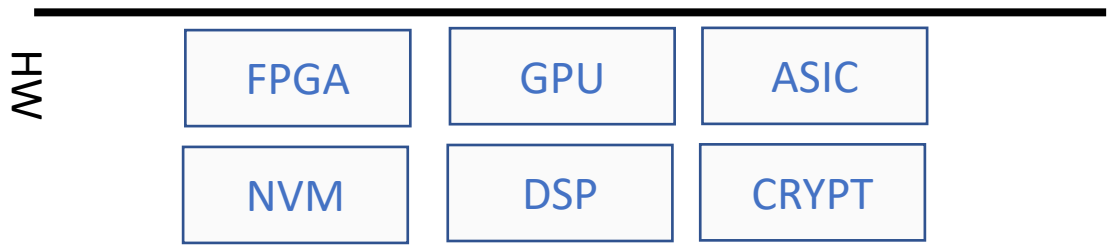

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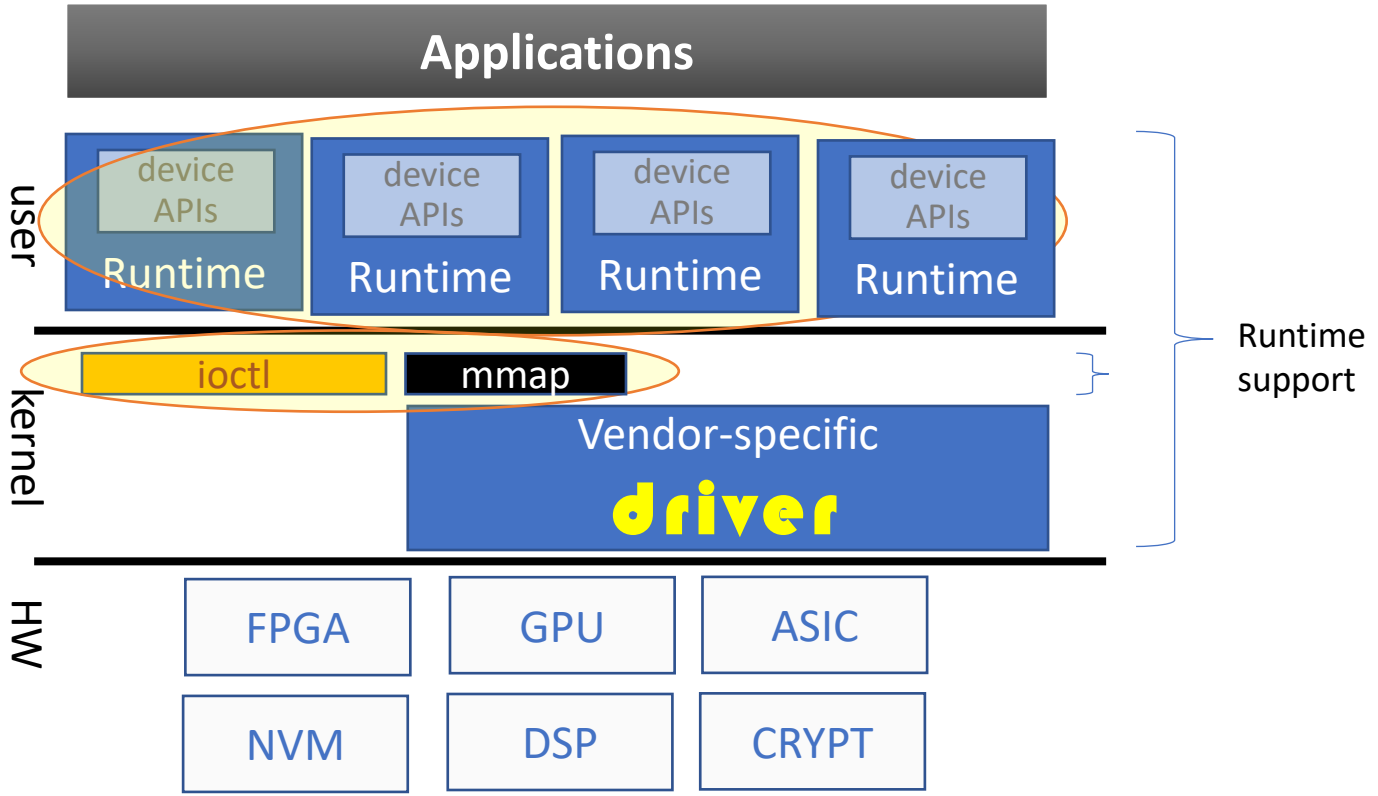
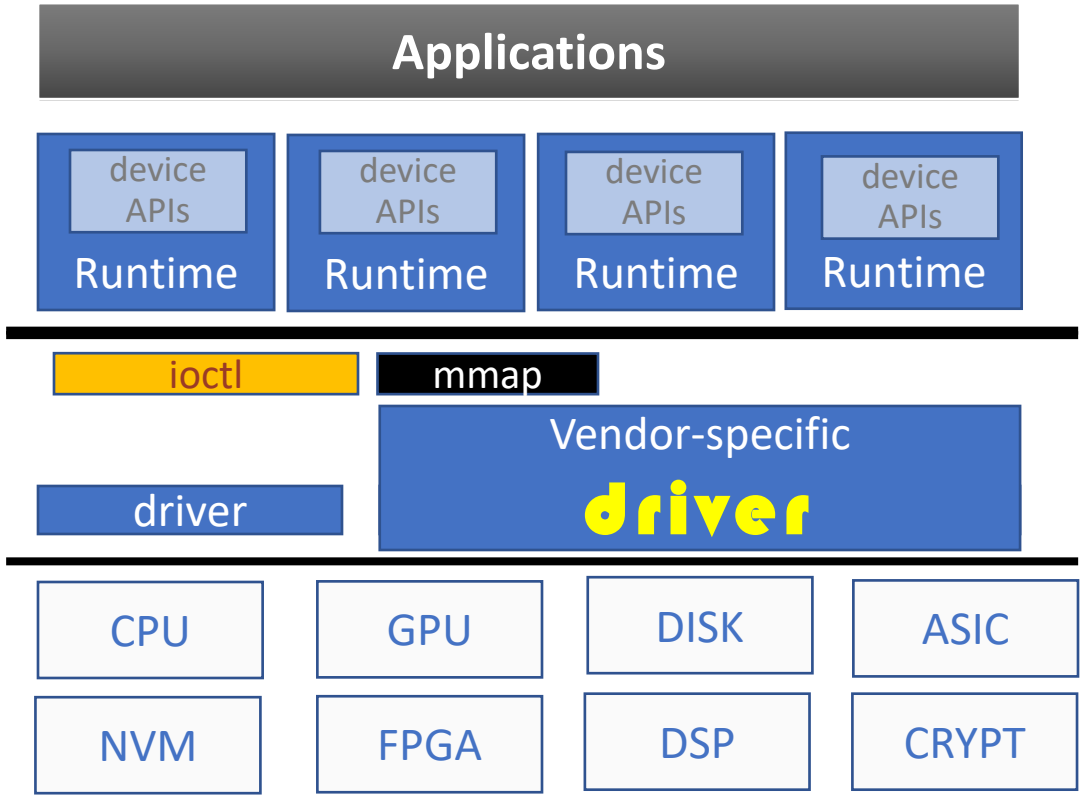


Concurrency and Parallelism are Everywhere



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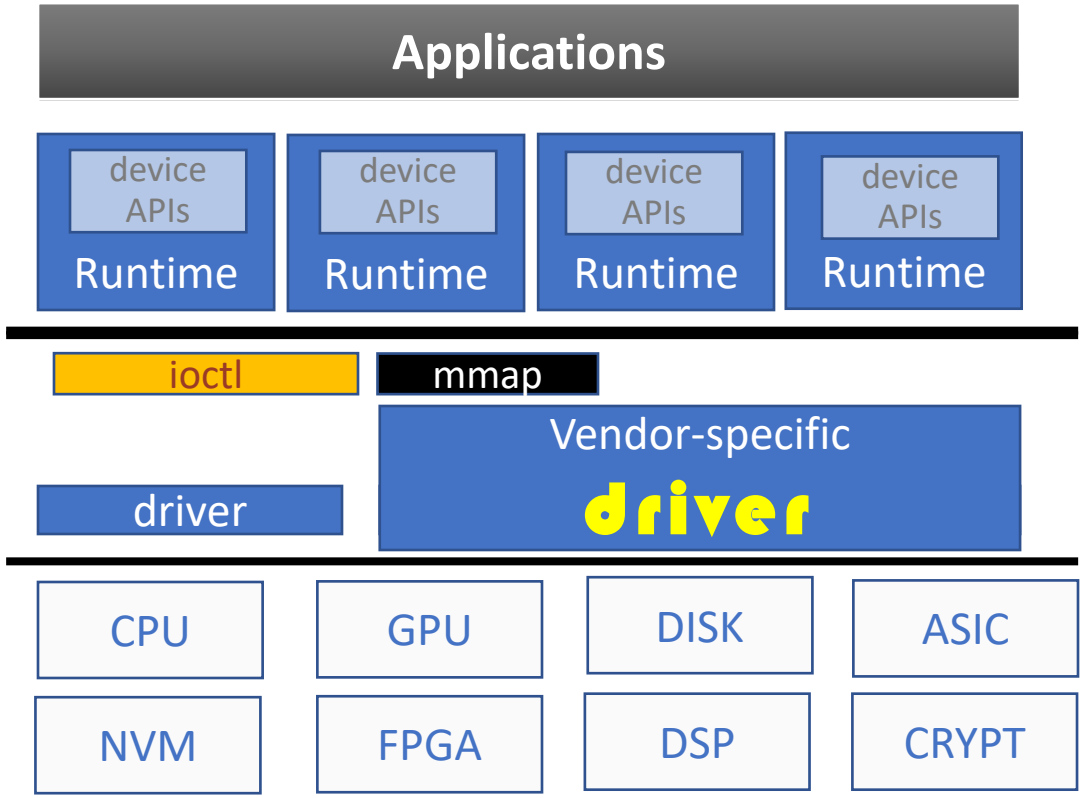

Wait!

- What's concurrency?
- What's parallelism?

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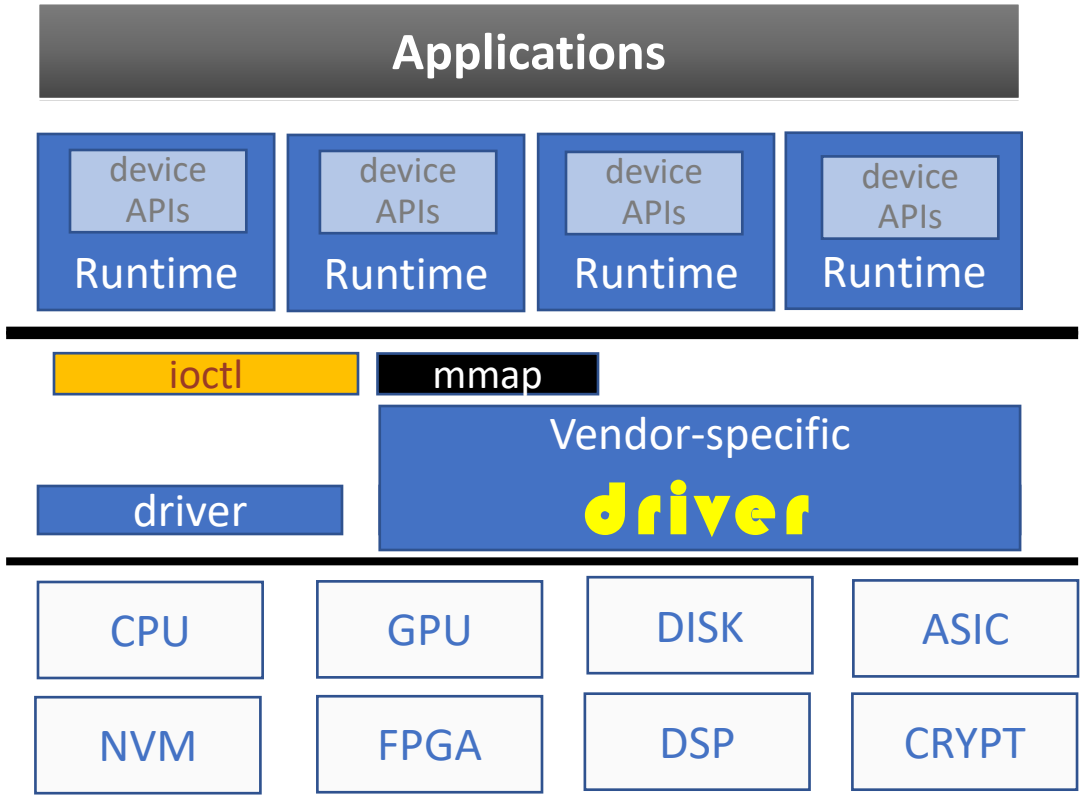

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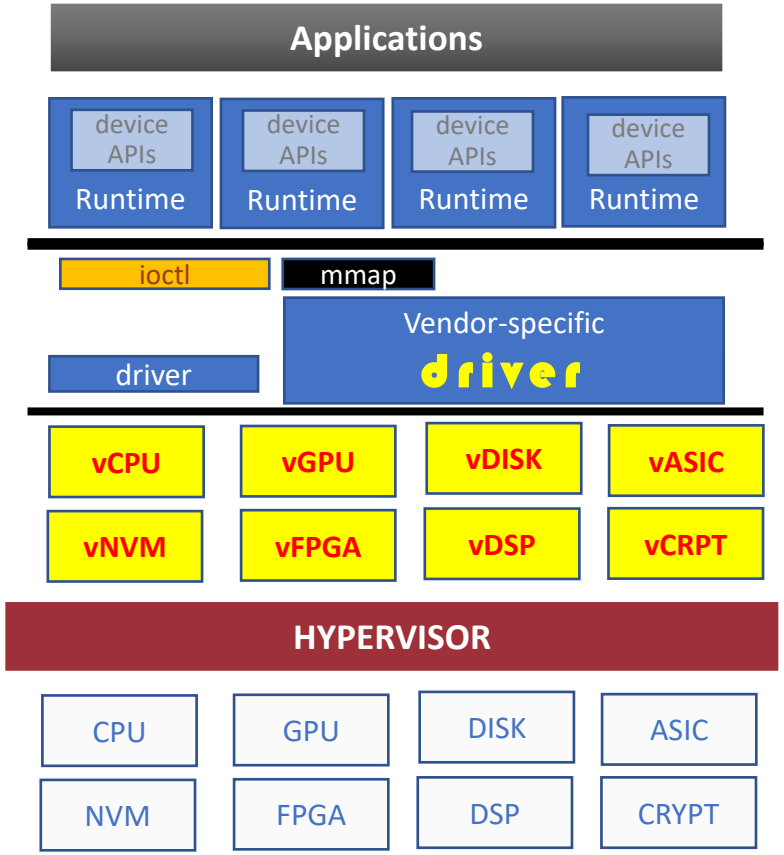

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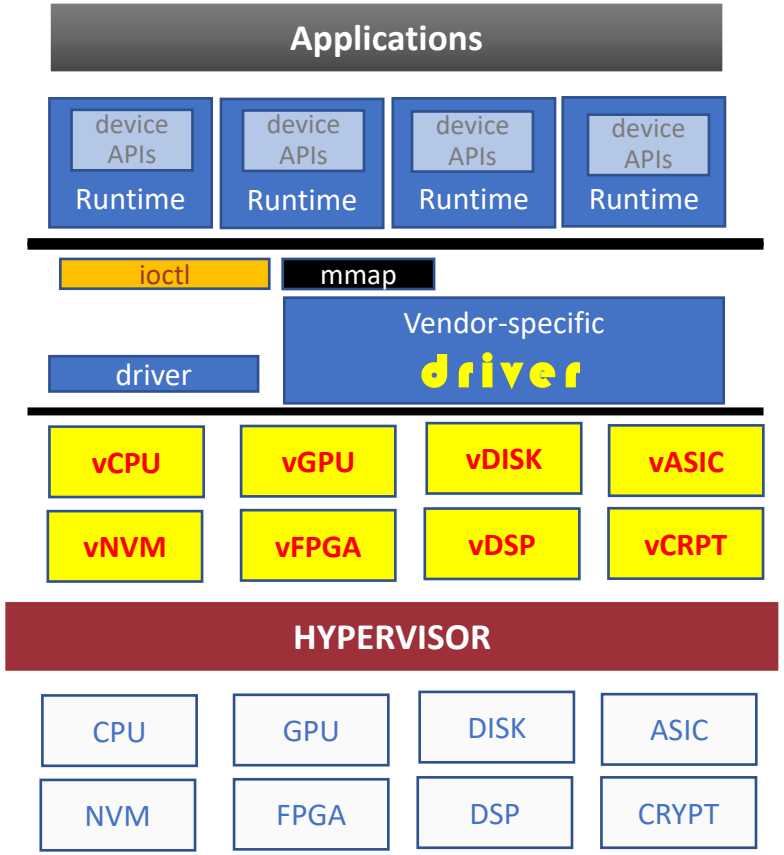

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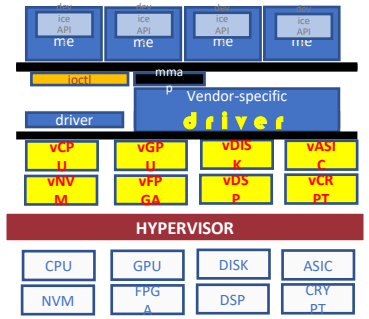

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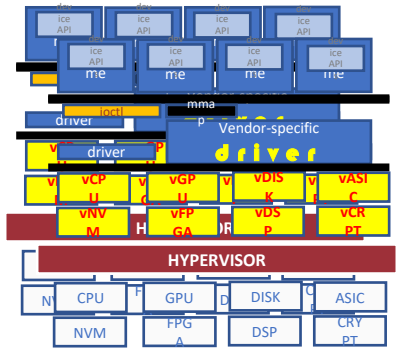

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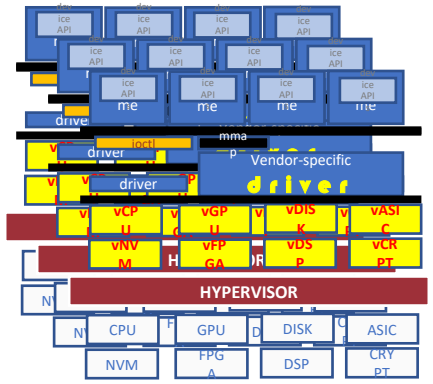

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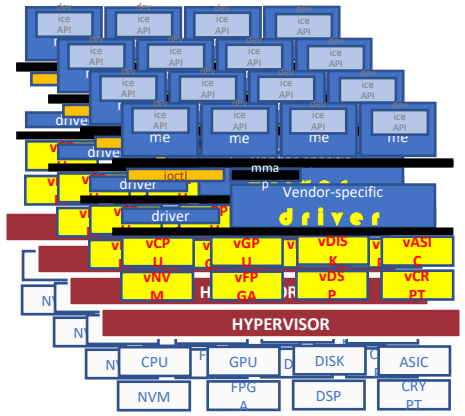

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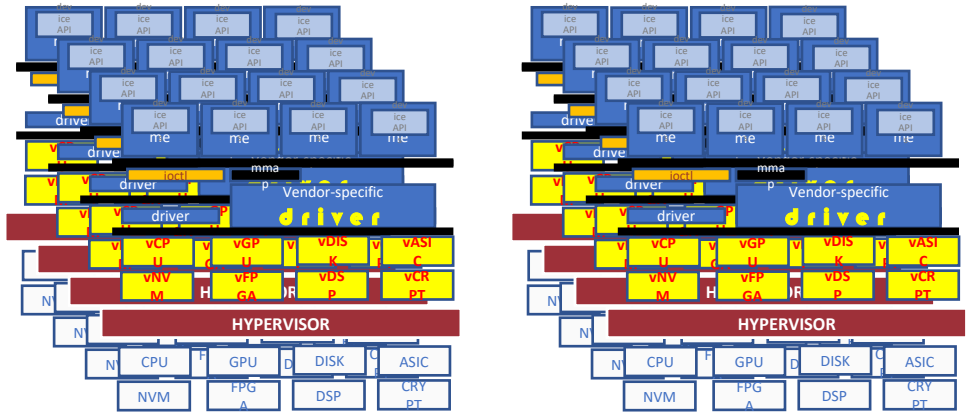

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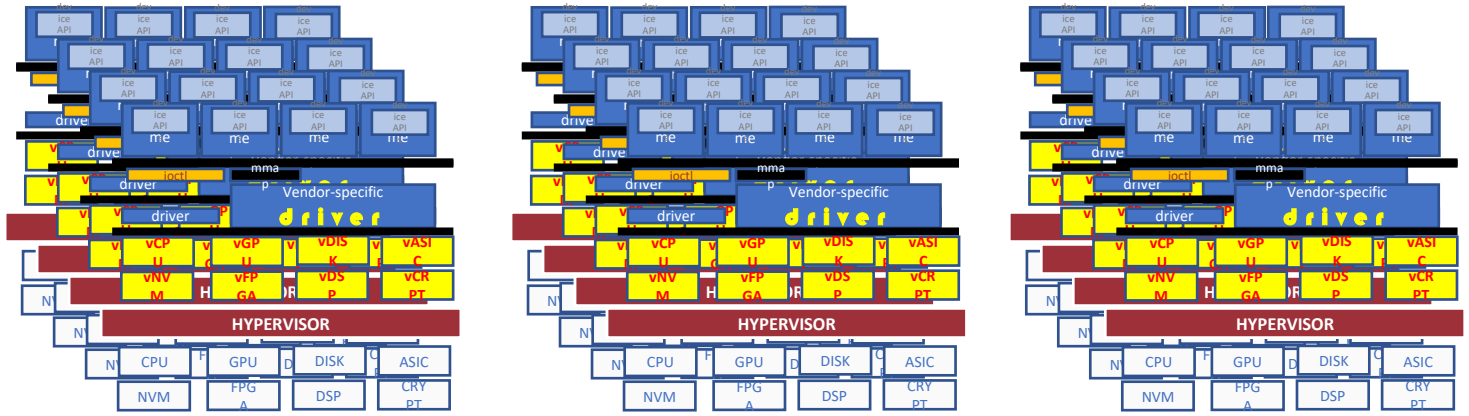

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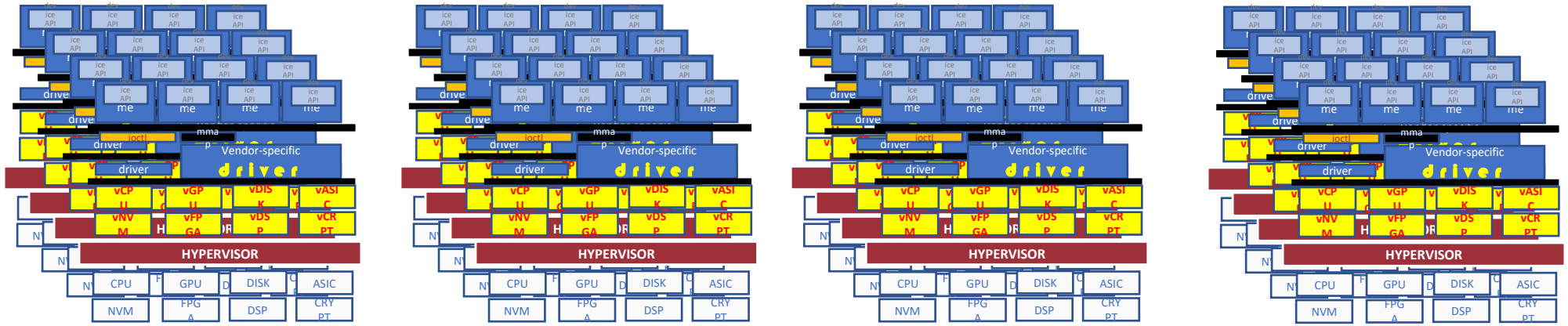

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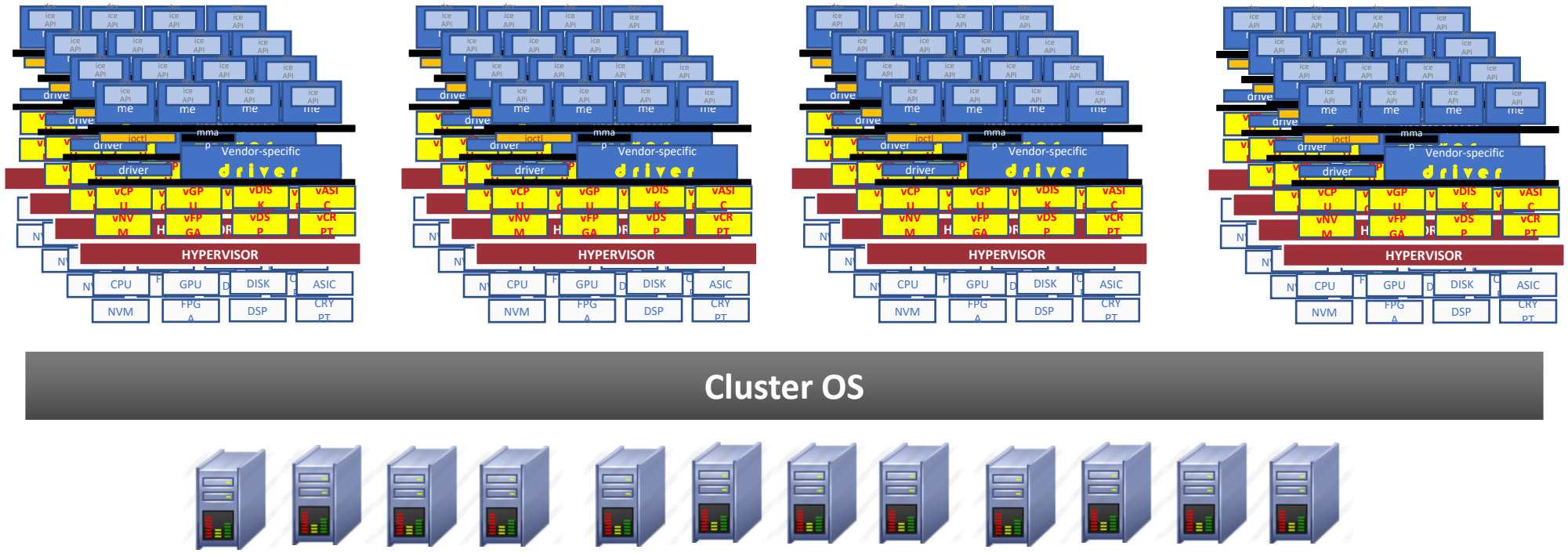

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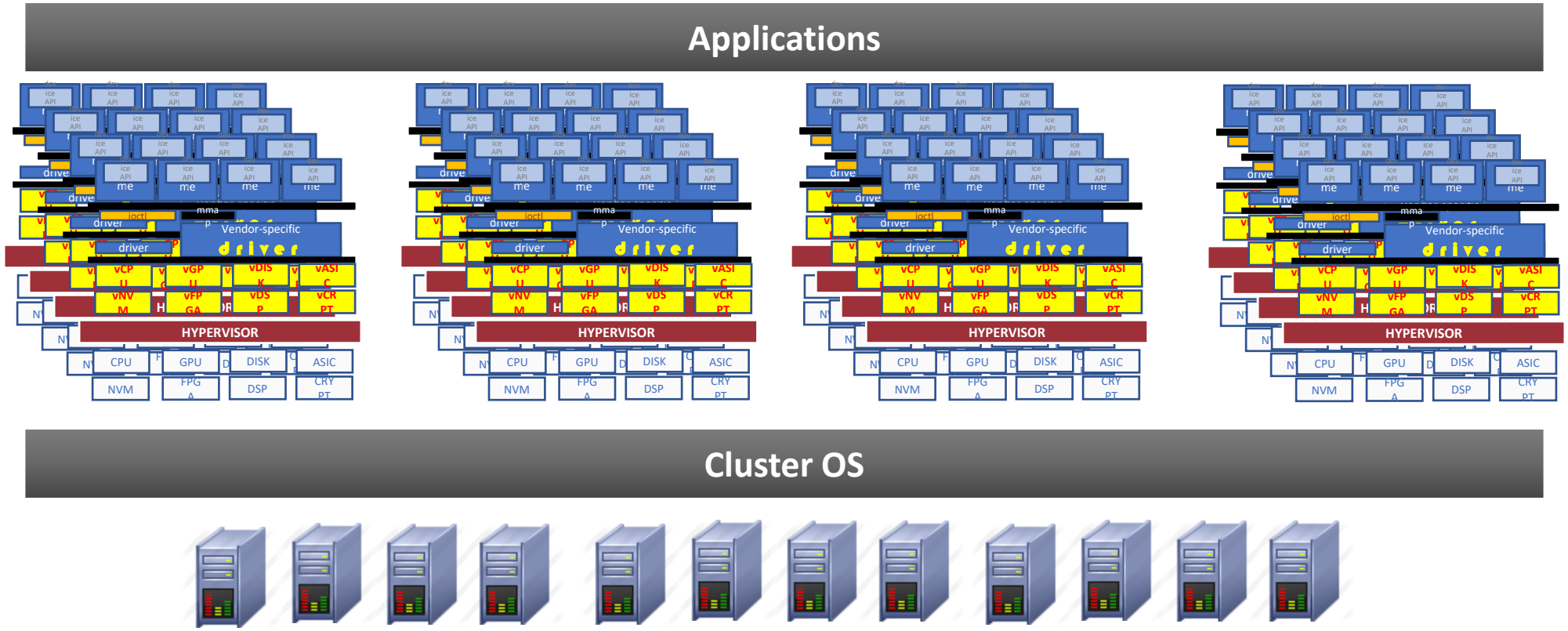

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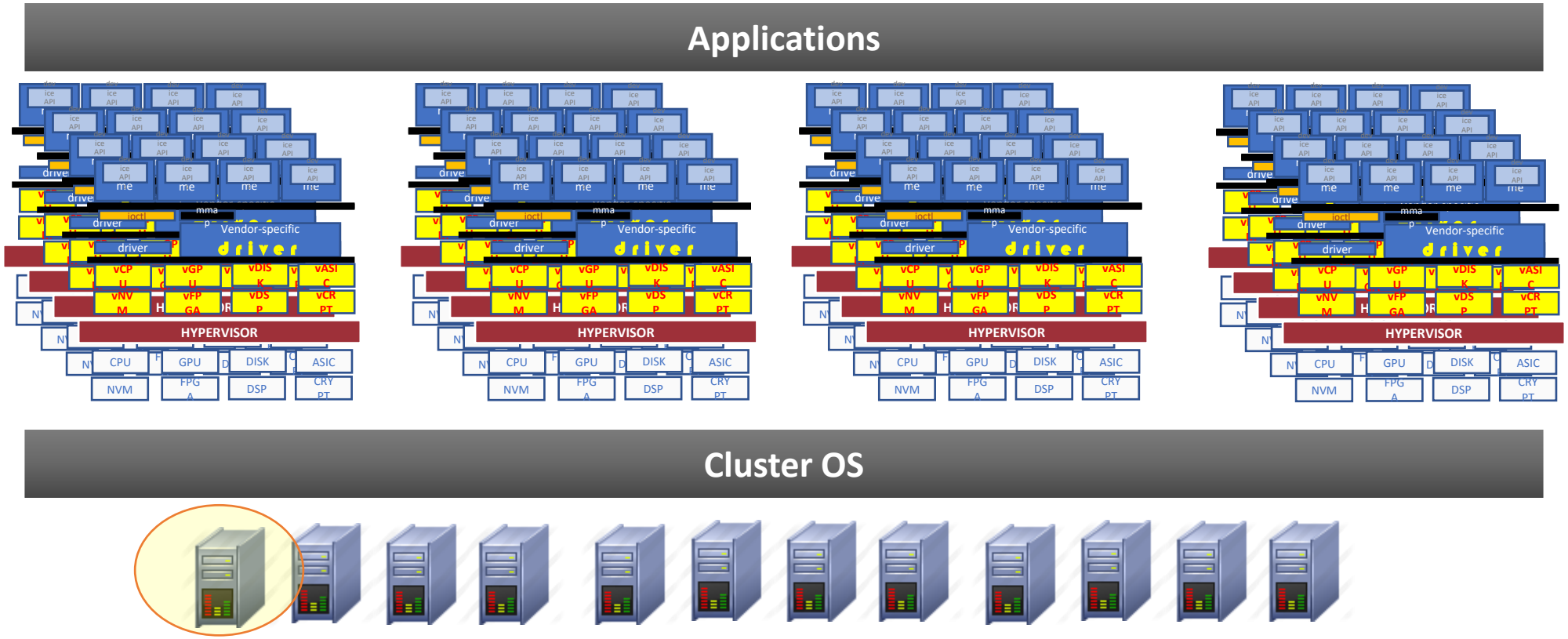
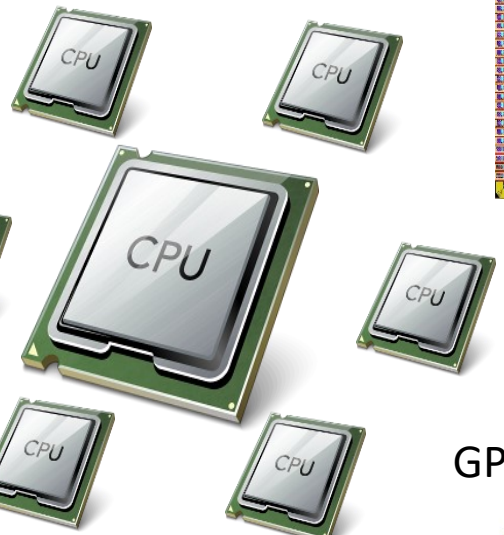
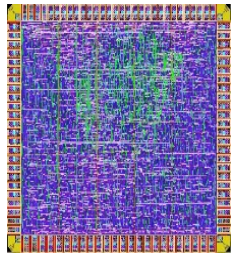


Concurrency and Parallelism are everywhere

DSP

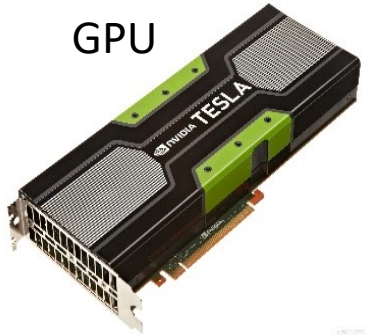




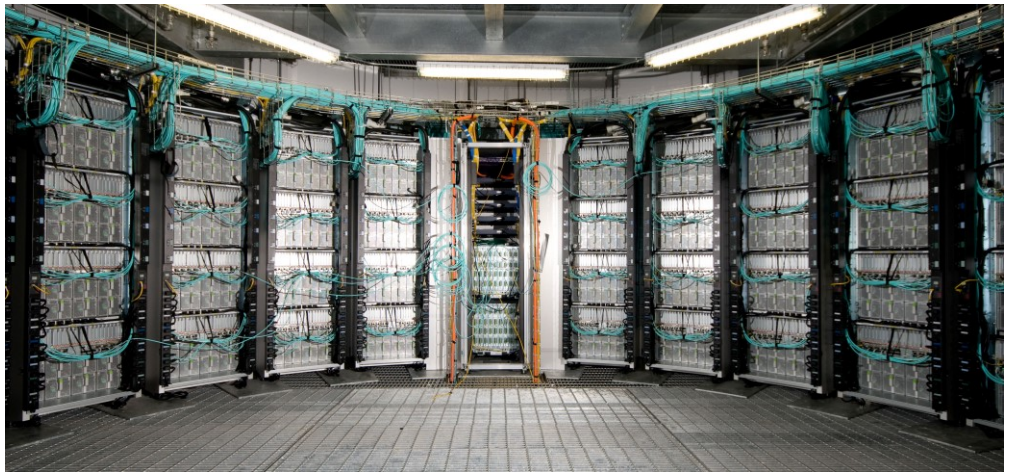
FPGA

Crypto

GPU



- CPU(s)
- GPU
- Image DSP
- Crypto
- …



Concurrency and Parallelism are everywhere

How much parallel and concurrent programming have you learned so far?

- CPU(s)
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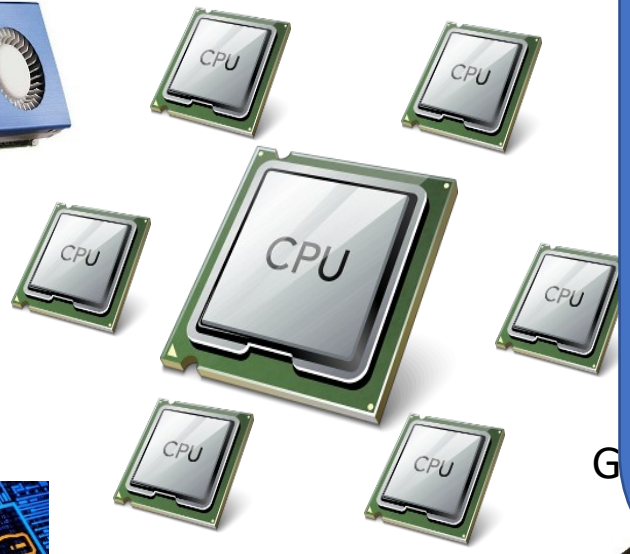
DSP

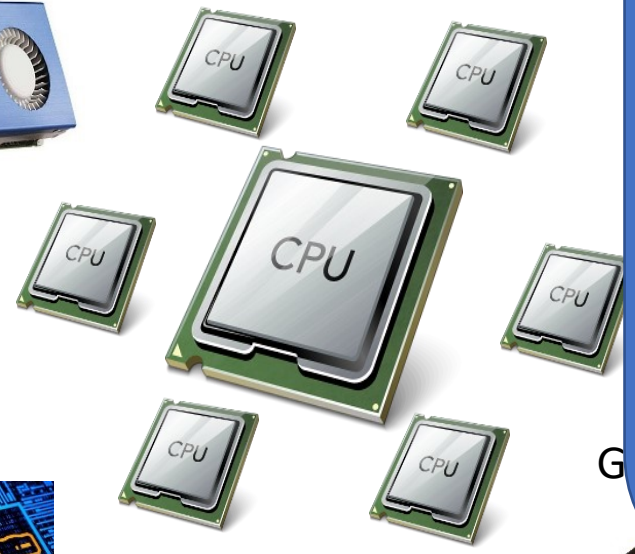


Crypto

G

Concurrency and Parallelism are everywhere

DSP



Crypto

G

How much parallel and concurrent programming have you learned so far?

- Concurrency/parallelism can't be avoided anymore (want a job?)
- A program or two playing with locks and threads isn't enough
- I've worked in industry a lot—I know

Course goal is to expose you to lots of ways of programming systems like these

…So "you should take this course because it's good for you" (eat your #$(*& kale!)

- CPU(s)
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Goal: Make Concurrency Your Close Friend
Method: Use Many Different Approaches to Concurrency

Abstract	Concrete
Locks and Shared Memory Synchronization	Prefix Sum with pthreads
Language Support	Go lab: condition variables, channels, go routines Rust lab: 2PC
Parallel Architectures	GPU Programming Lab ***(Optional) FPGA Programming Lab***
HPC	Optional MPI lab
Distributed Computing / Big Data	Rust 2PC / MPI labs
Modern/Advanced Topics	• Specialized Runtimes / Programming Models • Auto-parallelization • Race Detection
Whatever Interests YOU	Project

Logistics Reprise

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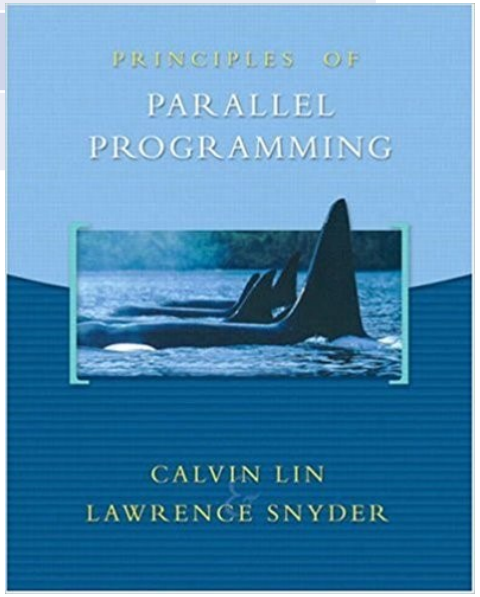

Seriously, read the syllabus!
Also, start Lab 1!

Two Super-Serious Notes

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- Inclusivity and respect are *absolute* musts

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Serial vs. Parallel Program

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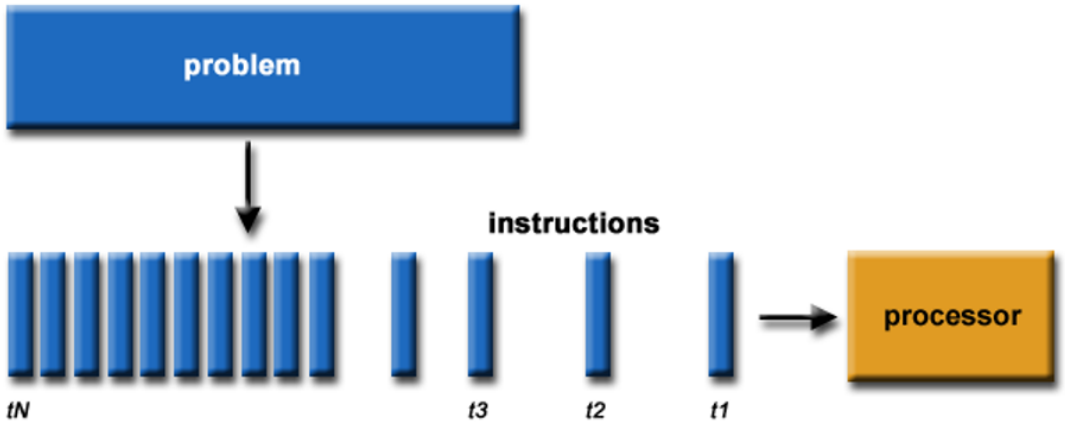
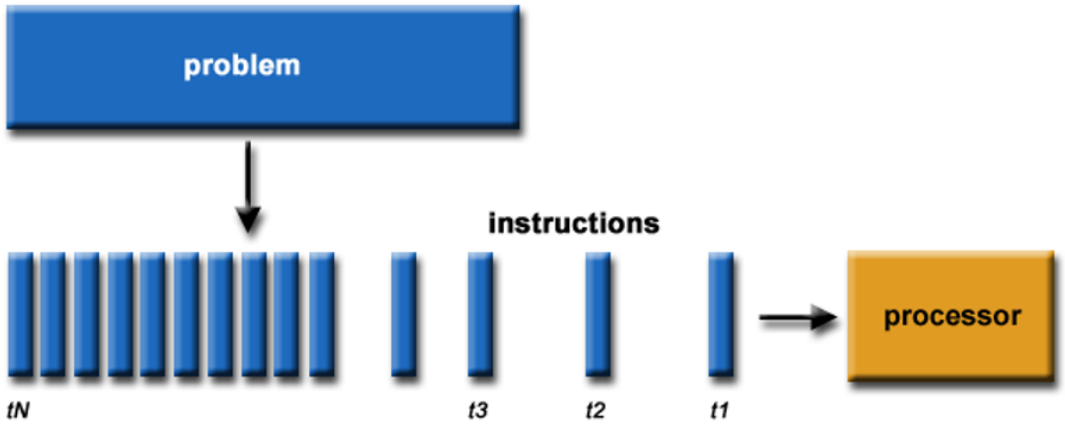


One instruction at a time (apparently)

Serial vs. Parallel Program



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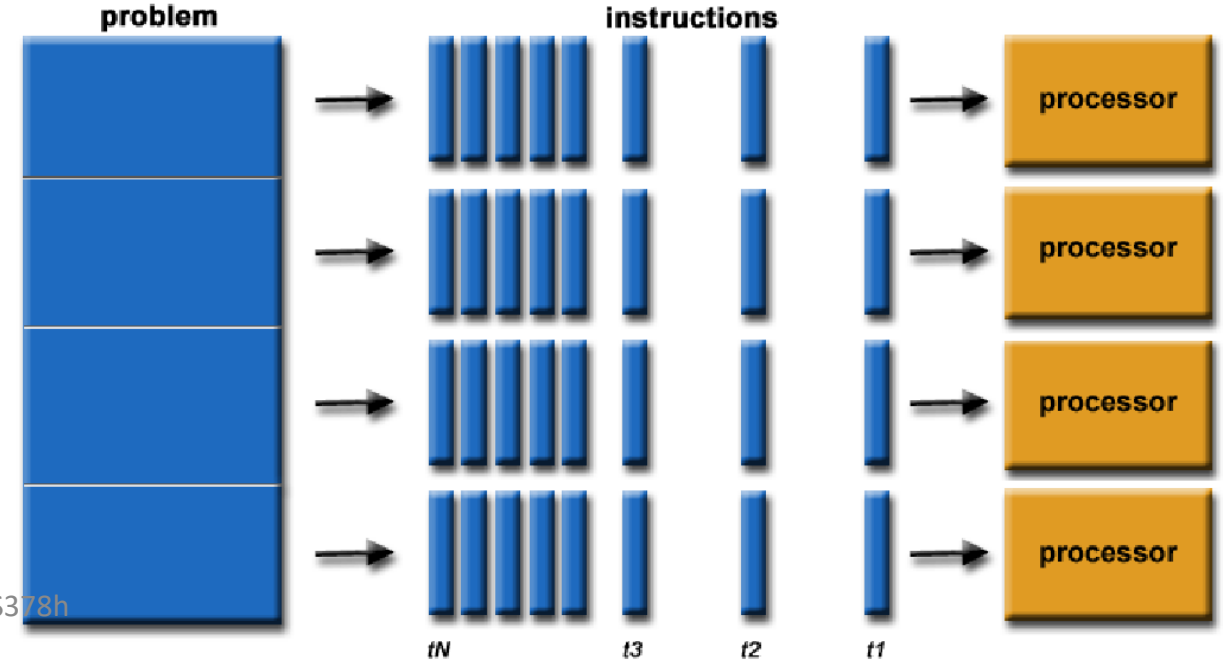
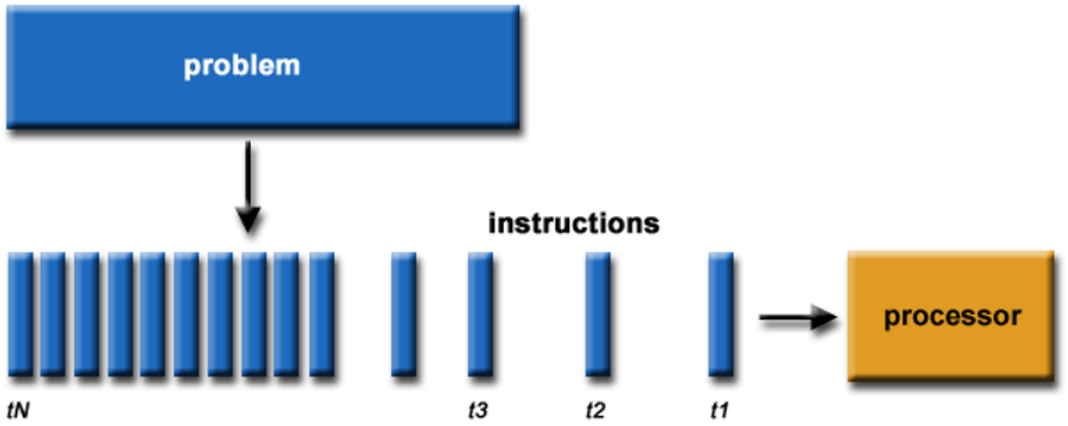
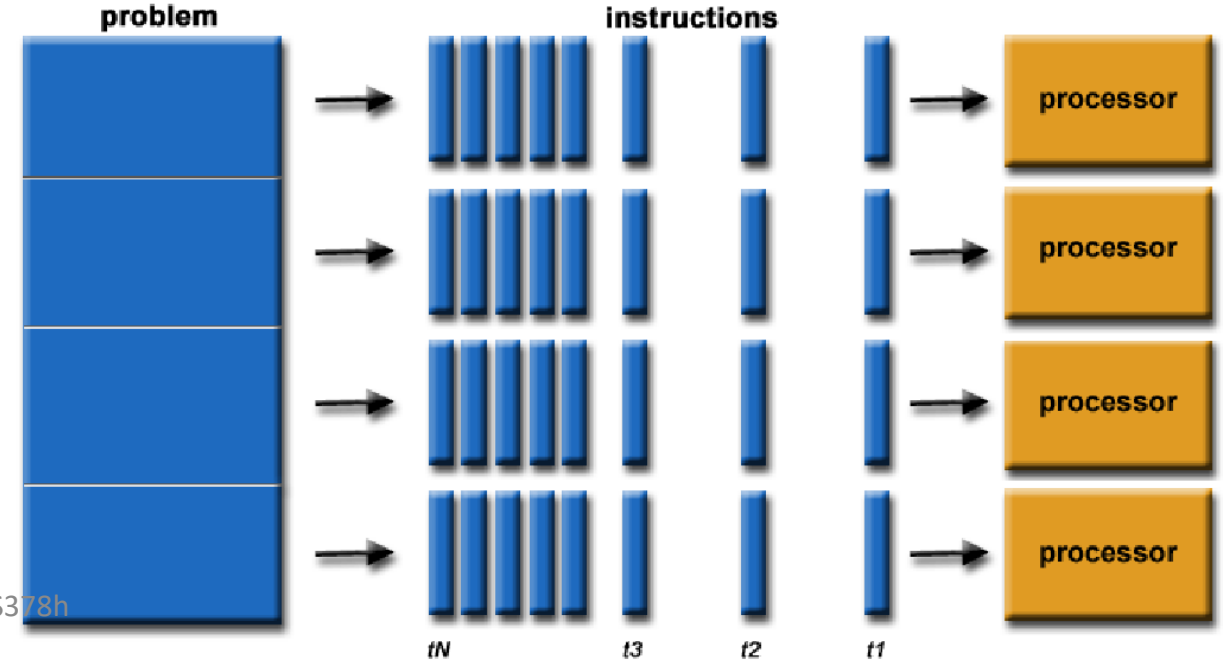


Multiple instructions in parallel

Serial vs. Parallel Program

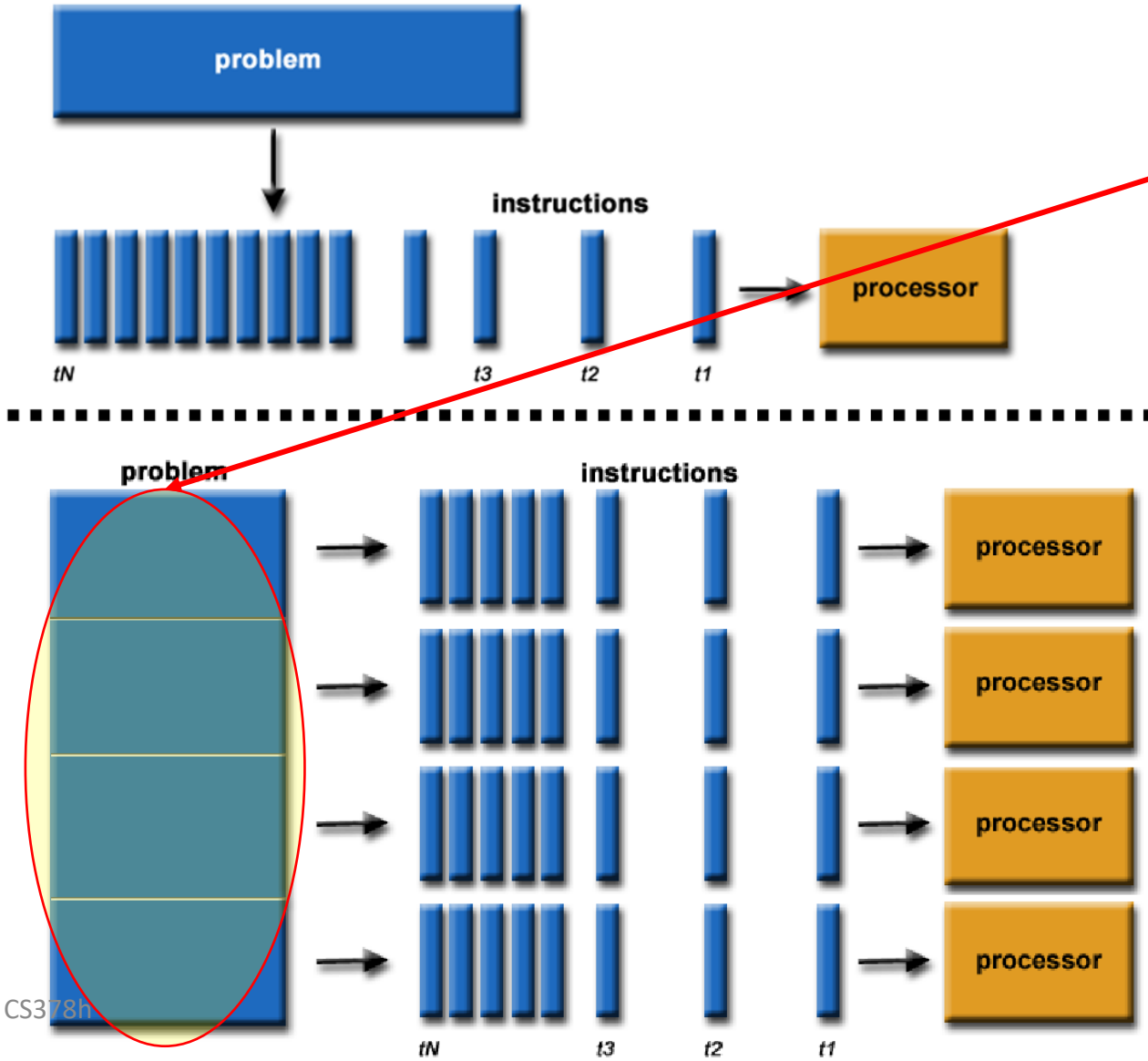


Key concerns:



Multiple instructions in parallel

Serial vs. Parallel Program

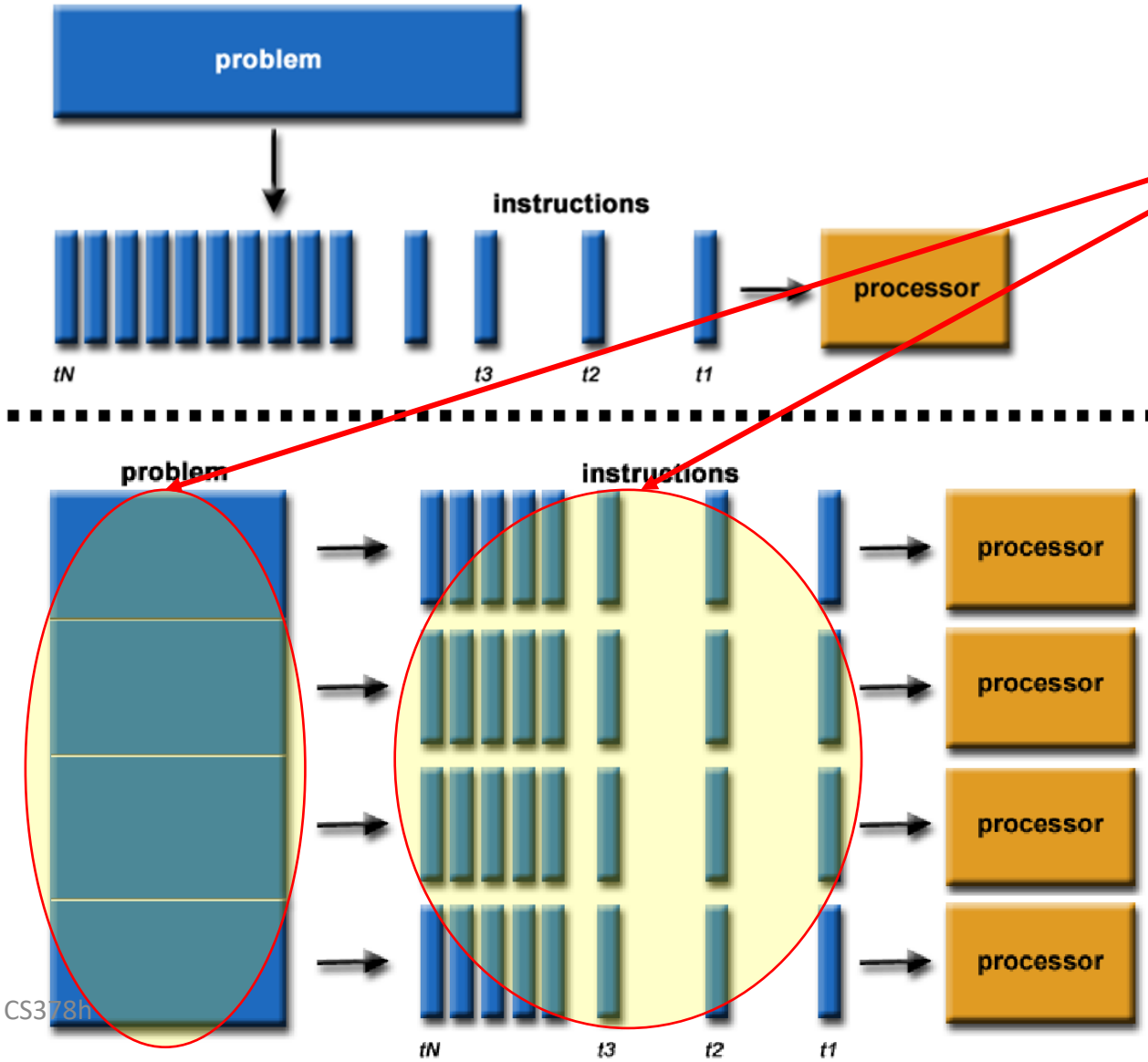


Key concerns:

- Programming model

Multiple instructions in parallel

Serial vs. Parallel Program

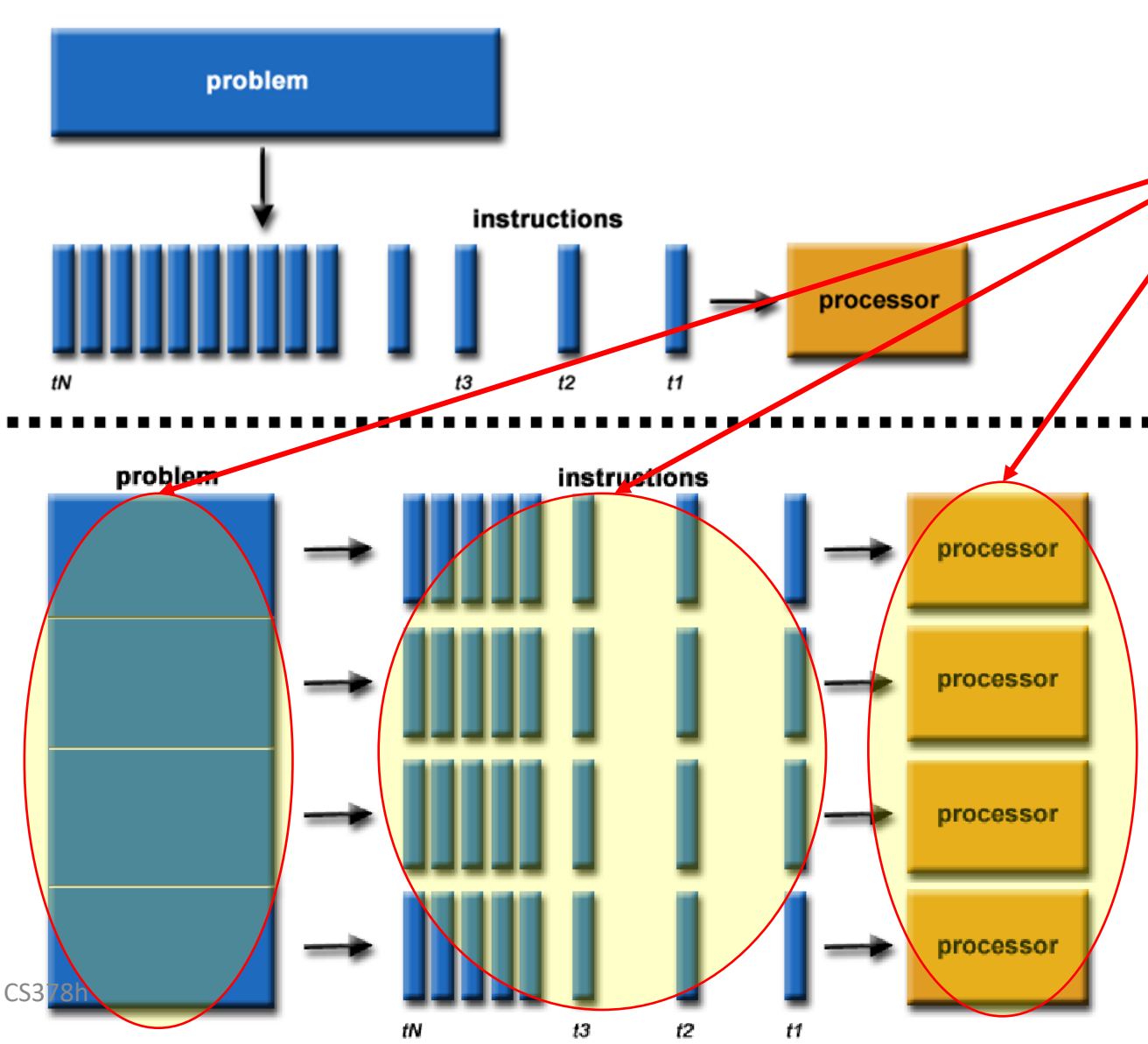


Key concerns:

- Programming model
- Execution Model

Multiple instructions in parallel

Serial vs. Parallel Program



Key concerns:

- Programming model
- Execution Model
- Performance/Efficiency

Multiple instructions in parallel

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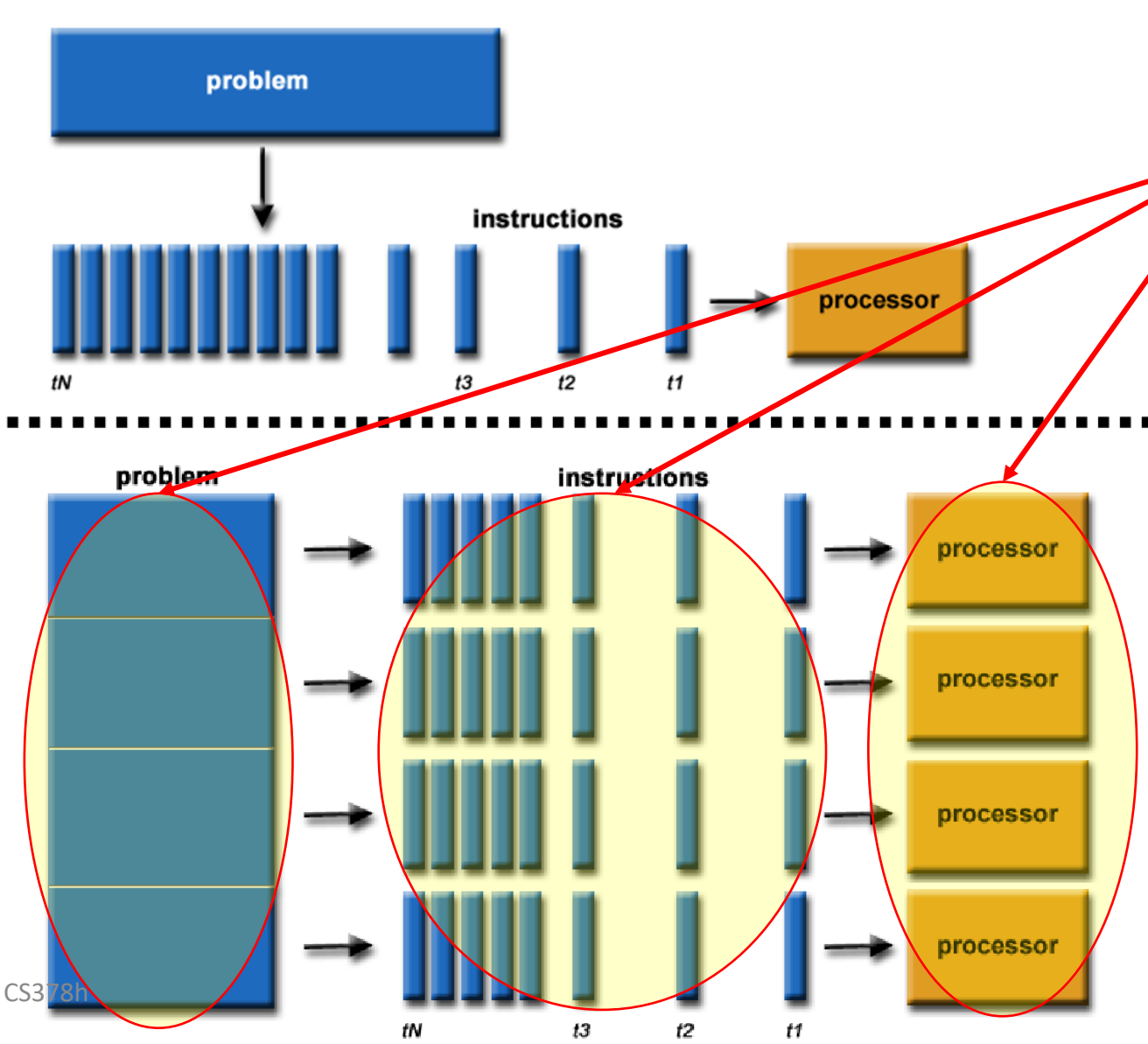
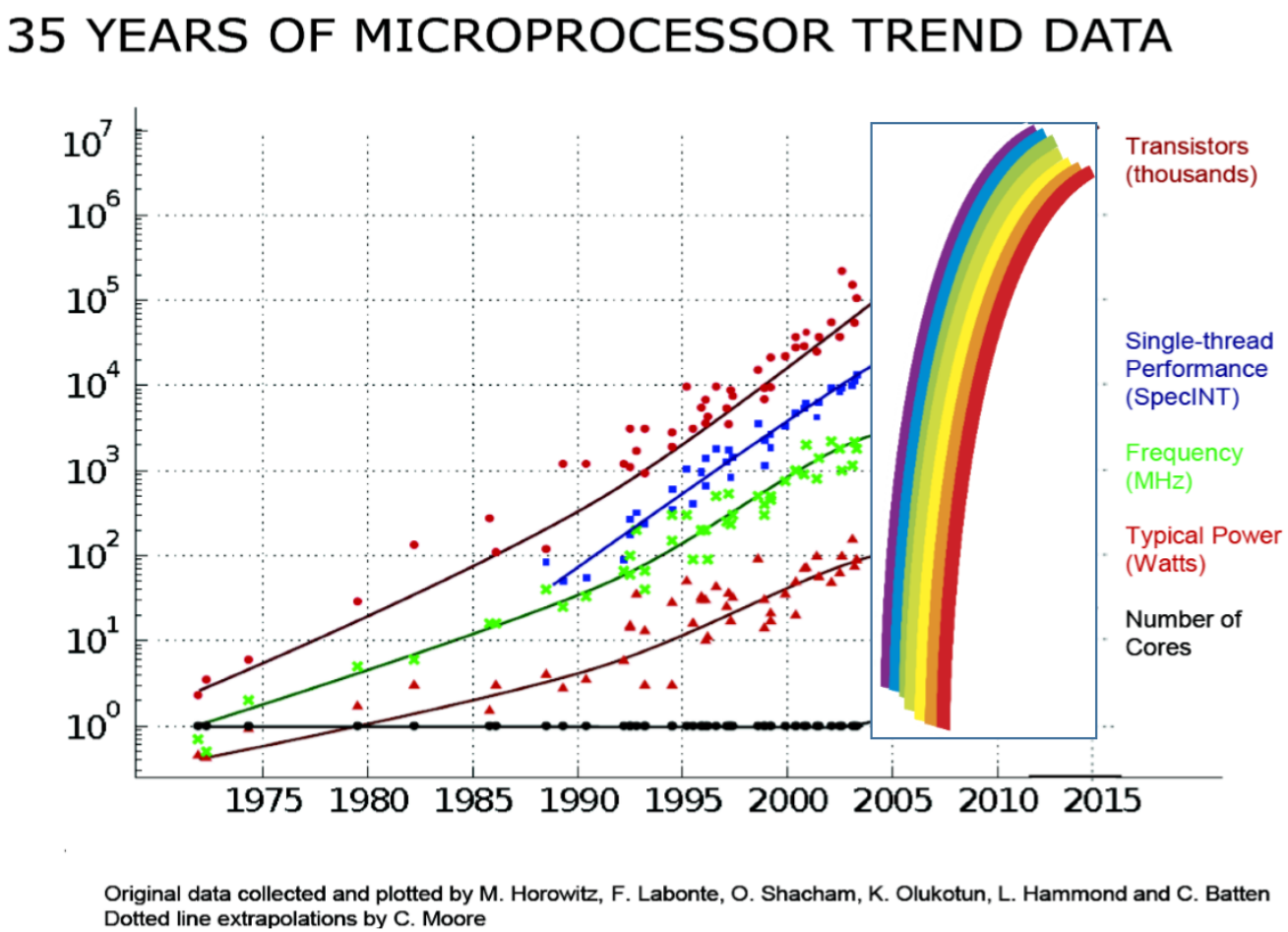


Key concerns:

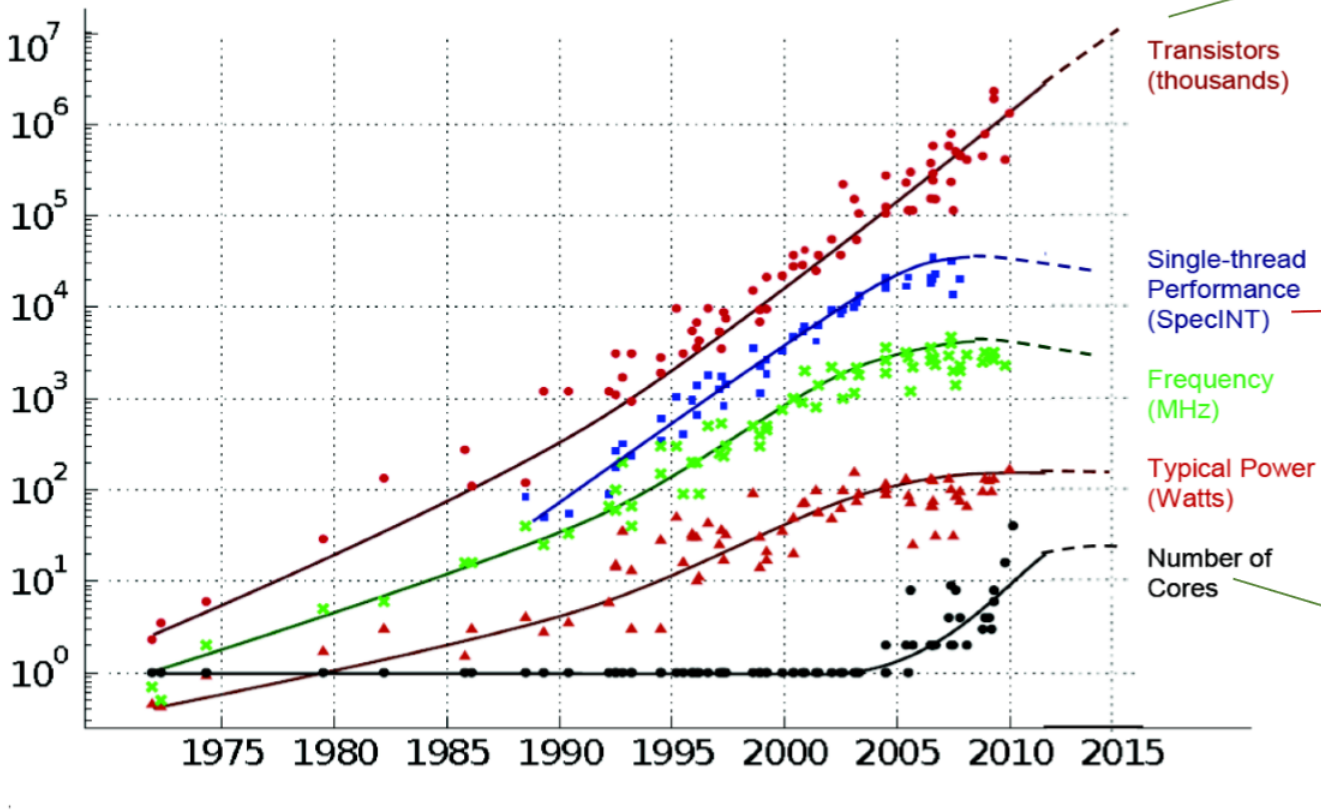
- Programming model
- Execution Model
- Performance/Efficiency
- Exposing parallelism

Multiple instructions in parallel

Free lunch…


35 YEARS OF MICROPROCESSOR TREND DATA
10^7
10^6
10^5
10^4
10^3
10^2
10^1
10^0
1975 1980 1985 1990 1995 2000 2005 2010 2015
Transistors (thousands)
Single-thread Performance (SpecINT)
Frequency (MHz)
Typical Power (Watts)
Number of Cores
Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten
Dotted line extrapolations by C. Moore

Free lunch – is over ☹



Transistor number grows (Moore's law)

Sequential performance no longer improves

Cores number grows

Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten
Dotted line extrapolations by C. Moore

Flynn’s Taxonomy

Flynn’s Taxonomy

SISD	SIMD
MISD	MIMD

Execution Models: Flynn’s Taxonomy

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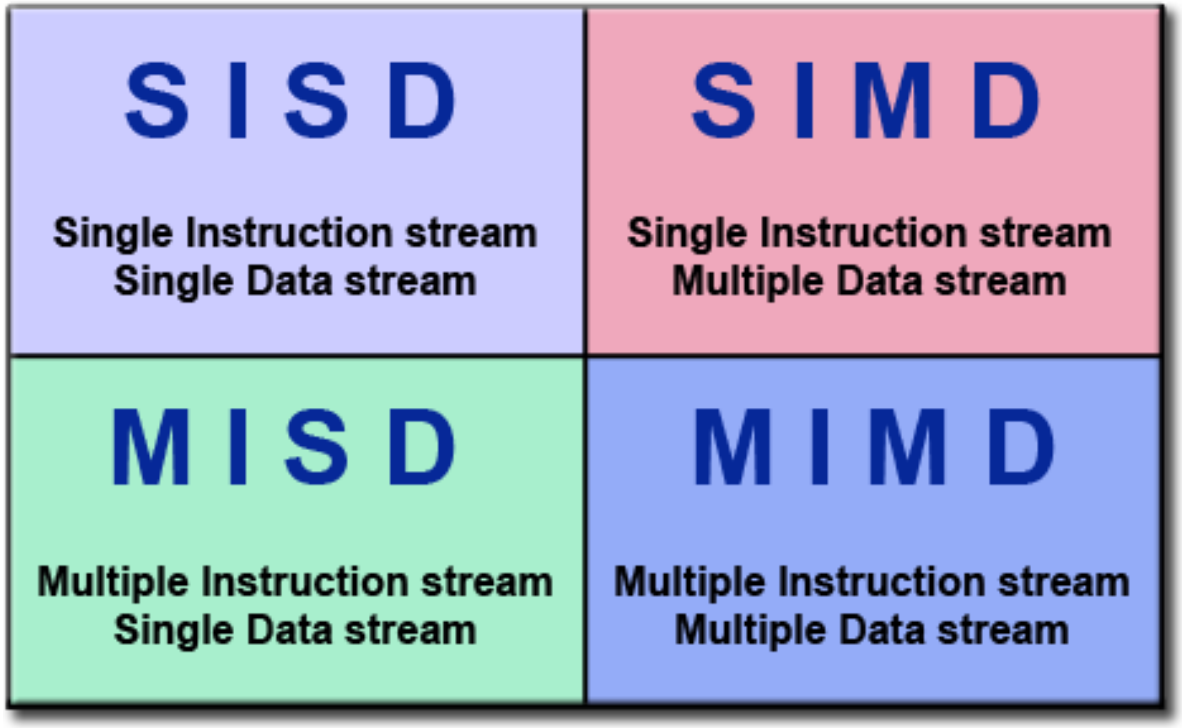
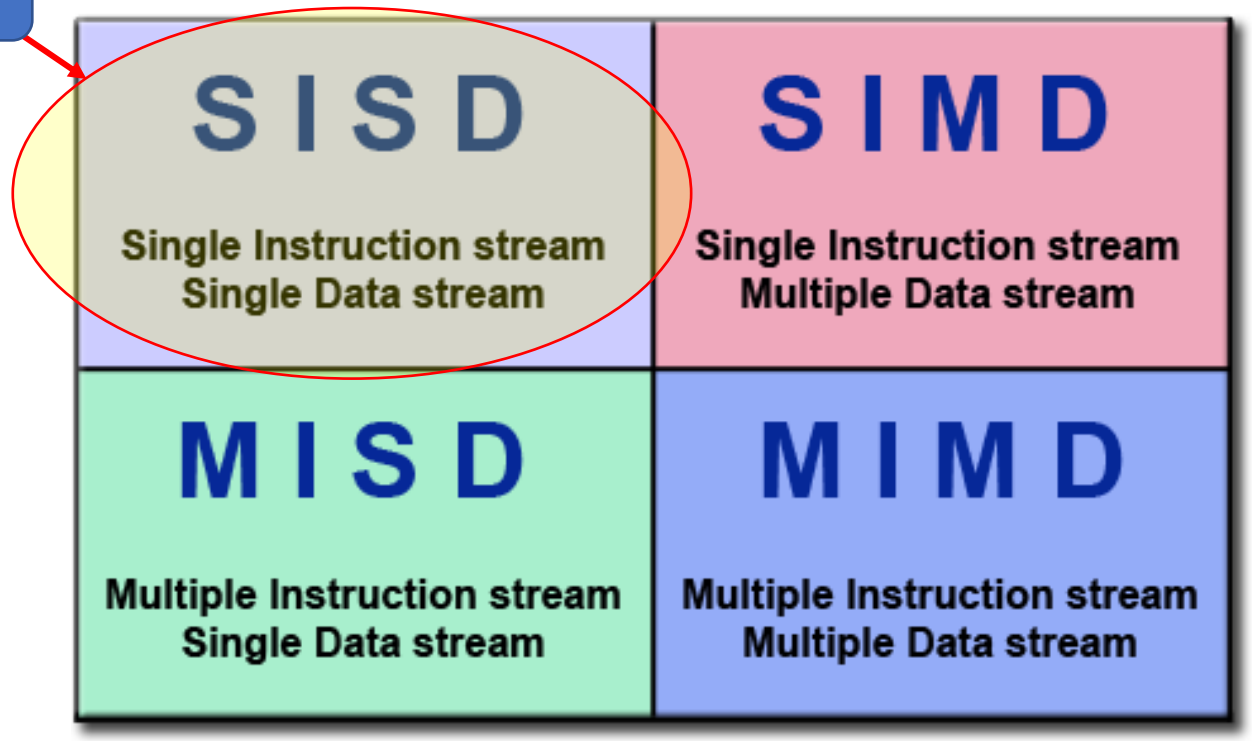


Execution Models: Flynn's Taxonomy

Normal Serial program



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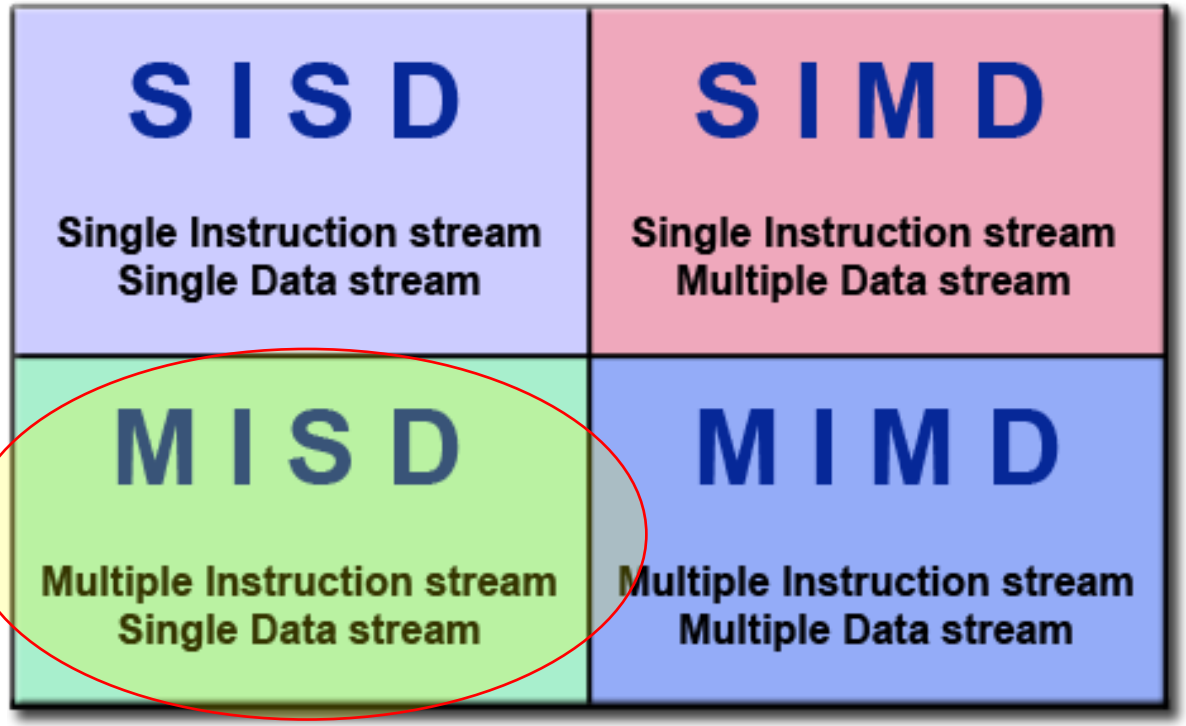
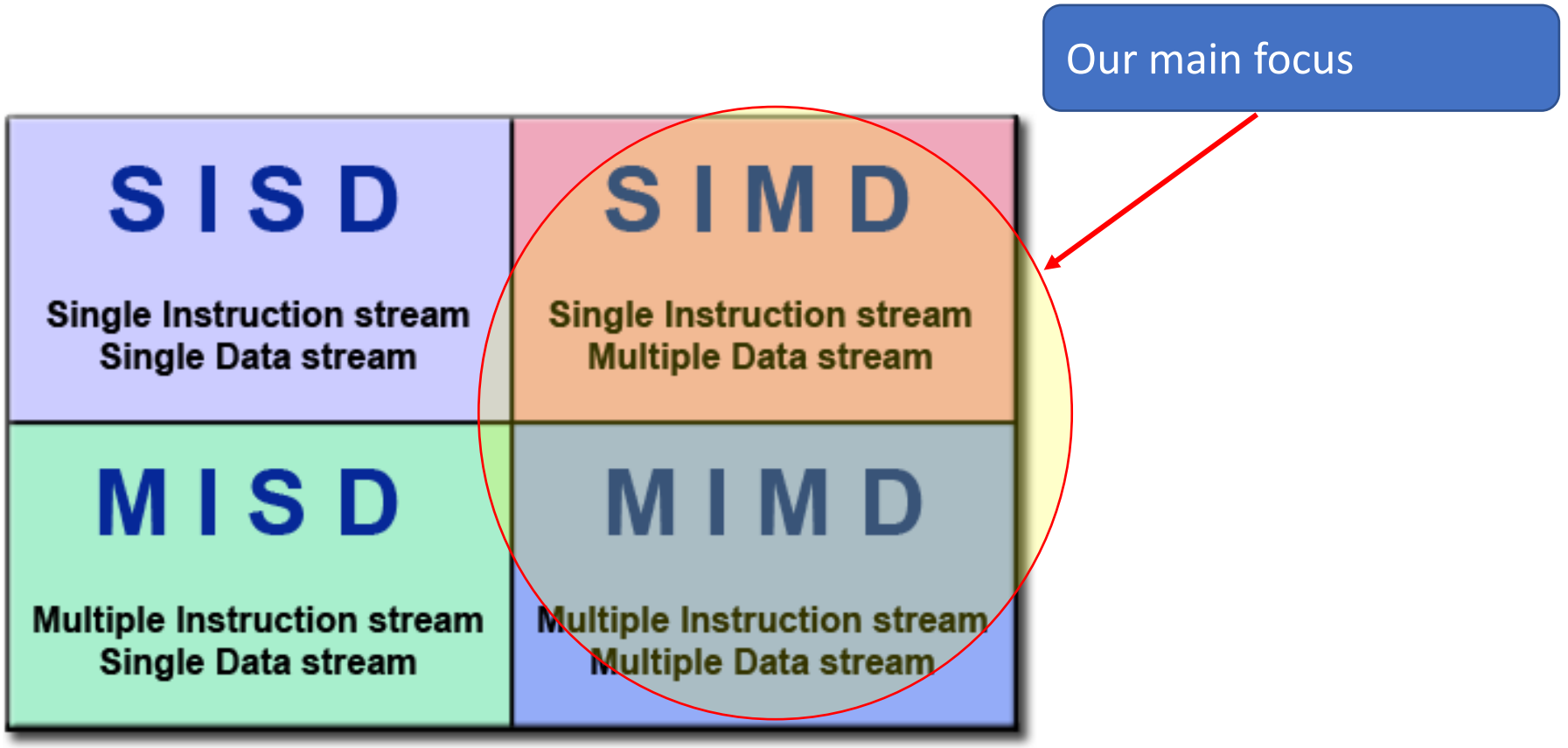


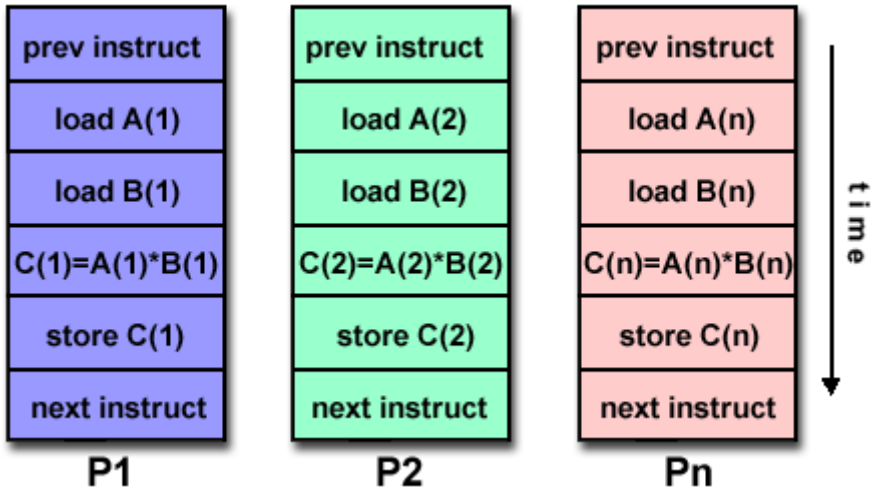
Uncommon architecture:
Fault – tolerance
Pipeline parallelism

Execution Models: Flynn's Taxonomy

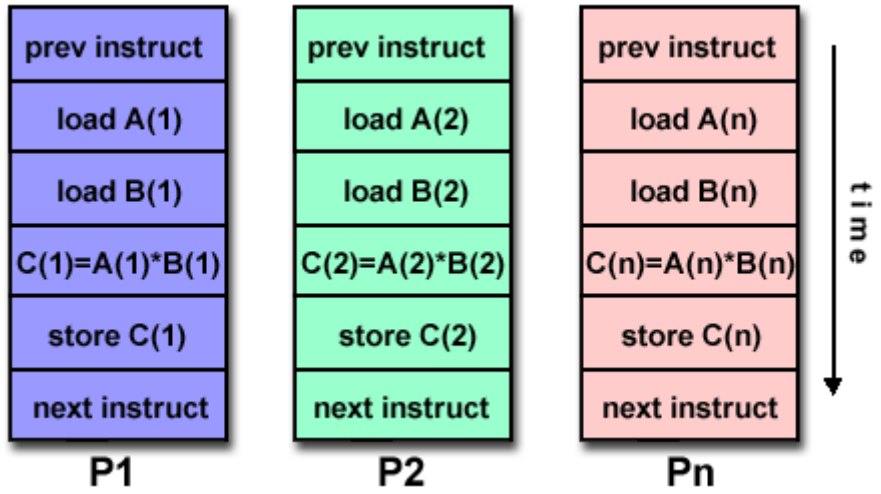


SIMD

SIMD

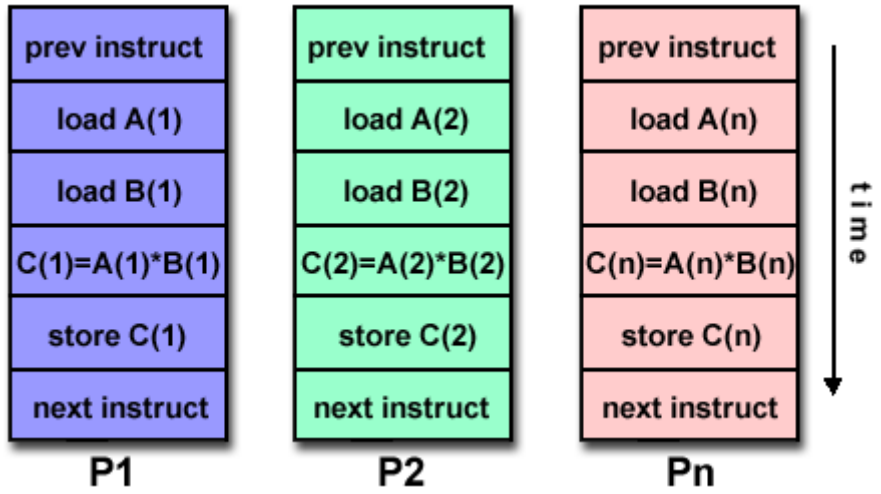

prev instruct
load A(1)
load B(1)
C(1)=A(1)*B(1)
store C(1)
next instruct
P1
prev instruct
load A(2)
load B(2)
C(2)=A(2)*B(2)
store C(2)
next instruct
P2
prev instruct
load A(n)
load B(n)
C(n)=A(n)*B(n)
store C(n)
next instruct
Pn
time

SIMD



- Example: vector operations (e.g., Intel SSE/AVX, GPU)

SIMD



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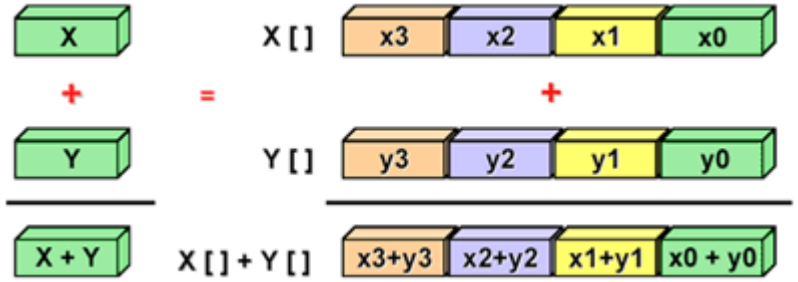

MIMD

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- Example: multi-core CPU

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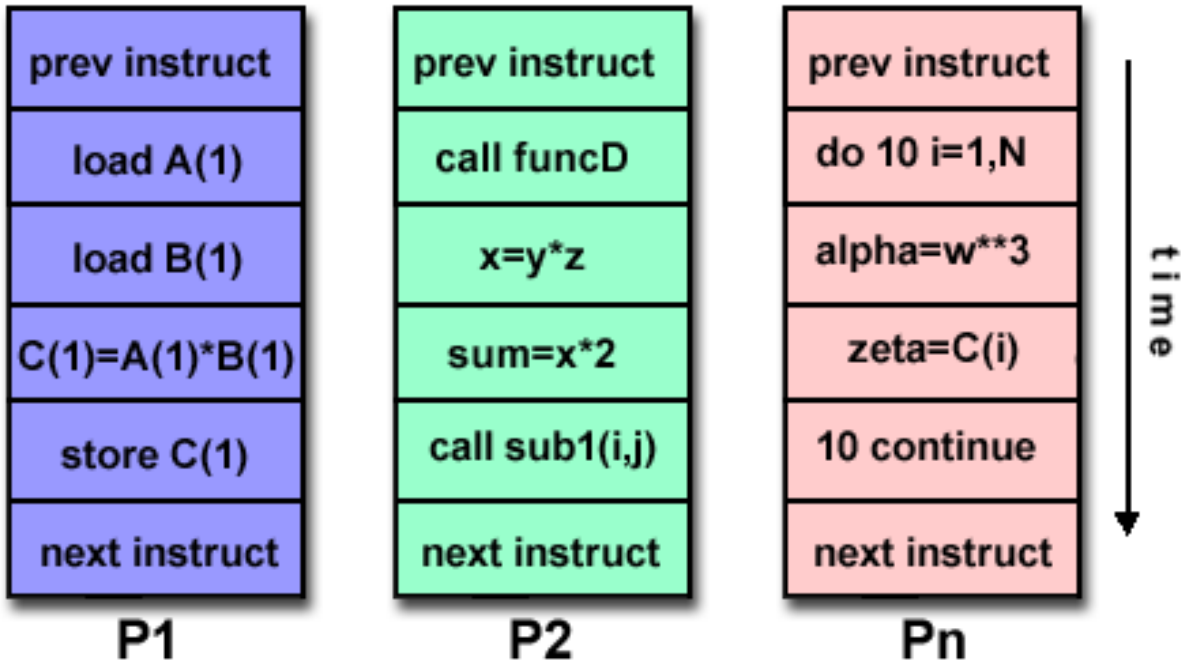

Problem Partitioning

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- Decomposition: Domain v. Functional

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  - SPMD
  - Input domain
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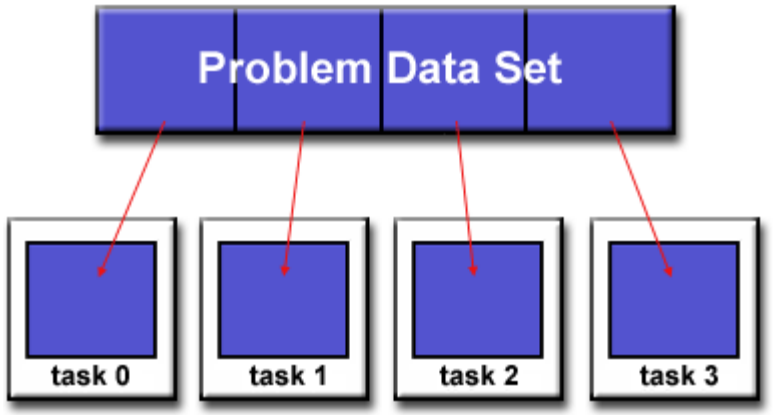

Problem Partitioning

- Decomposition: Domain v. Functional
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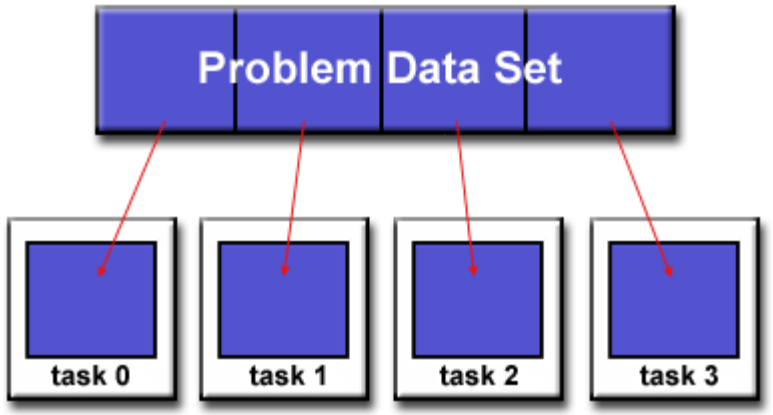
  - Independent Tasks
  - Pipelining



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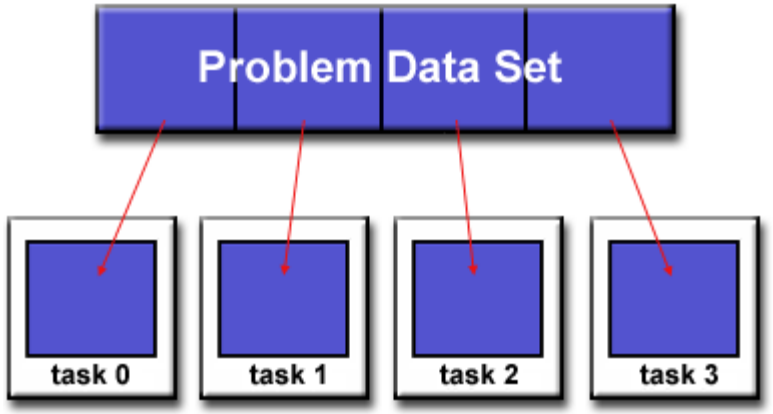
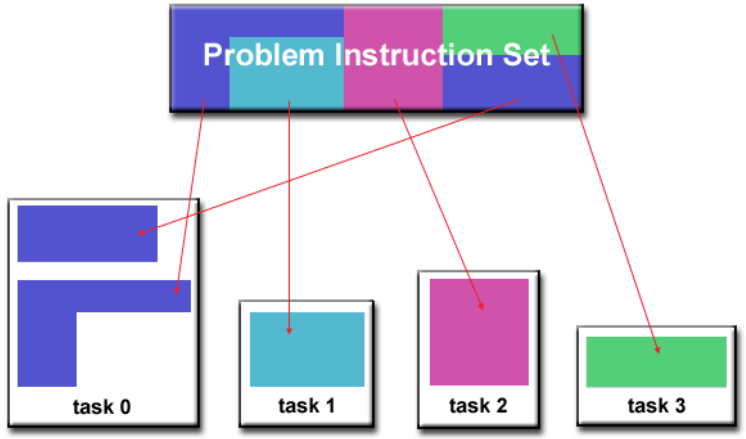
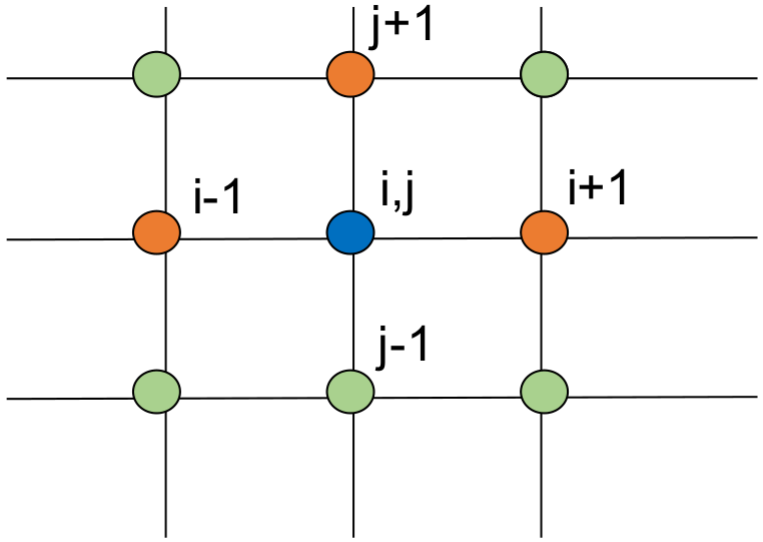




Game of Life

Game of Life

- Given a 2D Grid:
- $v_t(i,j) = F\left(v_{t-1}(of\ all\ its\ neighbors)\right)$



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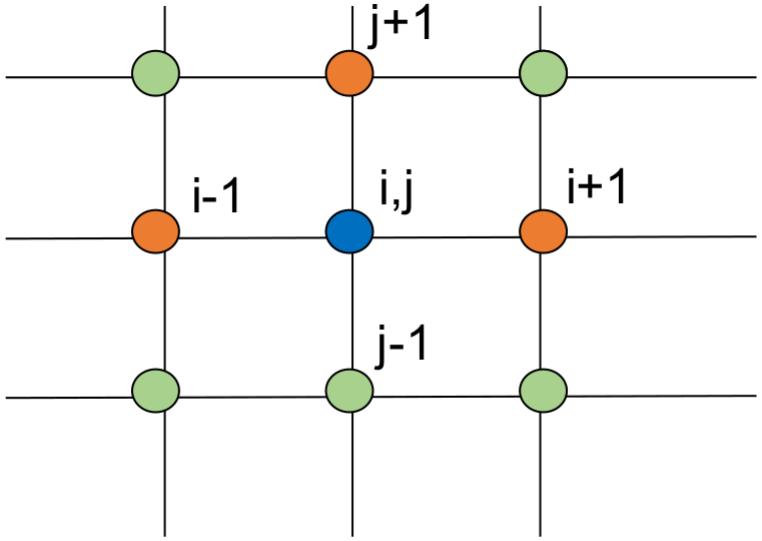
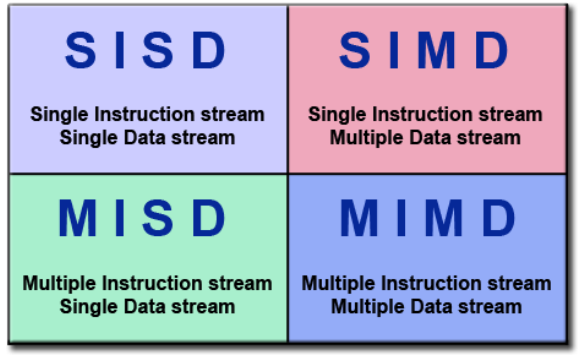


What model fits “best”?



Domain decomposition

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- Each CPU gets part of the input

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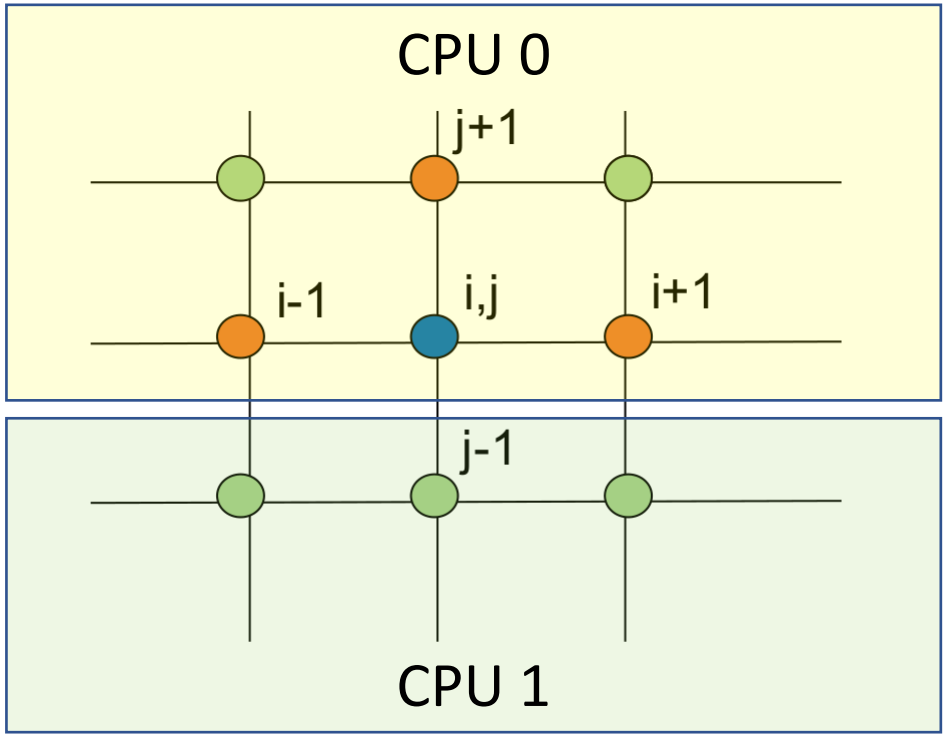

Domain decomposition

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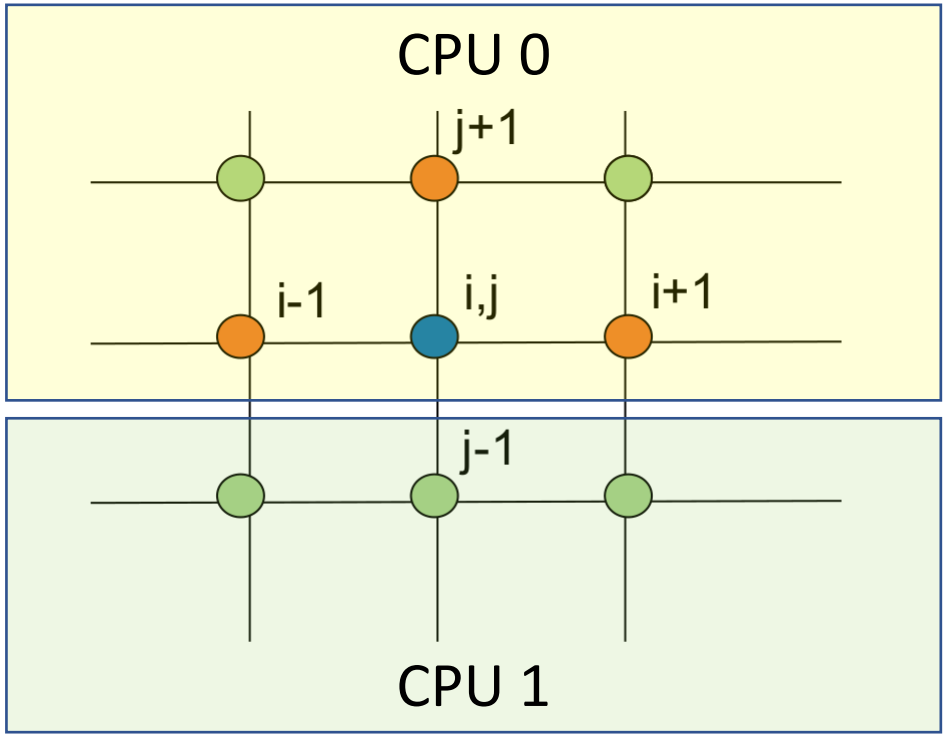
Issues?



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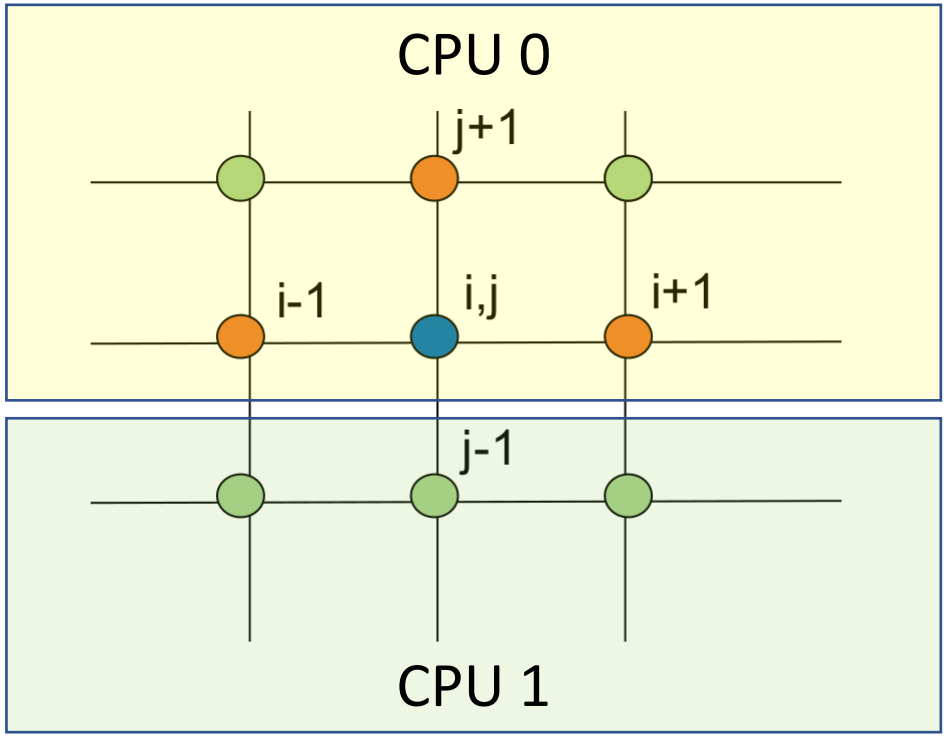

Issues?

- Accessing Data

Domain decomposition

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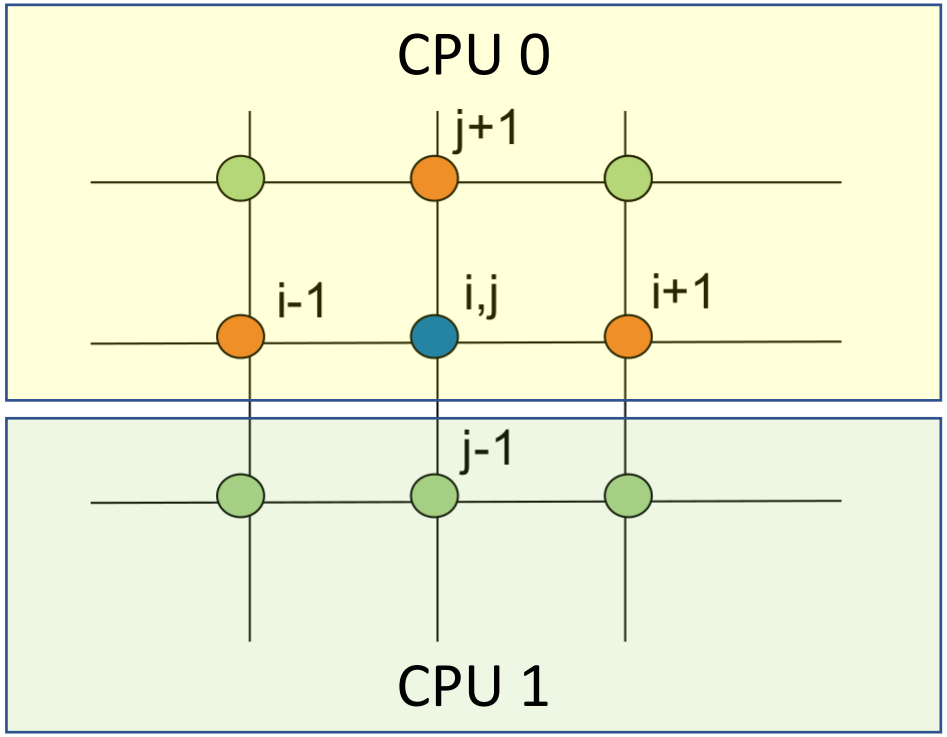

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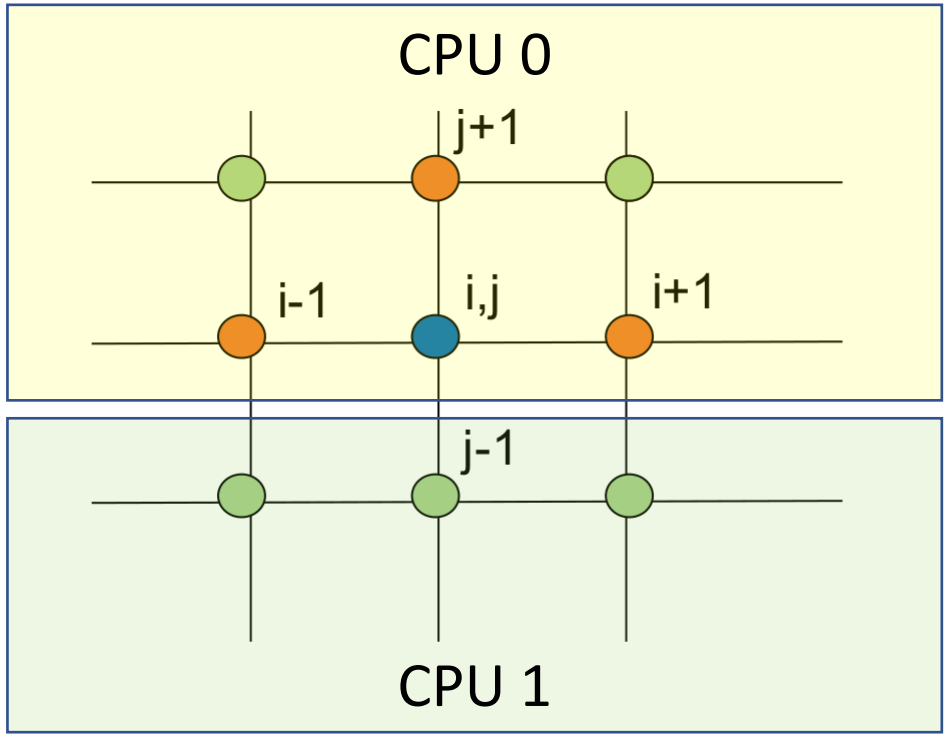

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    - Shared memory? Distributed?
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  - *Scalability vs Latency*

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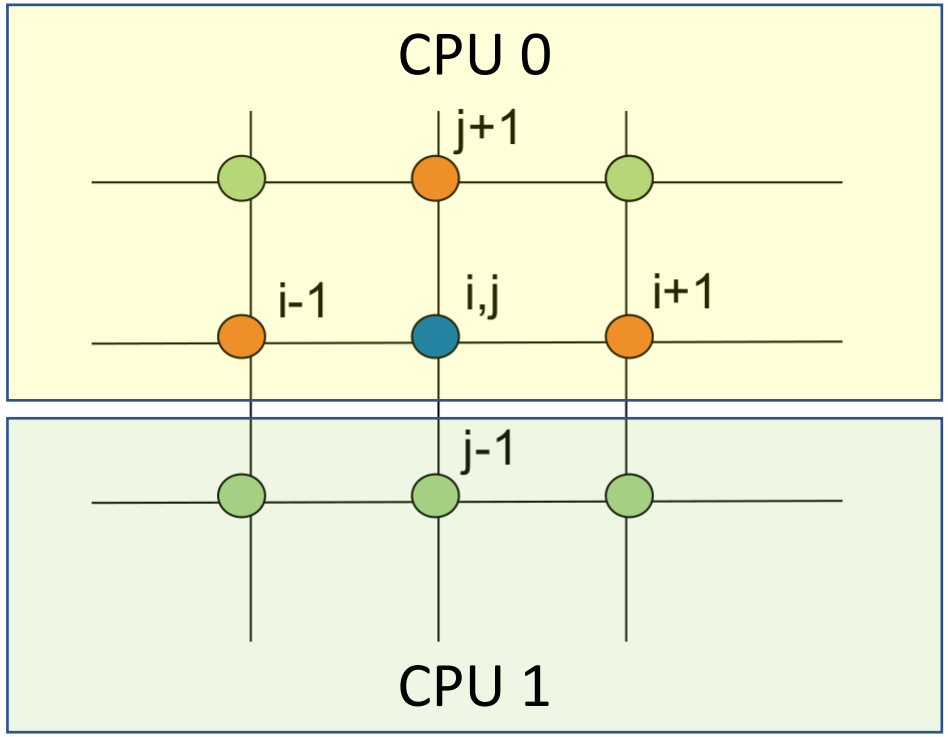

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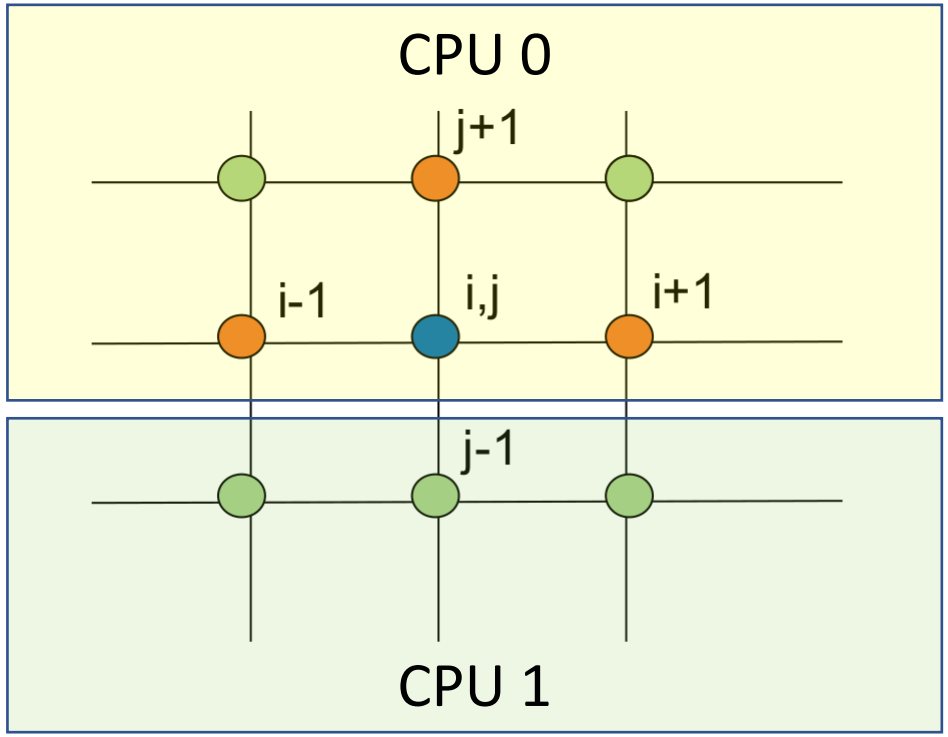

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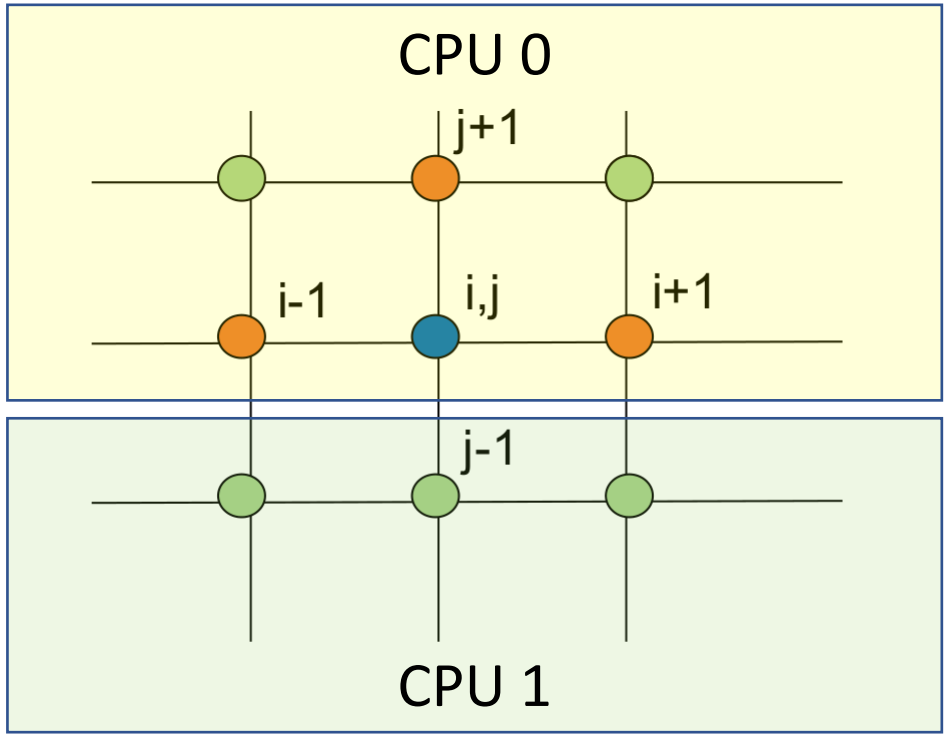

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- Correctness
  - order of reads and writes is non-deterministic
  - synchronization is required to enforce the order
  - *locks, semaphores, barriers, conditionals….*

Domain decomposition

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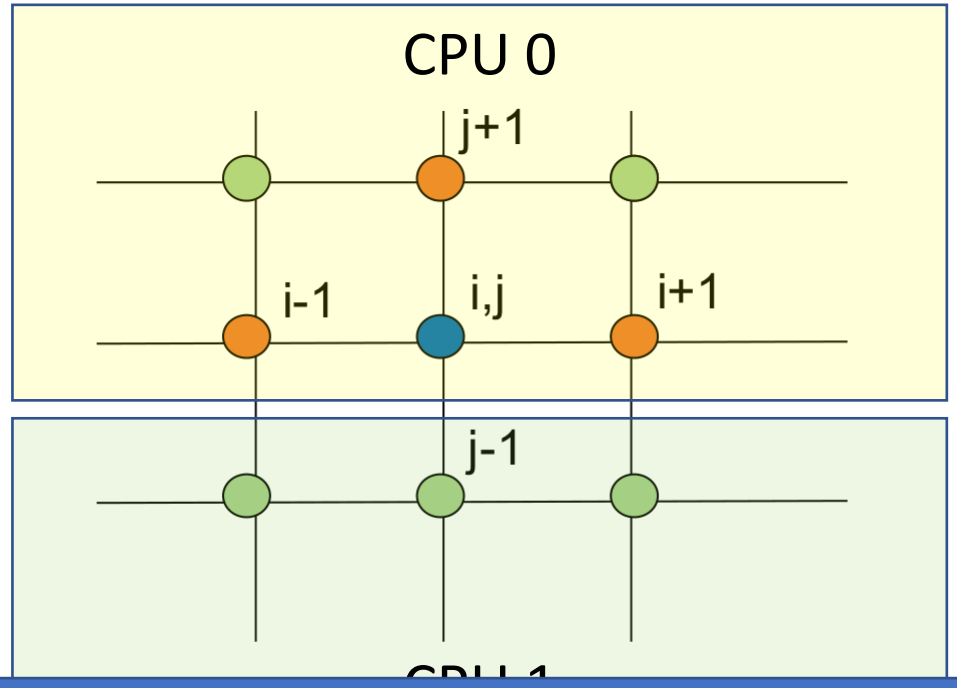

How could we do a functional decomposition?

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Lab #1

- Basic synchronization
- http://www.cs.utexas.edu/~rossbach/cs378/lab/lab0.html

- ***Start early!!!***

Questions?