Foundations: Concurrency Concerns Synchronization Basics

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CS378H

Today

- Questions?
- Administrivia
 - You've started Lab 1 right?
- Foundations
 - Parallelism
 - Basic Synchronization
 - Threads/Processes/Fibers, Oh my!
 - Cache coherence (maybe)
 - Acknowledgments: some materials in this lecture borrowed from
 - Emmett Witchel (who borrowed them from: Kathryn McKinley, Ron Rockhold, Tom Anderson, John Carter, Mike Dahlin, Jim Kurose, Hank Levy, Harrick Vin, Thomas Narten, and Emery Berger)
 - Mark Silberstein (who borrowed them from: Blaise Barney, Kunle Olukoton, Gupta)
 - Andy Tannenbaum
 - Don Porter
 - me...

•

Photo source: https://img.devrant.com/devrant/rant/r_10875_uRYQF.jpg

Multithreaded programming



Faux Quiz (answer any 2, 5 min)

- Who was Flynn? Why is her/his taxonomy important?
- How does domain decomposition differ from functional decomposition? Give examples of each.
- Can a SIMD parallel program use functional decomposition? Why/why not?
- What is an RMW instruction? How can they be used to construct synchronization primitives? How can sync primitives be constructed without them?





Michael J. Flynn

• Emeritus at Stanford



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- Proposed taxonomy in 1966 (!!)



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• (Thanks Wikipedia)





X AXIS:



X AXIS: Data Streams

Y AXIS: Instruction Streams	SISD Single Instruction stream Single Data stream	SIMD Single Instruction stream Multiple Data stream
	MISD Multiple Instruction stream Single Data stream	MIND Multiple Instruction stream Multiple Data stream

X AXIS:

Data Streams

• Domain Decomposition

- Domain Decomposition
 - SPMD
 - Input domain
 - Output Domain
 - Both

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 - MPMD
 - Independent Tasks
 - Pipelining



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• Each CPU gets part of the input

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• Each CPU gets part of the input



• Each CPU gets part of the input



Issues?

• Accessing Data

• Each CPU gets part of the input



- Accessing Data
 - Can we access v(i+1, j) from CPU 0

• Each CPU gets part of the input



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 - Can we access v(i+1, j) from CPU 0
 - ...as in a "normal" serial program?
 - Shared memory? Distributed?
 - Time to access v(i+1,j) == Time to access v(i-1,j) ?
 - Scalability vs Latency

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- Control
 - Can we assign one vertex per CPU?
 - Can we assign one vertex per process/logical task?
 - Task Management Overhead

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- Correctness
 - order of reads and writes is non-deterministic
 - synchronization is required to enforce the order
 - locks, semaphores, barriers, conditionals....

Load Balancing

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• Slowest task determines performance

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$$G = \frac{Computation}{Communication}$$

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- Fine-grain parallelism
 - G is small
 - Good load balancing
 - Potentially high overhead
 - Hard to get correct
- Coarse-grain parallelism
 - G is large
 - Load balancing is tough
 - Low overhead
 - Easier to get correct





 $G = \frac{Computation}{Communication}$

Performance: Amdahl's law

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- Speedup is bound by serial component
- Split program serial time ($T_{serial} = 1$) into
 - Ideally parallelizable portion: A
 - assuming perfect load balancing, identical speed, no overheads
 - Cannot be parallelized (serial) portion : 1 A
 - Parallel time:

$$T_{\text{parallel}} = \frac{A}{\#CPUs} + (1 - A)$$

$$Speedup(\#CPUs) = \frac{T_{serial}}{T_{parallel}} = \frac{1}{\frac{A}{\#CPUs} + (1 - A)}$$

Performance: Amdahl's law



$$Speedup(\#CPUs) = \frac{T_{serial}}{T_{parallel}} = \frac{1}{\frac{A}{\#CPUs} + (1 - A)}$$

L

X seconds



X seconds

my task	
X/2 seconds	X/2 seconds
Serial	Parallelizable



What makes something "serial" vs. parallelizable?







X/2 seconds

Serial



X/2 seconds X/2 seconds Parallelizable Parallelizable

Amdahl's law



X/4 seconds X/2 seconds Parallelizable Parallelizable

Amdahl's law



X/4 seconds X/2 seconds Parallelizable Parallelizable

Amdahl's law

End to end time: (X/2 + X/4) = (3/4)X seconds



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What is the "speedup" in this case?

$$Speedup = \frac{\text{serial run time}}{\text{parallel run time}} = \frac{1}{\frac{A}{\#CPUs} + (1 - A)} = \frac{1}{\frac{.5}{2 \text{ cpus}} + (1 - .5)} = 1.333$$









Speedup exercise





Serial















Speedup exercise





Speedup exercise







Amdahl Action Zone



NUMBER OF CPUS

Amdahl Action Zone



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Amdahl Action Zone



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- N = #CPUs, S = serial portion = 1 A
- Amdahl's law: $Speedup(N) = \frac{1}{\frac{A}{N}+S}$
 - Strong scaling: Speedup(N) calculated given total amount of work is fixed
 - Solve same problems faster when problem size is fixed and #CPU grows
 - Assuming parallel portion is fixed, speedup soon seizes to increase





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- Gustafson's law: Speedup(N) = S + (S-1)*N
 - Weak scaling: Speedup(N) calculated given that work per CPU is fixed
 - Work/CPU fixed when adding more CPUs keeps granularity fixed
 - Problem size grows: solve larger problems
 - Consequence: speedup upper bound is much higher





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Amdahl vs. Gustafson

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When is Gustavson's law a better metric? When is Amdahl's law a better metric?


Speedup





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- But usually just poor methodology
- Baseline: *best* serial algorithm



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Efficient **bubble sort**



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Efficient **bubble sort** •*Serial: 150s*



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Efficient **bubble sort** • Serial: 150s • Parallel 40s • Speedup: NO NO NO! $\frac{150}{40} = 3.75$?



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Efficient **bubble sort** •Serial: 150s •Parallel 40s •Speedup: **NO NO NO!** $\frac{150}{40} = 3.75$? •Serial quicksort: 30s



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Why insist on best serial algorithm as baseline?

Concurrency and Correctness

If two threads execute this program concurrently, how many different final values of X are there?

Initially, X == 0.



```
void increment() {
    int temp = X;
    temp = temp + 1;
    X = temp;
}
```



Schedules/Interleavings

Model of concurrent execution

- Interleave statements from each thread into a single thread
- If any interleaving yields incorrect results, synchronization is needed



Thread 1

Thread 2

Schedules/Interleavings

Model of concurrent execution

- Interleave statements from each thread into a single thread
- If any interleaving yields incorrect results, synchronization is needed



If X==0 initially, X == 1 at the end. WRONG result!

Locks fix this with Mutual Exclusion

```
void increment() {
    lock.acquire();
    int temp = X;
    temp = temp + 1;
    X = temp;
    lock.release();
}
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Mutual exclusion ensures only safe interleavings

• But it limits concurrency, and hence scalability/performance

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Is mutual exclusion a good abstraction?

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 - Simple to develop
 - Easy to avoid deadlock
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 - Greater concurrency
 - Greater code complexity
 - Potential deadlocks
 - Not composable
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 - Which lock to lock?

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```
// WITH FINE-GRAIN LOCKS
void move(T s, T d, Obj key){
  LOCK(s);
  LOCK(d);
  tmp = s.remove(key);
  d.insert(key, tmp);
  UNLOCK(d);
  UNLOCK(s);
}
```

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Thread 0	Thread 1	
move(a, b, key1);		
		•

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DEADLOCK!

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 - If a thread i is in entry section, then there is a bound on the number of times that other threads are allowed to enter the critical section before thread i's request is granted

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Entry section

Exit section

Critical section

Non-critical section


Review: correctness conditions

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Mutex, spinlock, etc. are ways to implement

Did we get all the important conditions? Why is correctness defined in terms of locks? Theorem: Every property is a combination of a safety property and a liveness property. -Bowen Alpern & Fred Schneider https://www.cs.cornell.edu/fbs/publications/defliveness.pdf

Entry section

Exit section

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Non-critical section

int lock_value = 0; int* lock = &lock_value;

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```
Lock::Acquire() {
while (*lock == 1)
; //spin
*lock = 1;
}
```

int lock_value = 0; int* lock = &lock_value;

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Lock::Acquire() {
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Lock::Release() { *lock = 0; }

int lock_value = 0; int* lock = &lock_value;

```
Lock::Acquire() {
while (*lock == 1)
; //spin
*lock = 1;
}
```

Lock::Release() {
 *lock = 0;
}

What are the problem(s) with this?

- ➤ A. CPU usage
- ➢ B. Memory usage
- C. Lock::Acquire() latency
- D. Memory bus usage
- E. Does not work

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Completely and utterly broken. How can we fix it?

Lock::Release() {
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