Foundations: Synchronization Execution Abstractions

Chris Rossbach

CS378H Fall 2018

9/10/18

Today

- Questions?
- Administrivia
  - Lab 1 due sooner than you'd like
- Foundations
  - Threads/Processes/Fibers
  - Cache coherence (maybe)

- Acknowledgments: some materials in this lecture borrowed from
  - Emmett Witchel (who borrowed them from: Kathryn McKinley, Ron Rockhold, Tom Anderson, John Carter, Mike Dahlin, Jim Kurose, Hank Levy, Harrick Vin, Thomas Narten, and Emery Berger)
  - Andy Tannenbaum

Faux Quiz (answer any 2, 5 min)

- What is the maximum possible speedup of a 75% parallelizable program on 8 CPUs
- What is super-linear speedup? List two ways in which super-linear speedup can occur.
- What is the difference between strong and weak scaling?
- Define Safety, Liveness, Bounded Waiting, Failure Atomicity
- What is the difference between processes and threads?
- What's a fiber? When and why might fibers be a better abstraction than threads?

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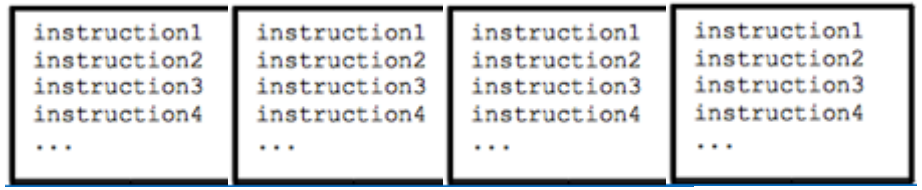
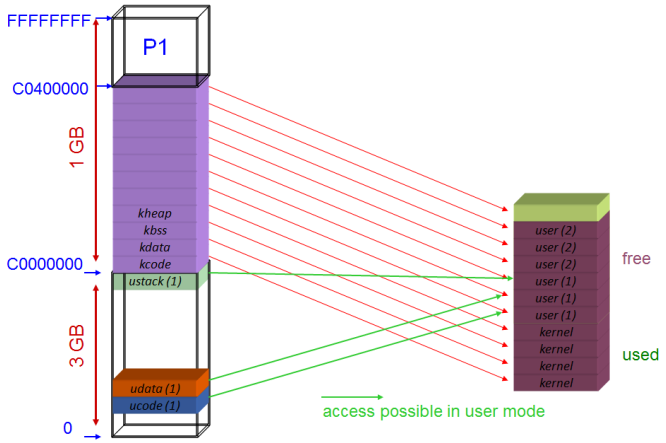
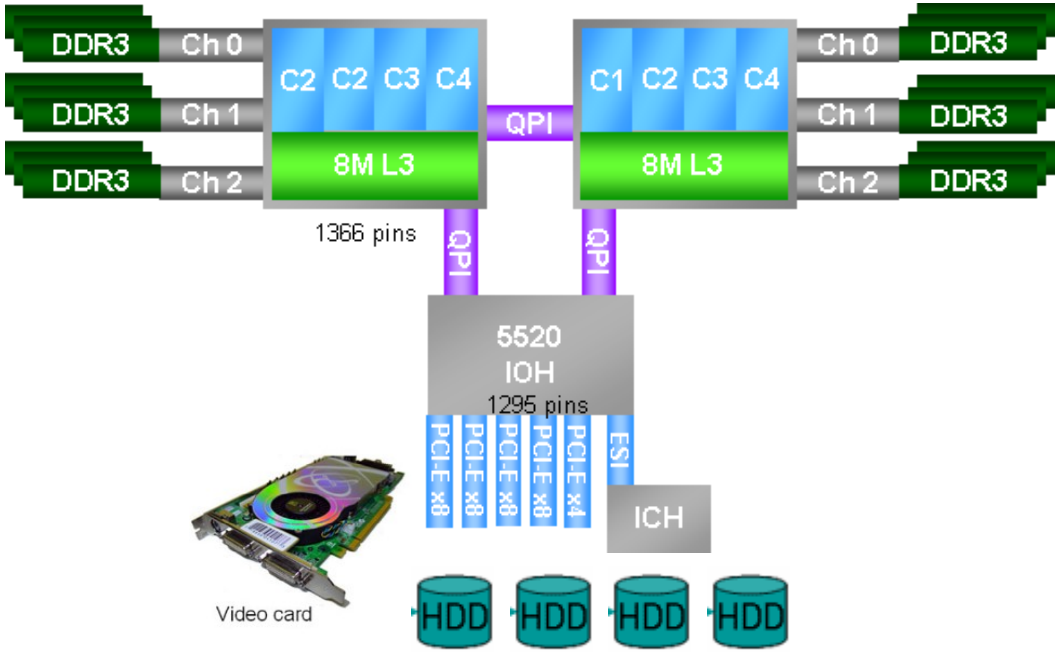
Processes and Threads and Fibers…

- Abstractions
- Containers
- State
  - Where is shared state?
  - How is it accessed?
  - Is it mutable?







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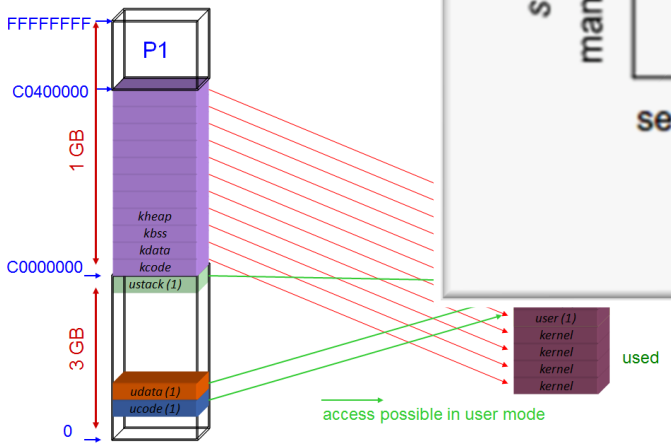
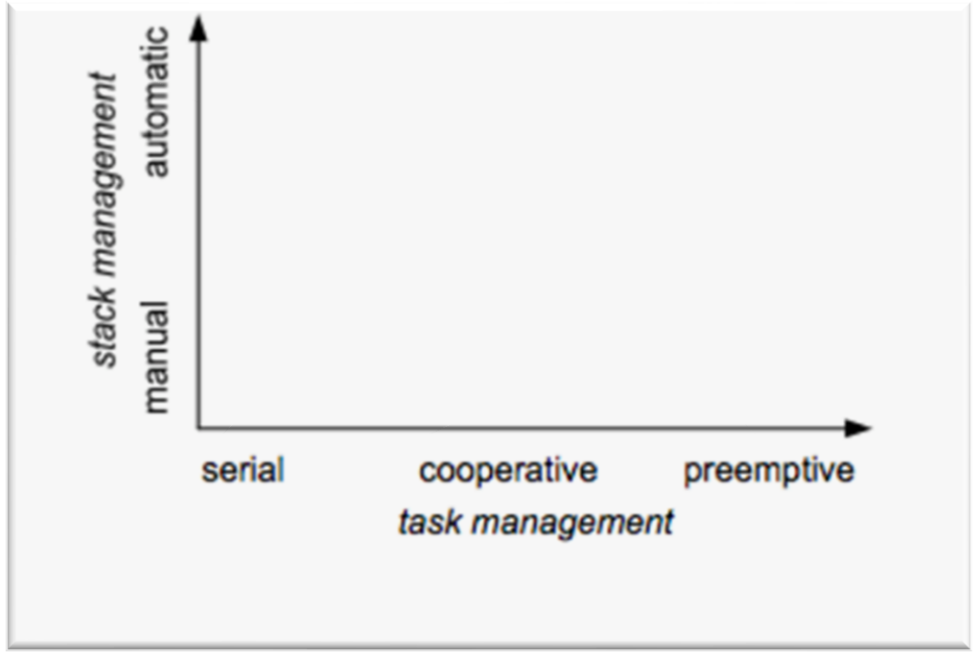
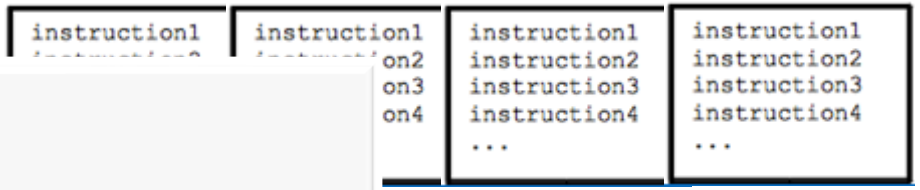
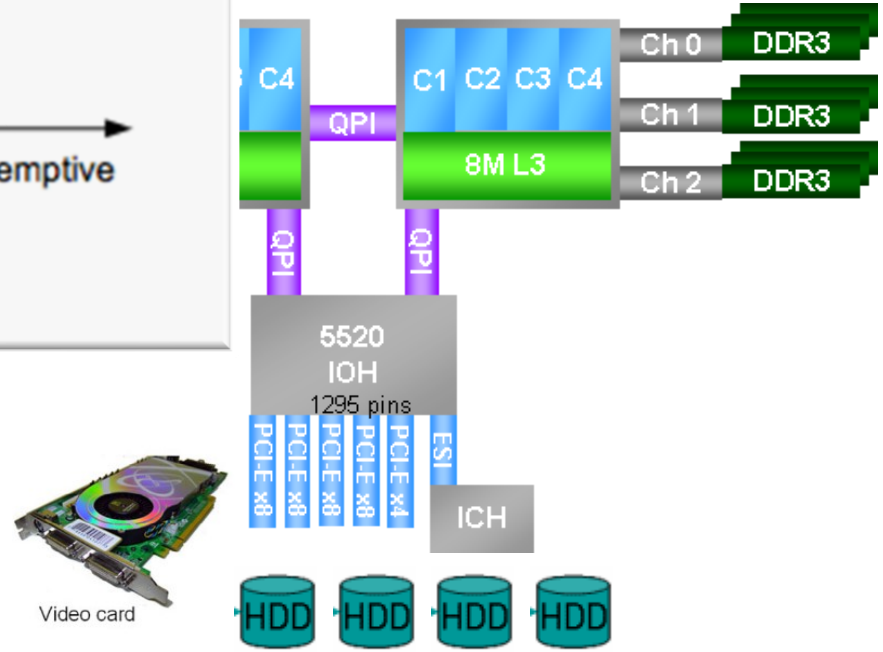
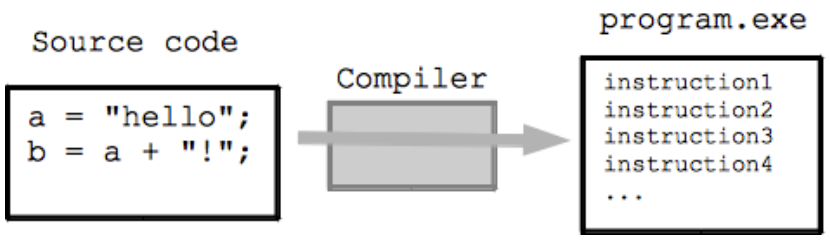








Programming and Machines: a mental model




```
struct machine_state{
  uint64 pc;
  uint64 Registers[16];
  uint64 cr[6]; // control registers cr0-cr4 and EFER on AMD
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} machine;
while(1) {
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void execute_instruction(i) {
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  case add_rr:
   machine.Registers[i.dst] += machine.Registers[i.src];
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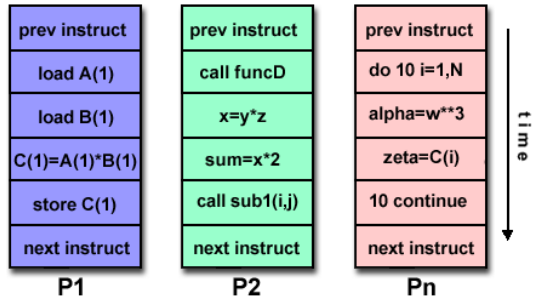
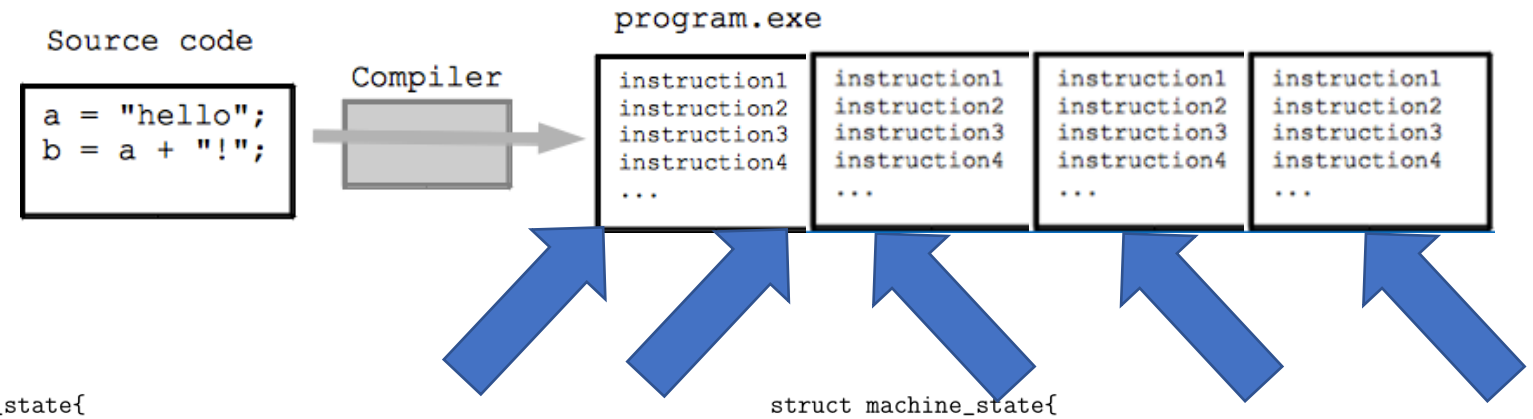
Parallel Machines: a mental model



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Processes

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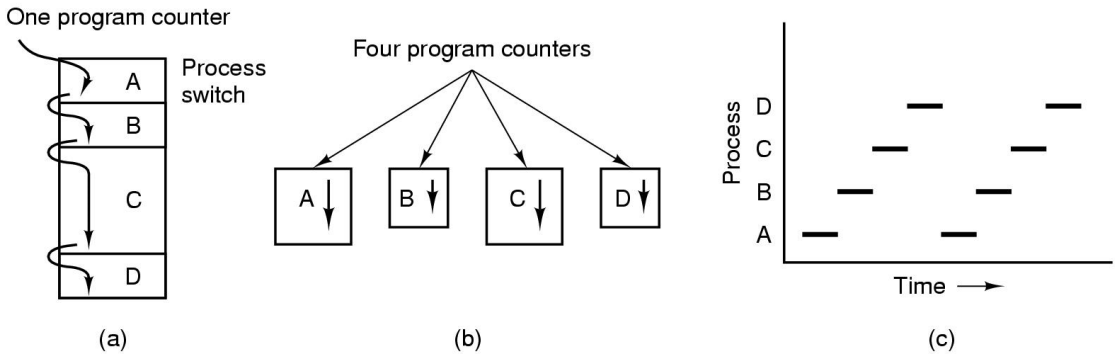

- Multiprogramming of four programs
- Conceptual model of 4 independent, sequential processes
- Only one program active at any instant

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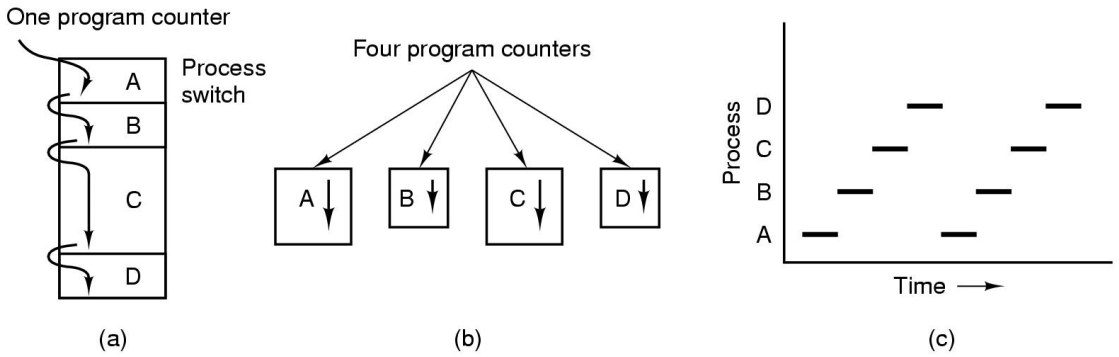

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Implementation

Process management	**Memory management**	**File management**
Registers	Pointer to text segment	Root directory
Program counter	Pointer to data segment	Working directory
Program status word	Pointer to stack segment	File descriptors
Stack pointer		User ID
Process state		Group ID
Priority		
Scheduling parameters		
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Parent process		
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Signals		
Time when process started		
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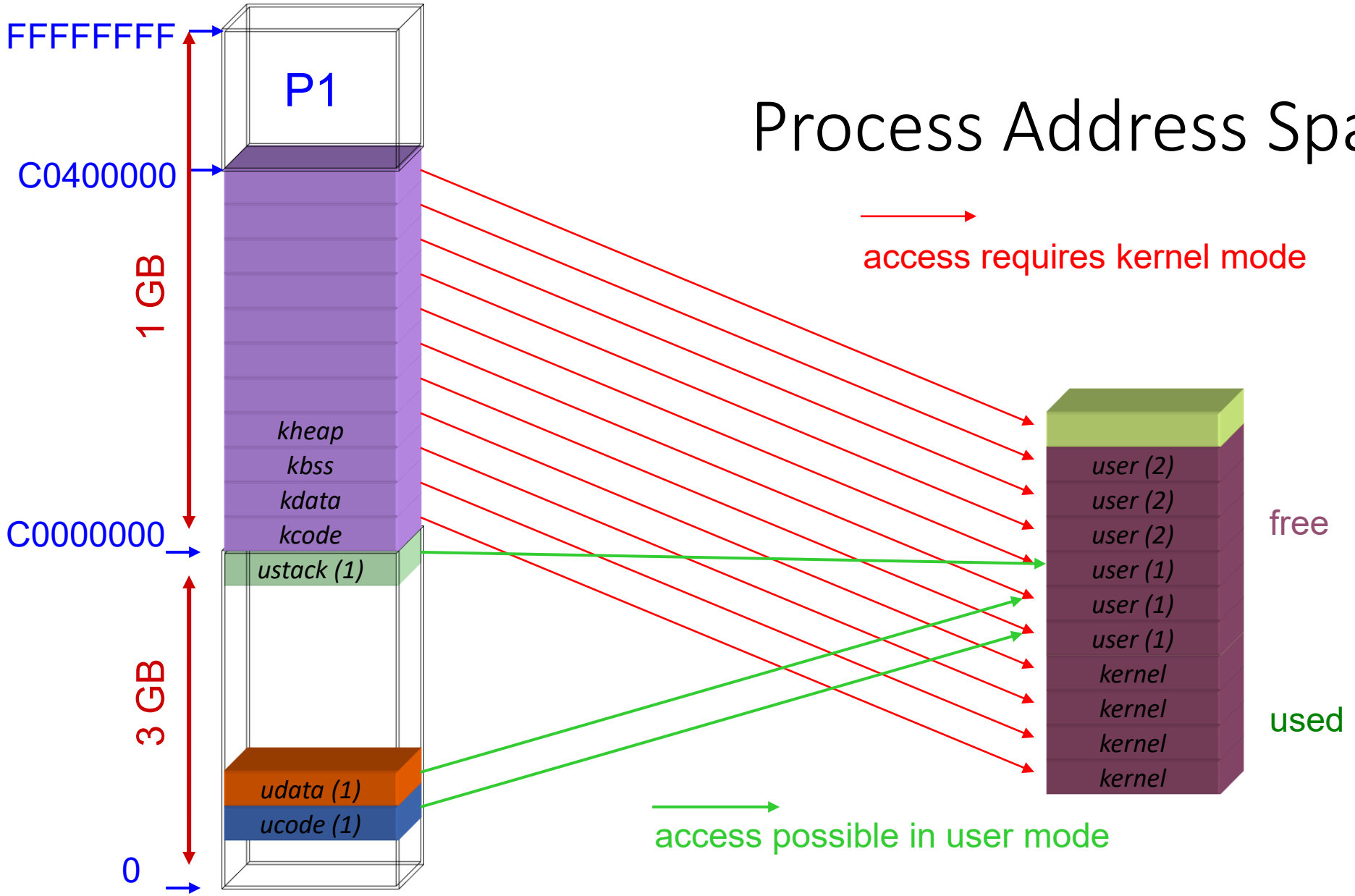
Children's CPU time		
Time of next alarm		

Process Address Space



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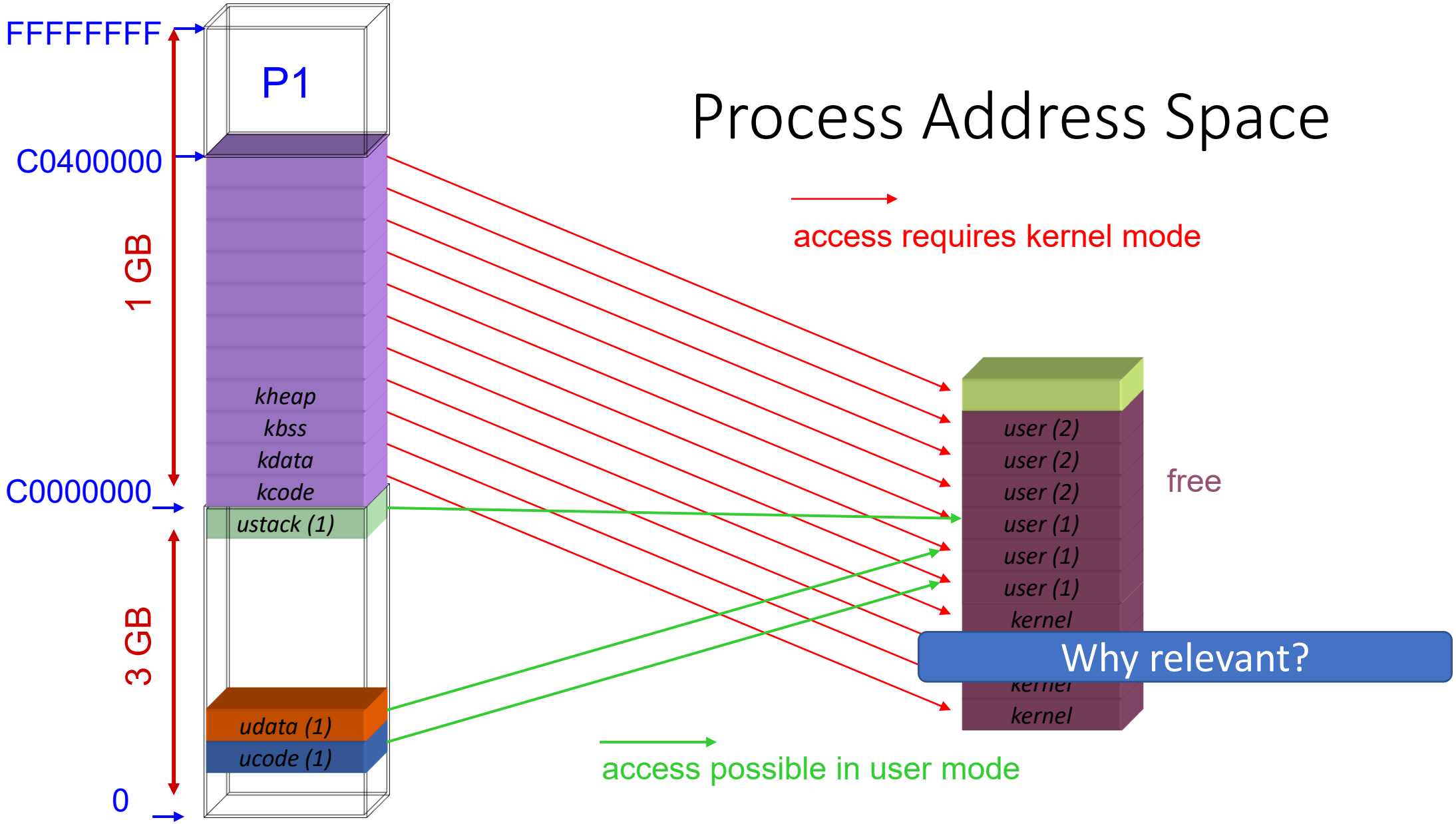

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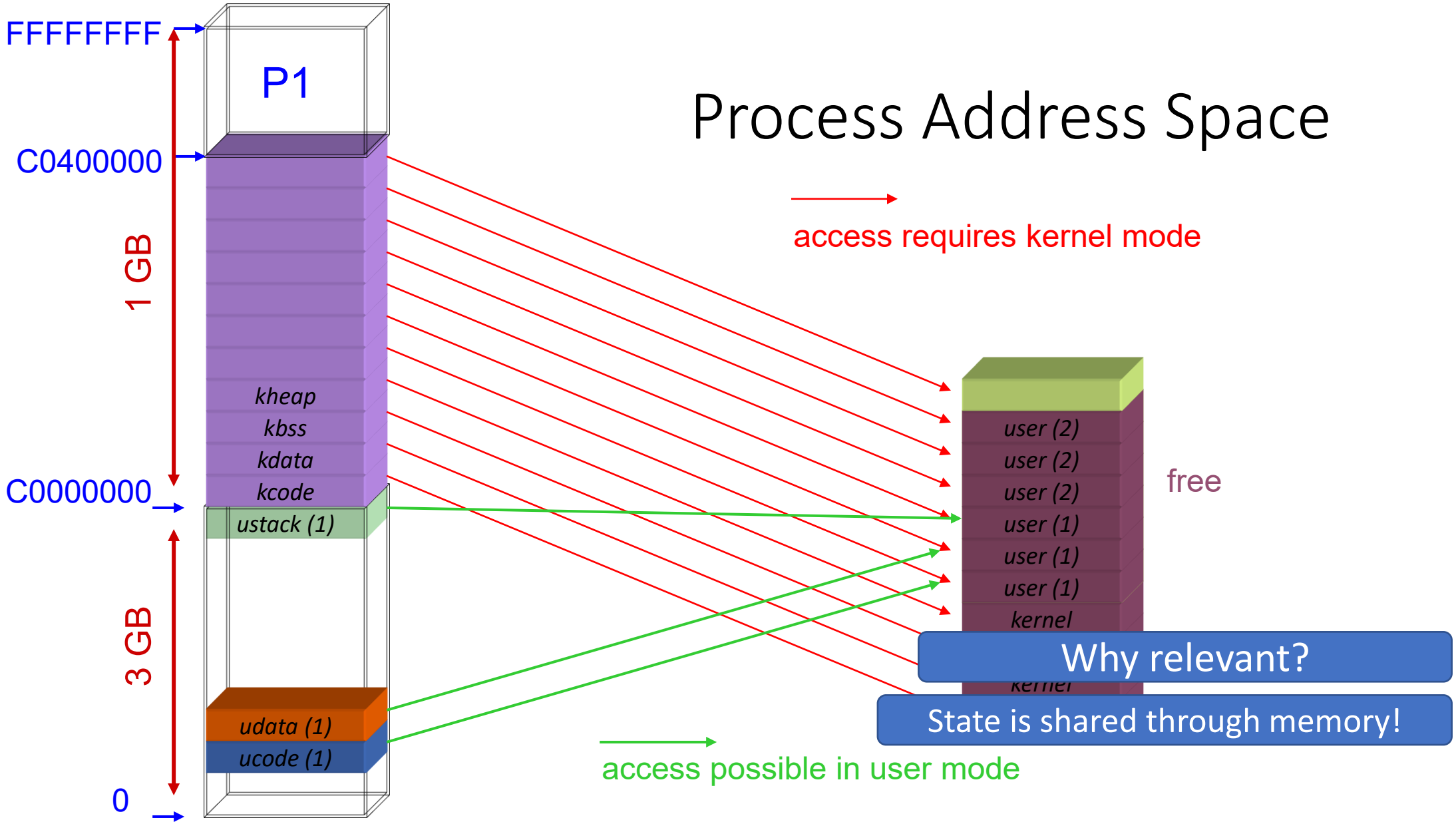

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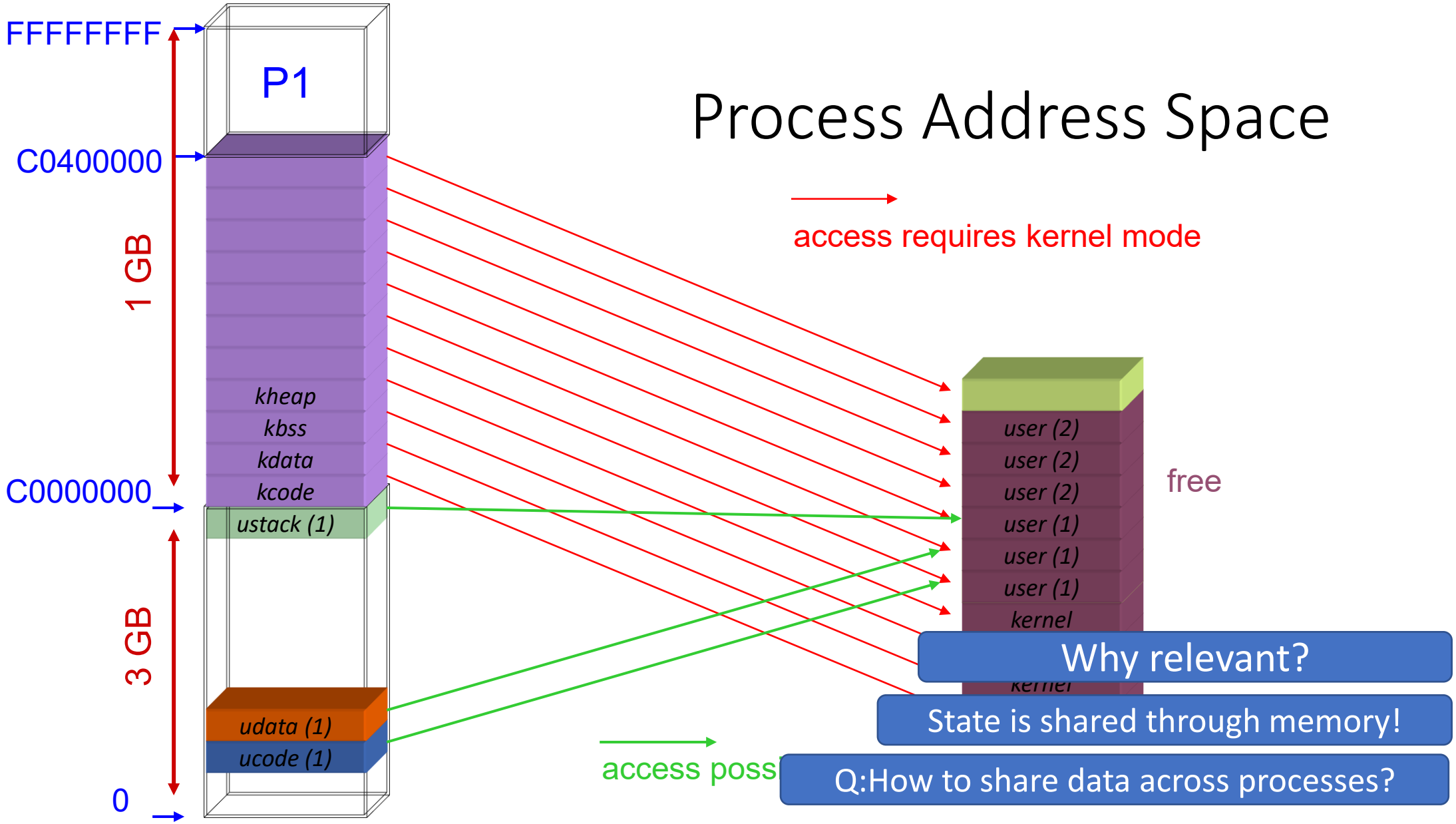

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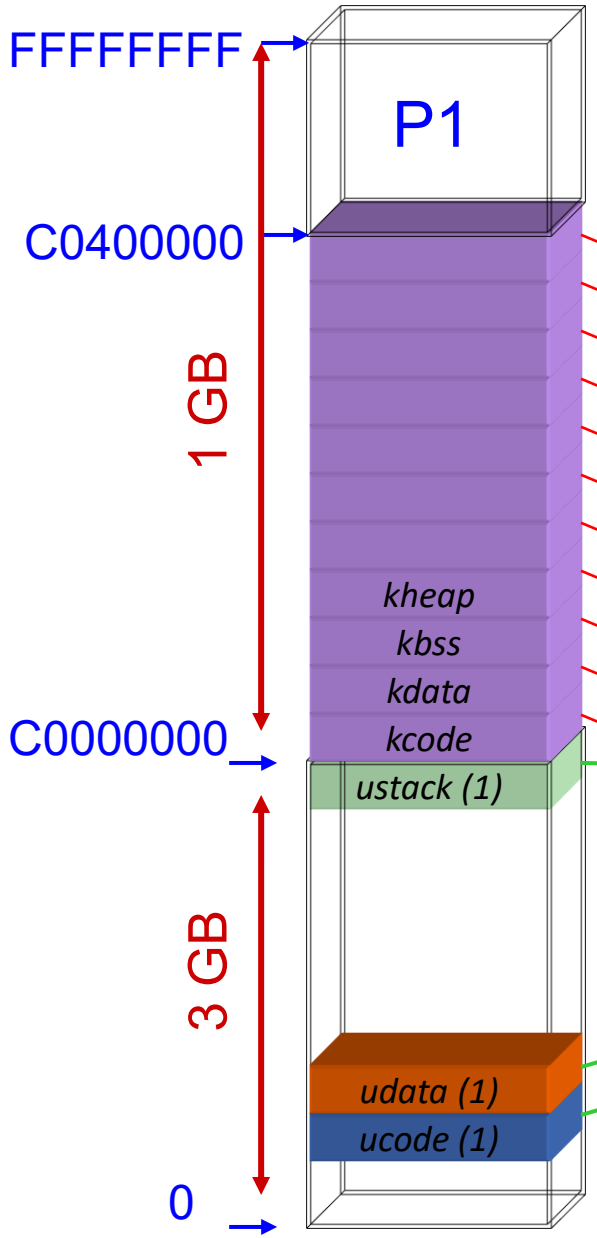
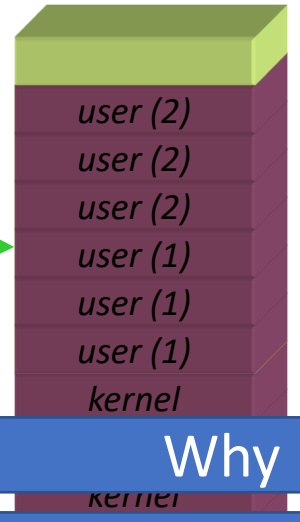


access requires kernel mode



free

access poss

Why relevant?

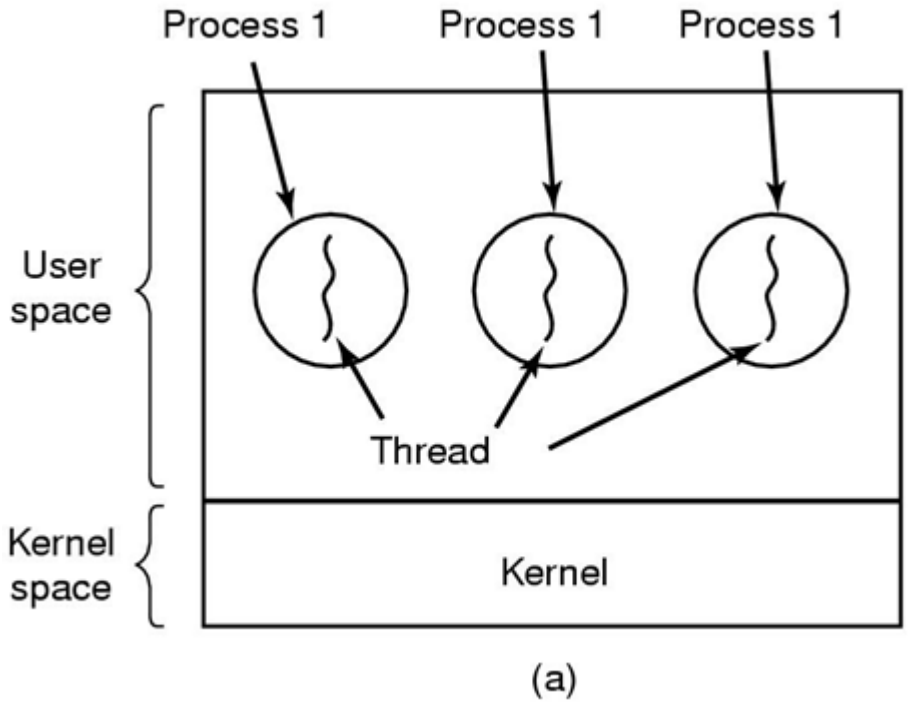
State is shared through memory!

Q:How to share data across processes?

Anyone see another issue?

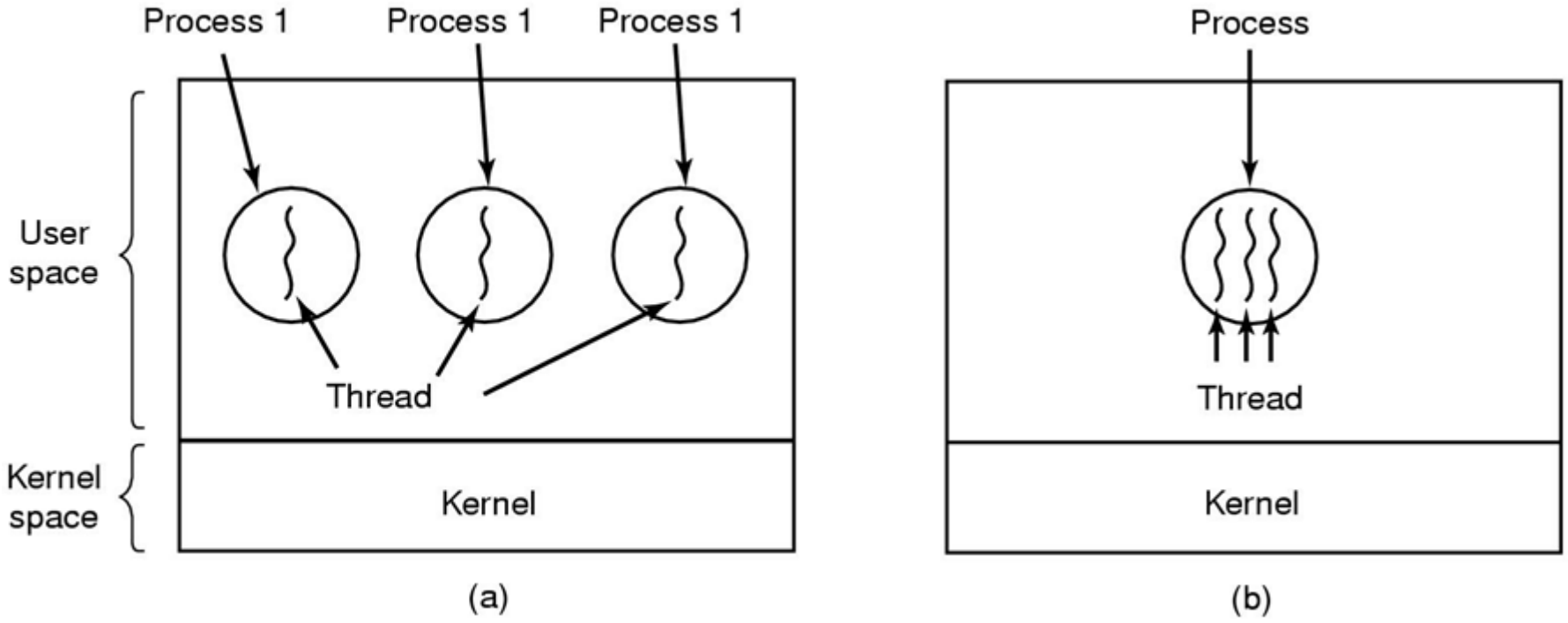
Abstractions for Concurrency

Abstractions for Concurrency



(a) Three processes each with one thread

Abstractions for Concurrency



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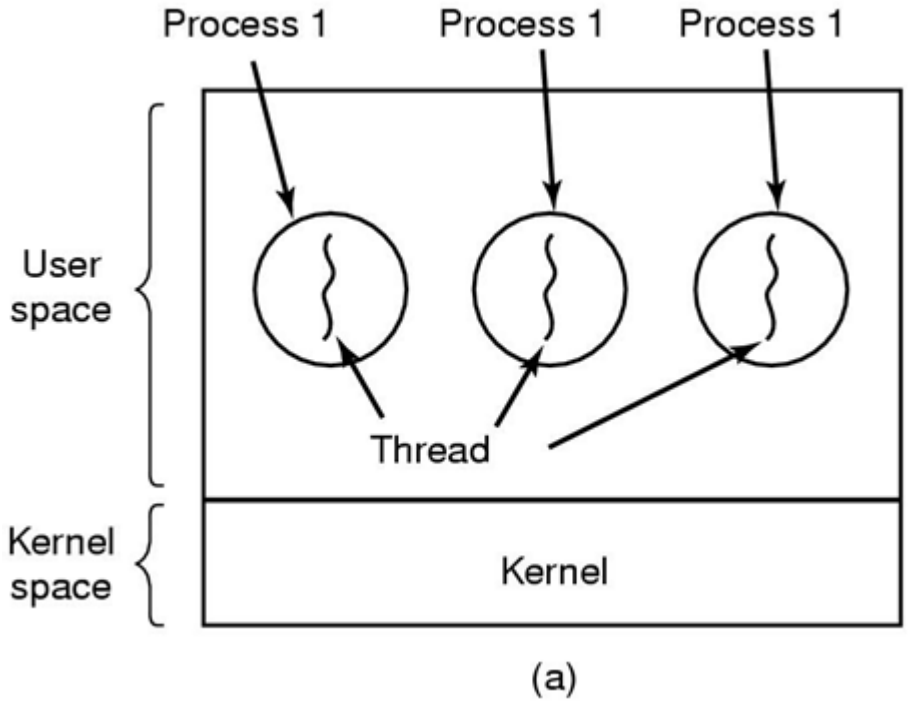

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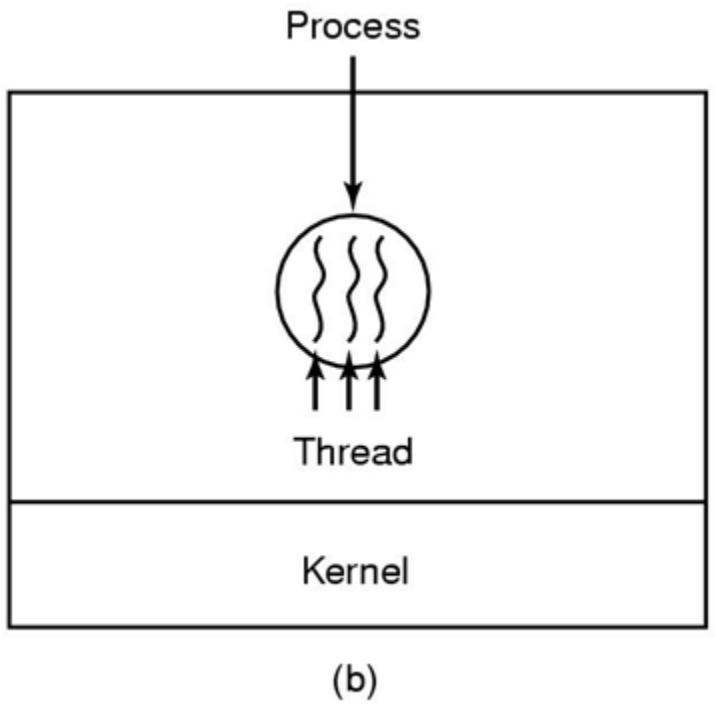

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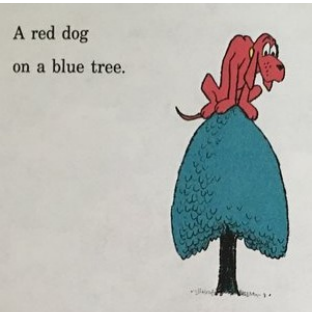

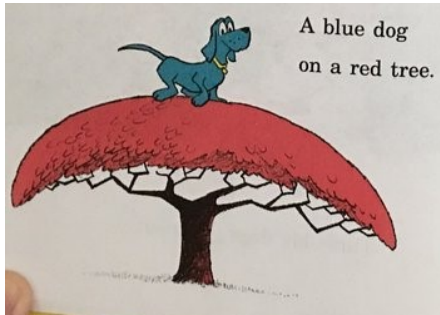

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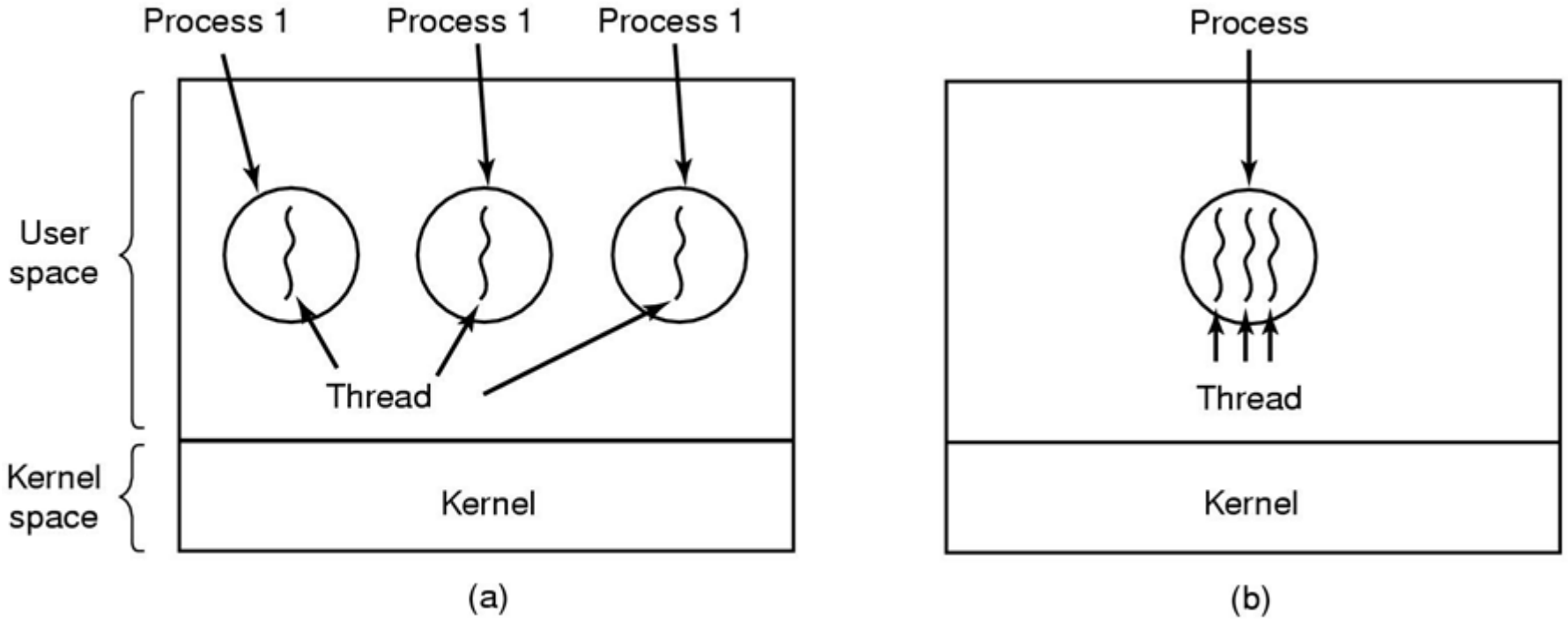

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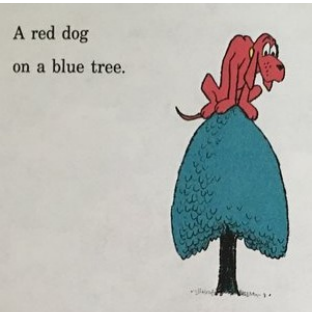

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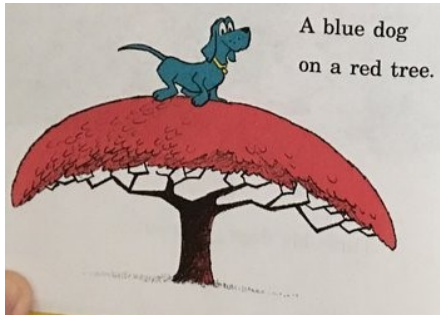

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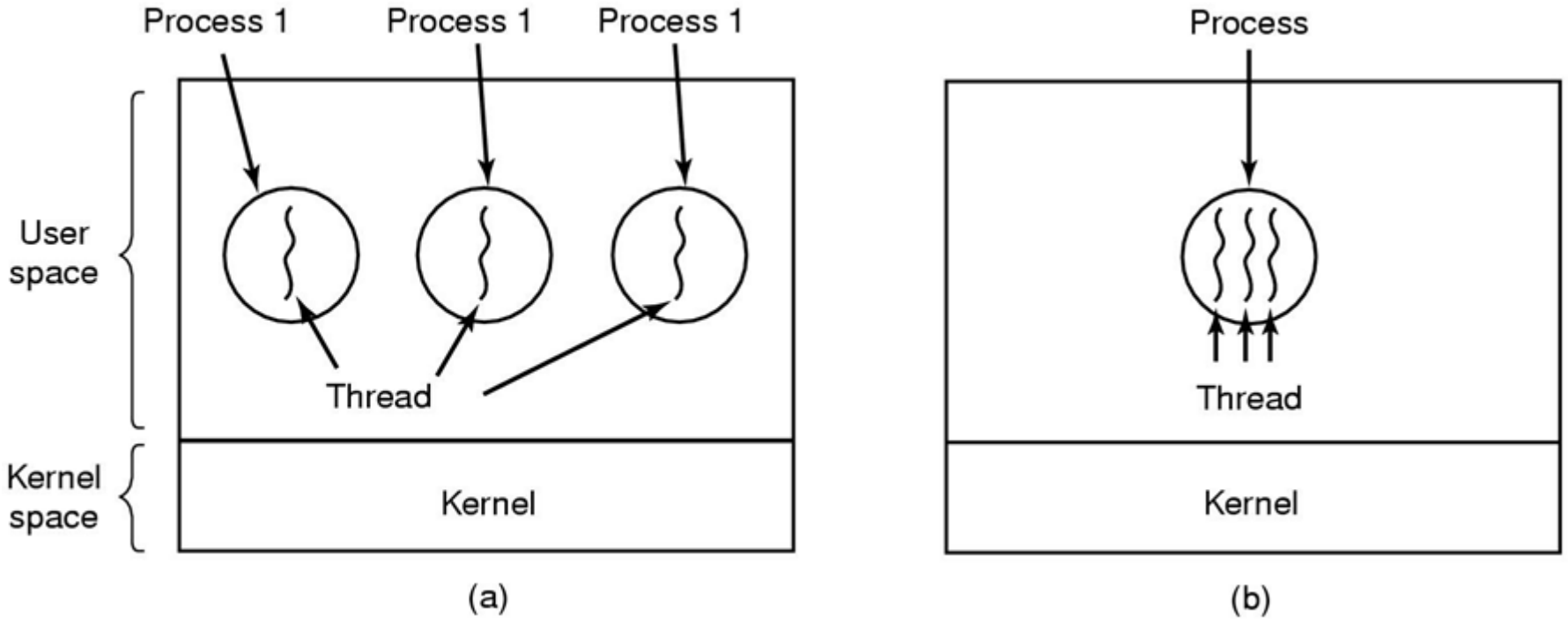

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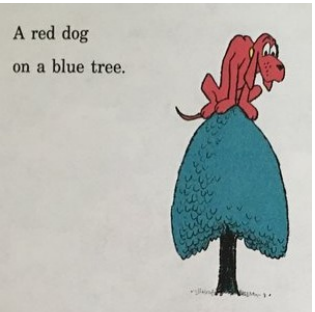

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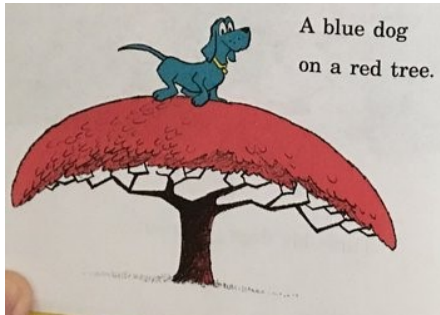

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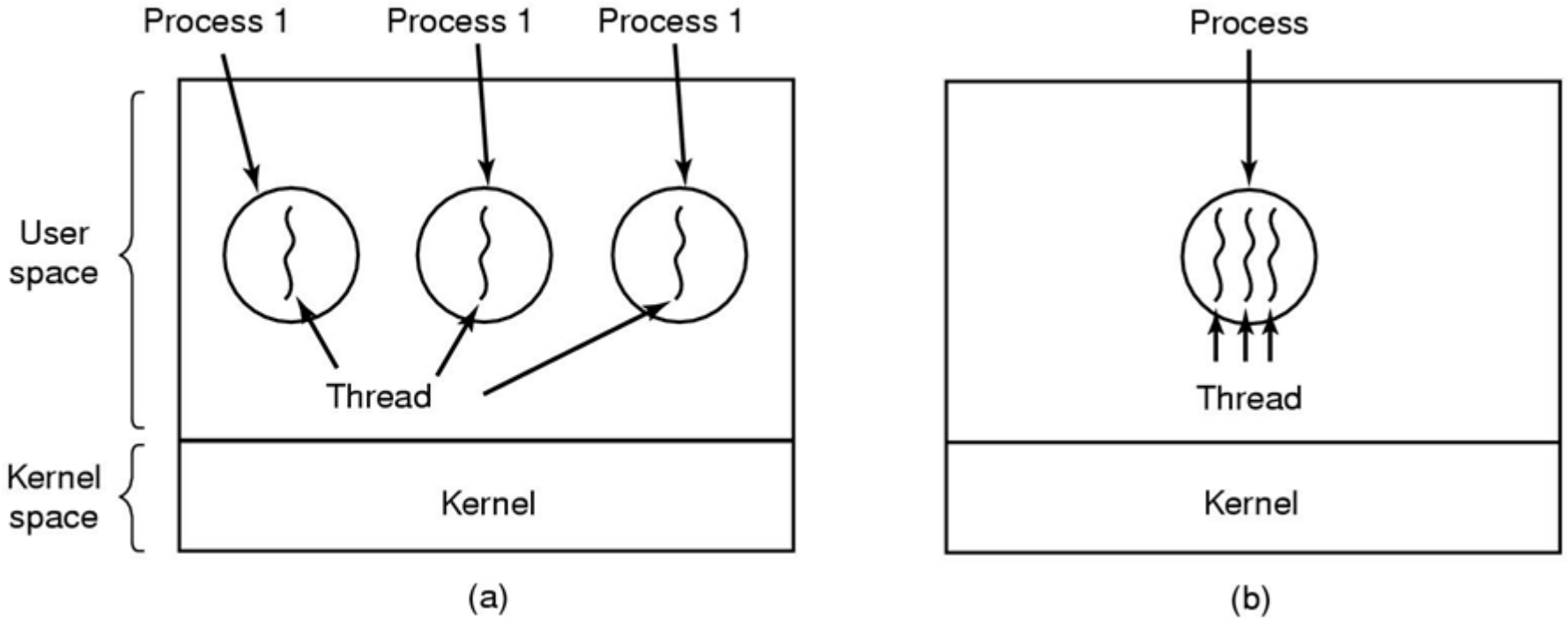

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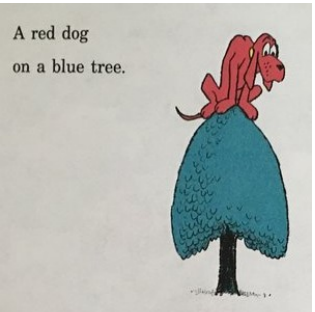

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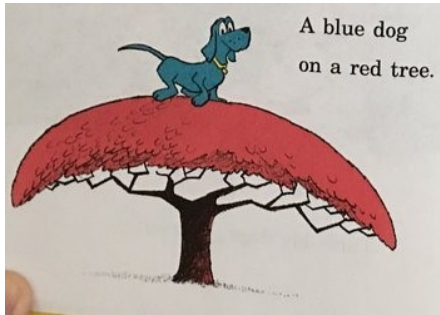
Threads simplify sharing and reduce context overheads



The Thread Model

Per process items	Per thread items
Address space	Program counter
Global variables	Registers
Open files	Stack
Child processes	State
Pending alarms	
Signals and signal handlers	
Accounting information	

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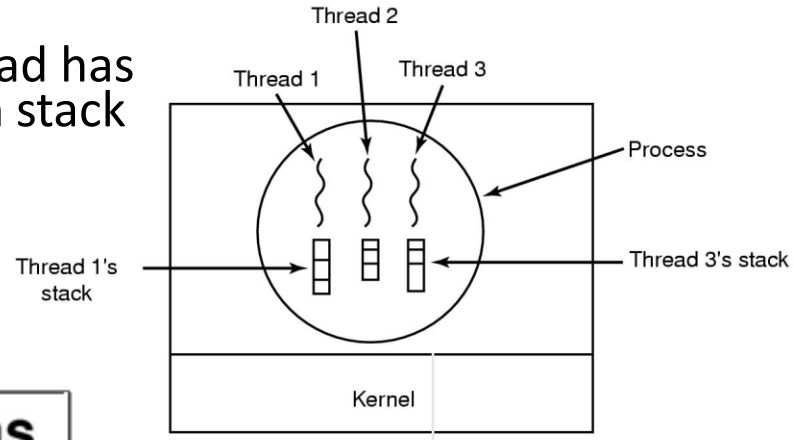

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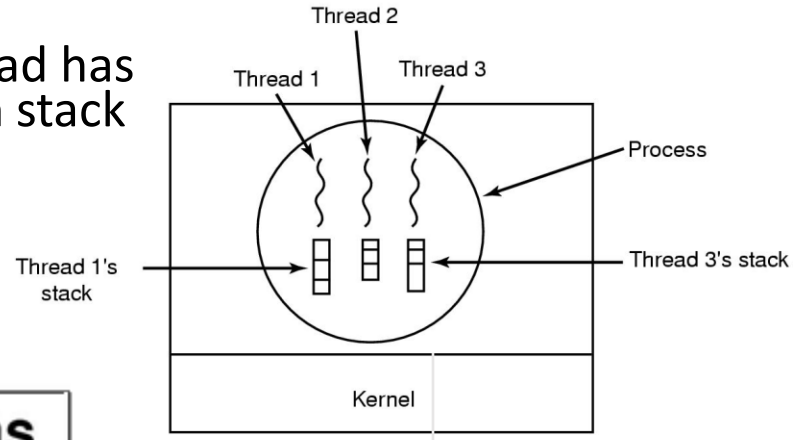

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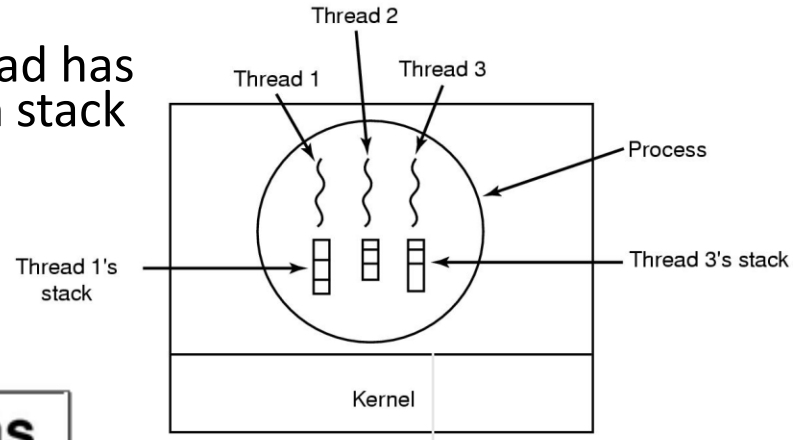

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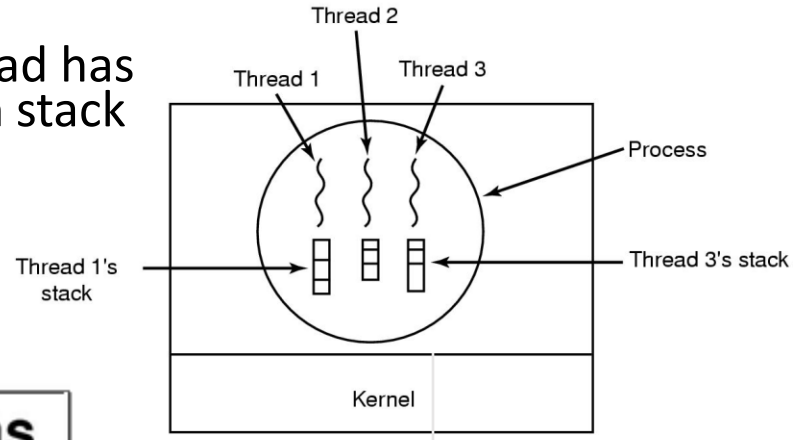

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User Space

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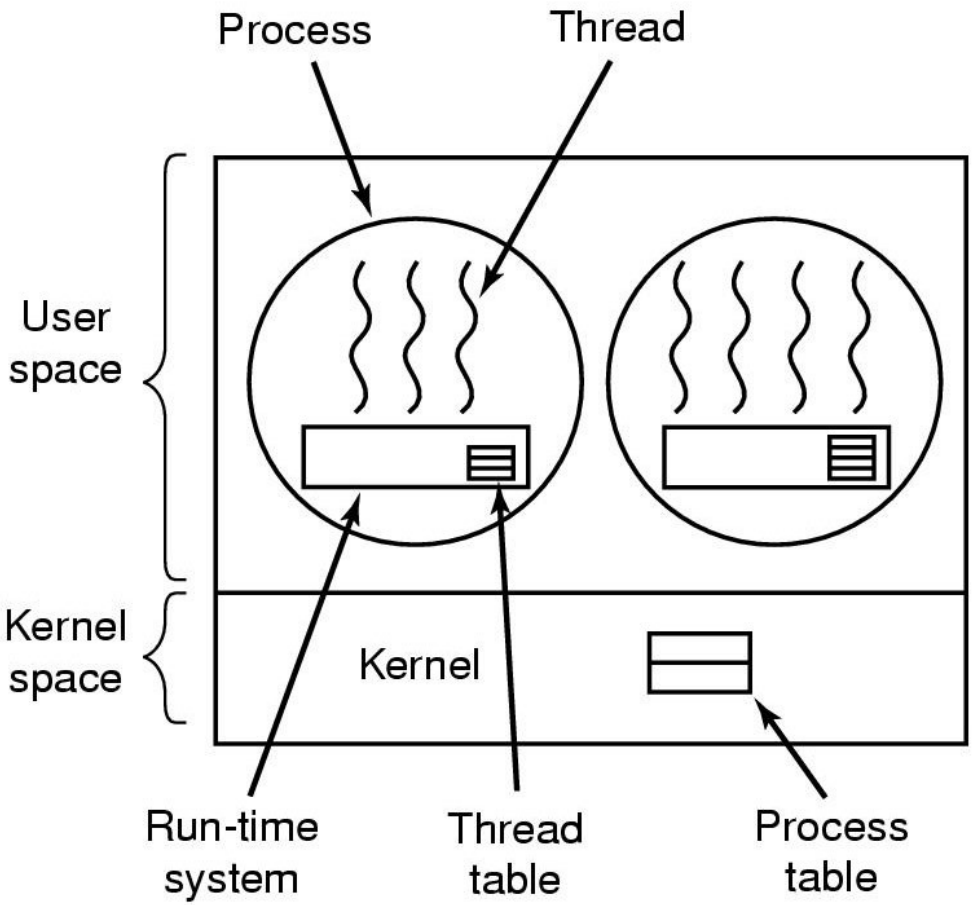

A user-level threads package

Where to Implement Threads:

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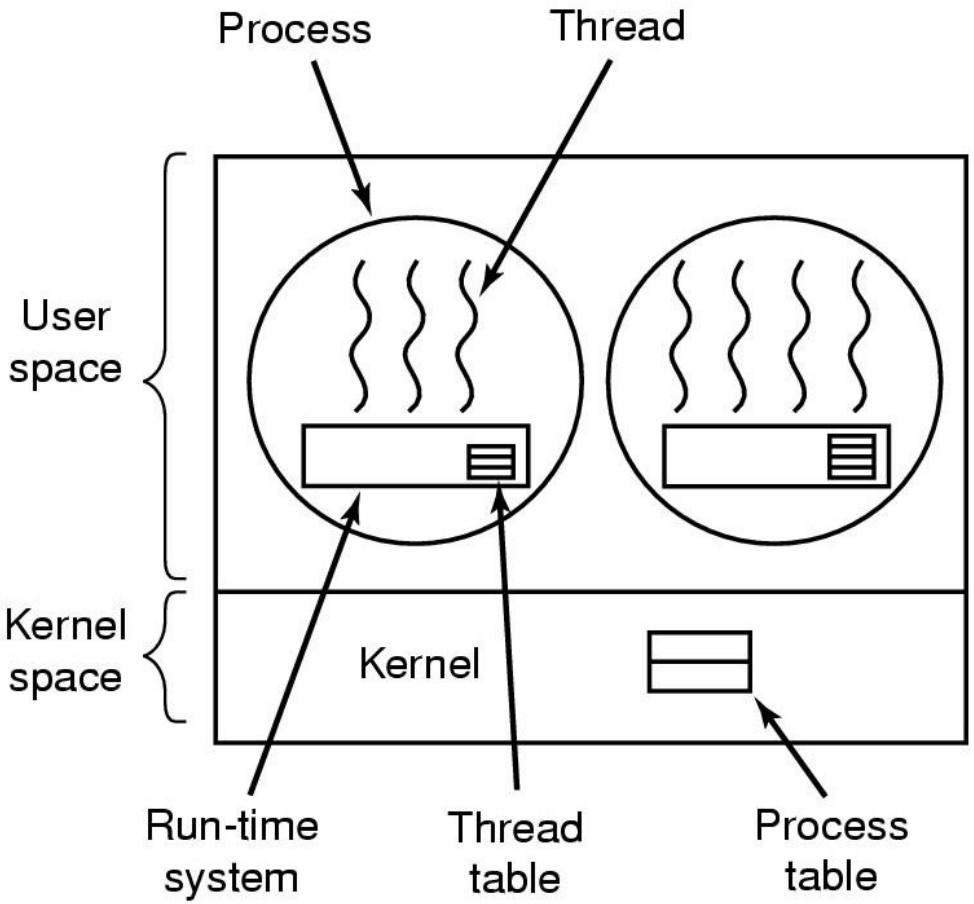

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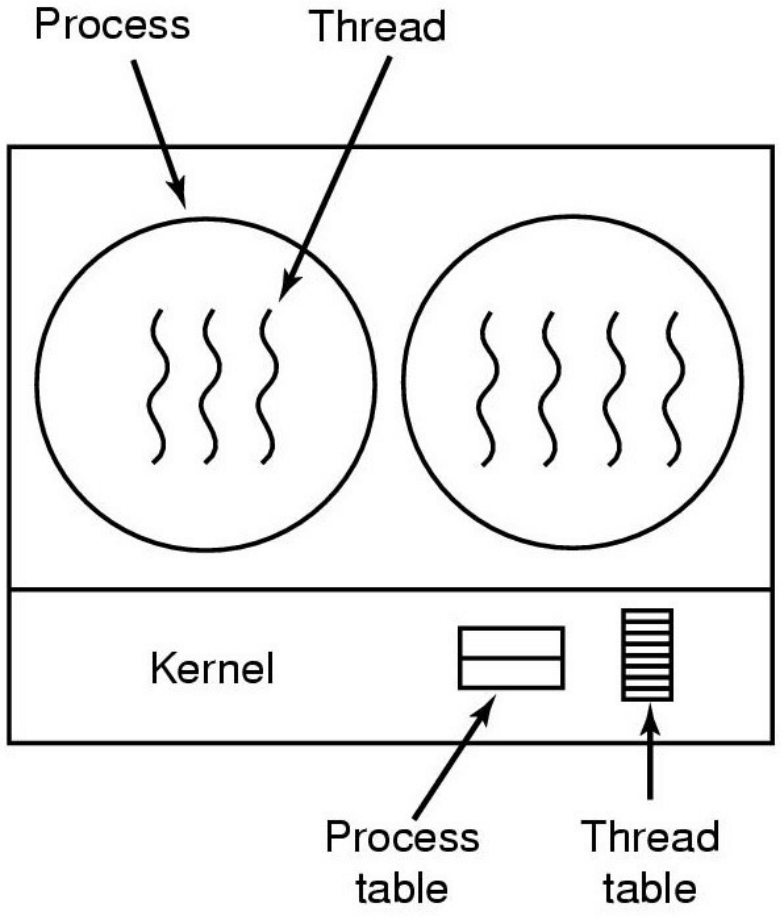
Kernel Space



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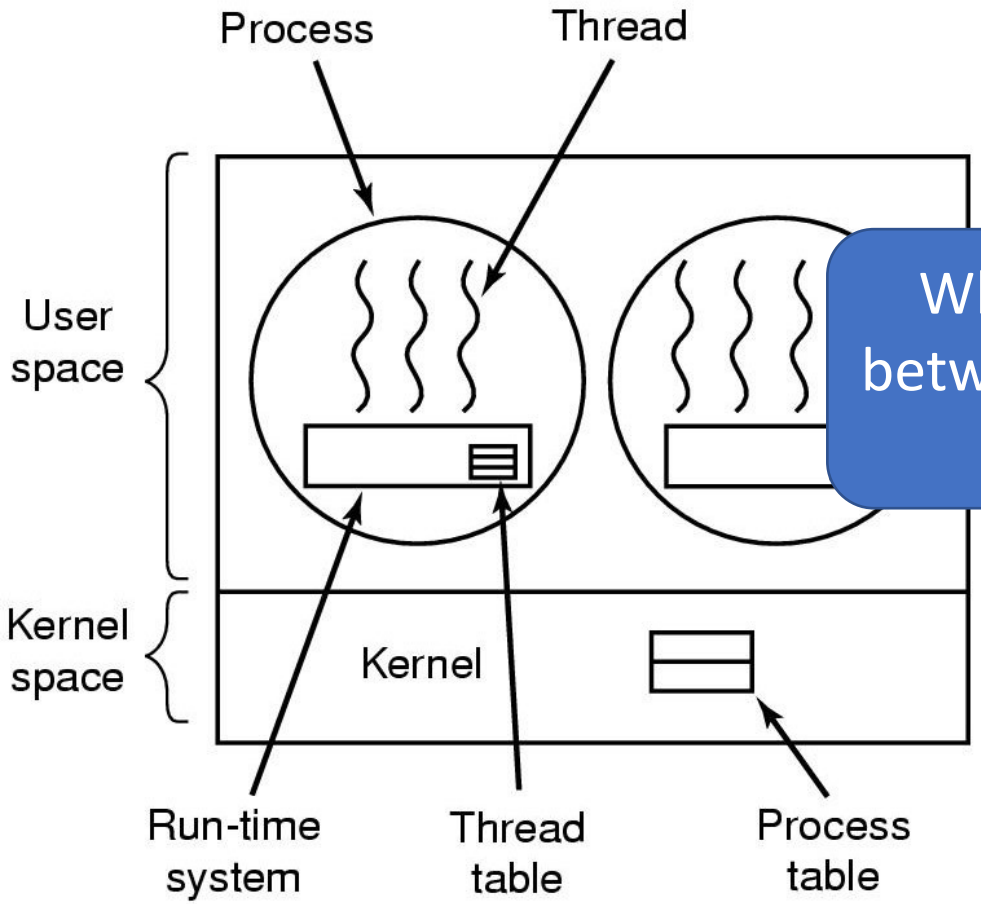

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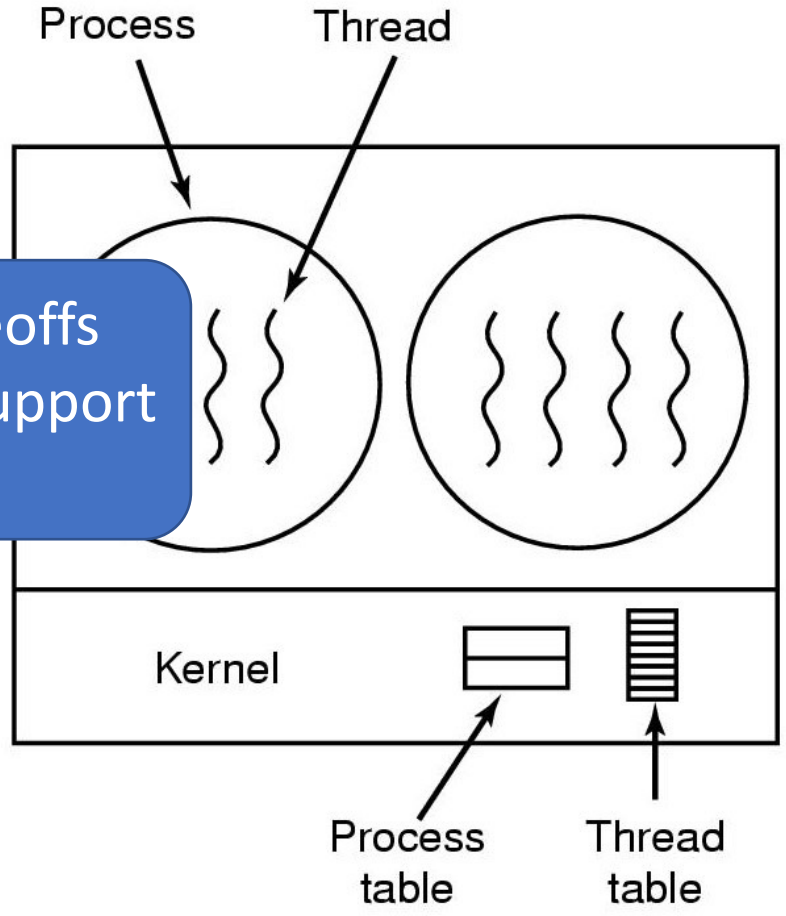

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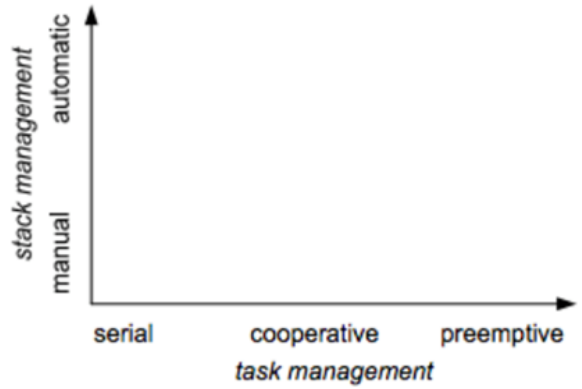
What are some tradeoffs between user/kernel support for threads?

Execution Context Management

“Task” == “Flow of Control”, but with less typing
“Stack” == Task State



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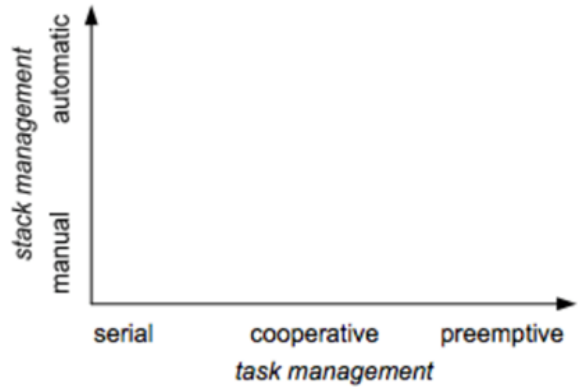
Task Management



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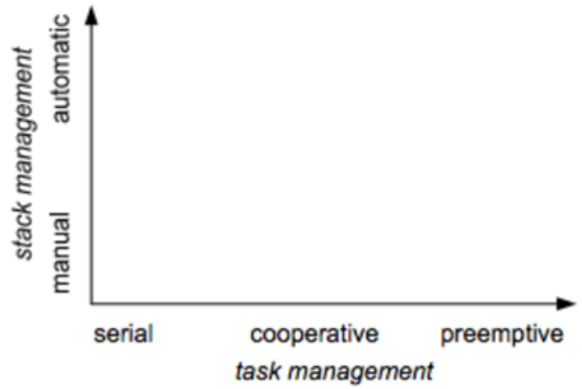

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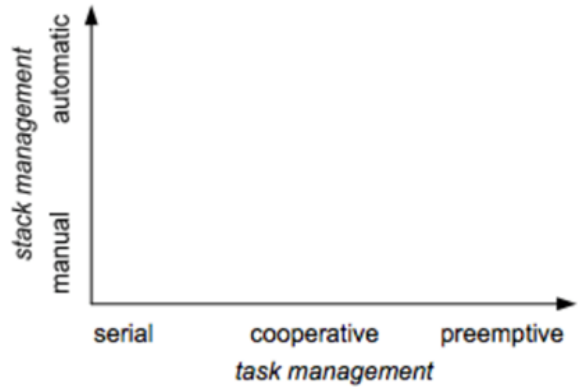

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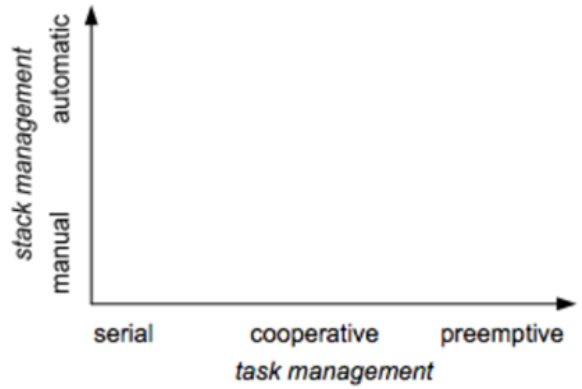

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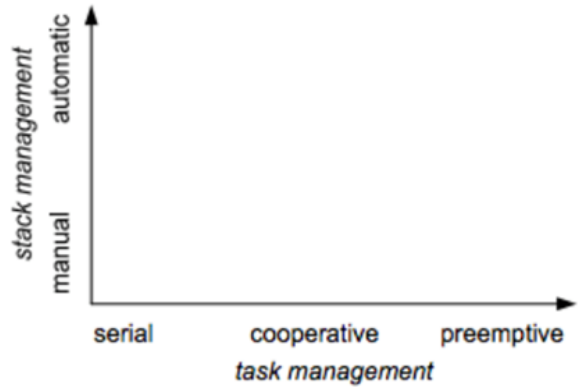

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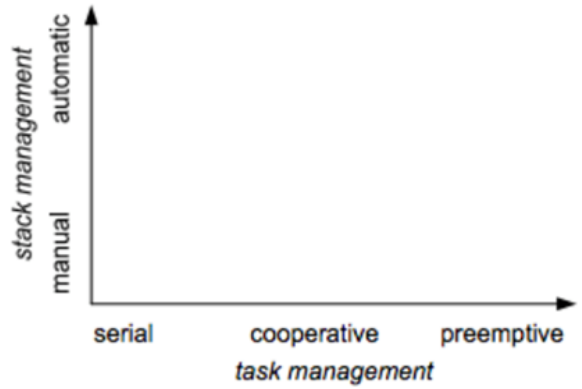

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These dimensions can be orthogonal

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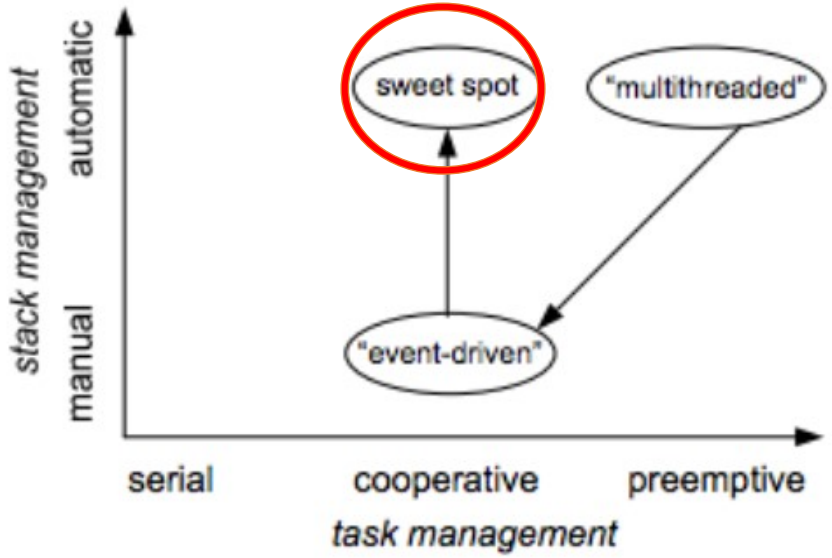

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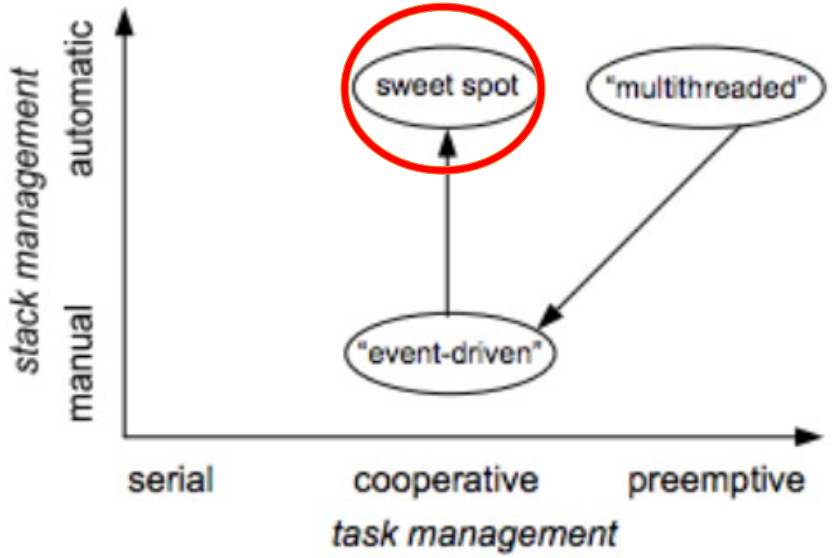
Fibers: cooperative threading with automatic stack management



Threads vs Fibers

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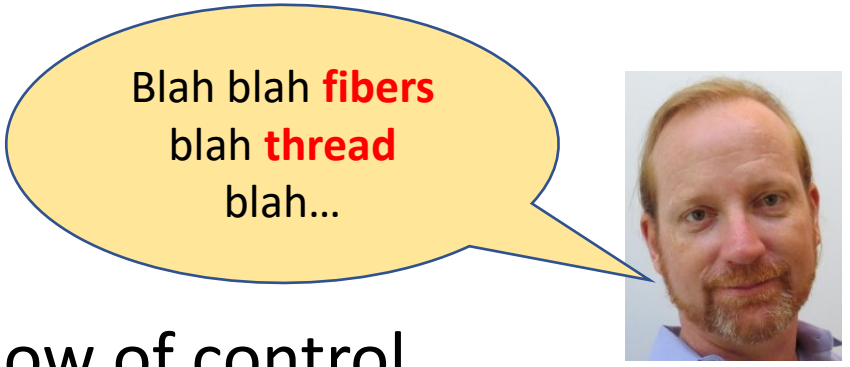

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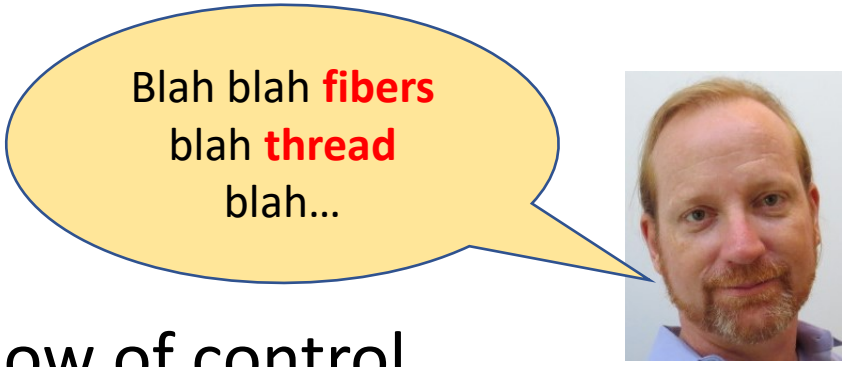

- Like threads, *just an abstraction* for flow of control
- *Lighter weight* than threads
  - In Windows, just a stack, subset of arch. registers, non-preemptive
  - *Not* just threads without exception support
  - stack management/impl has interplay with exceptions
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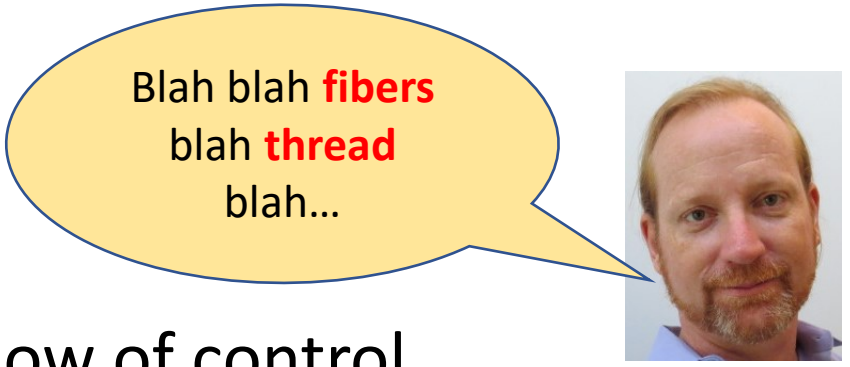

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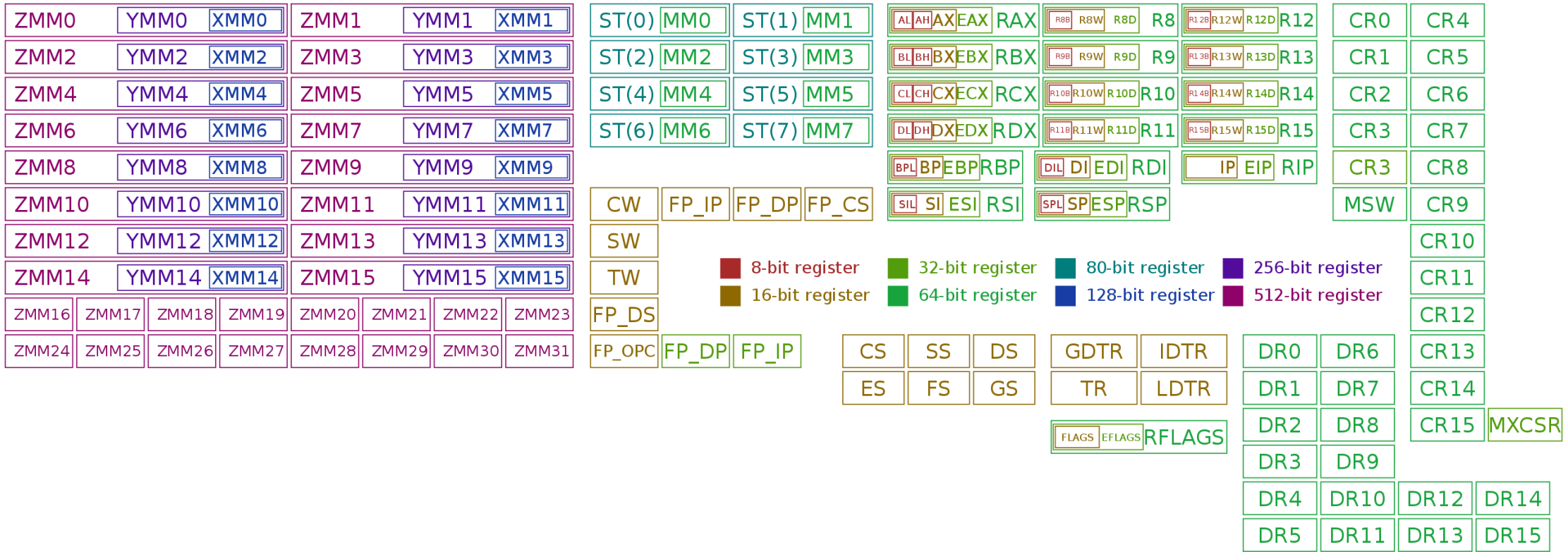
- ***Takeaway***: diversity of abstractions/containers for execution flows

x86_64 Architectural Registers



- *Register map diagram courtesy of: By Immae - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=32745525*

Linux x86_64 context switch ***excerpt***

```
/*
 *      switch_to(x,y) should switch tasks from x to y.
 *
 * This could still be optimized:
 * - fold all the options into a flag word and test it with a single test.
 * - could test fs/gs bitsliced
 *
 * Kprobes not supported here. Set the probe on schedule instead.
 * Function graph tracer not supported too.
 */
__visible __notrace_funcgraph struct task_struct *
__switch_to(struct task_struct *prev_p, struct task_struct *next_p)
{
        struct thread_struct *prev = &prev_p->thread;
        struct thread_struct *next = &next_p->thread;
        struct fpu *prev_fpu = &prev->fpu;
        struct fpu *next_fpu = &next->fpu;
        int cpu = smp_processor_id();
        struct tss_struct *tss = &per_cpu(cpu_tss_rw, cpu);

        WARN_ON_ONCE(IS_ENABLED(CONFIG_DEBUG_ENTRY) &&
                     this_cpu_read(irq_count) != -1);

        switch_fpu_prepare(prev_fpu, cpu);

        /* We must save %fs and %gs before load_TLS() because
         * %fs and %gs may be cleared by load_TLS().
         *
         * (e.g. xen_load_tls())
         */
        save_fsgs(prev_p);

        /*
         * Load TLS before restoring any segments so that segment loads
         * reference the correct GDT entries.
         */
        load_TLS(next, cpu);

        /*
         * Leave lazy mode, flushing any hypercalls made here.  This
         * must be done after loading TLS entries in the GDT but before
         * loading segments that might reference them, and and it must
         * be done before fpu__restore(), so the TS bit is up to
         * date.
         */
        arch_end_context_switch(next_p);

        /* Switch DS and ES.
         *
         * Reading them only returns the selectors, but writing them (if
         * nonzero) loads the full descriptor from the GDT or LDT.  The
         * LDT for next is loaded in switch_mm, and the GDT is loaded
         * above.
         *
         * We therefore need to write new values to the segment
         * registers on every context switch unless both the new and old
         * values are zero.
         *
         * Note that we don't need to do anything for CS and SS, as
         * those are saved and restored as part of pt_regs.
         */
        savesegment(es, prev->es);
        if (unlikely(next->es | prev->es))
                loadsegment(es, next->es);

        savesegment(ds, prev->ds);
        if (unlikely(next->ds | prev->ds))
                loadsegment(ds, next->ds);

        load_seg_legacy(prev->fsindex, prev->fsbase,
                        next->fsindex, next->fsbase, FS);
        load_seg_legacy(prev->gsindex, prev->gsbase,
                        next->gsindex, next->gsbase, GS);
```

Complete fiber context switch on Unix and Windows

```
* The AMD64 architecture provides 16 general 64-bit registers together with 16
* 128-bit SSE registers, overlapping with 8 legacy 80-bit x87 floating point
* registers.
*
*             Both              Unix only          Windows only
*             ----              ---------          ------------
*  rax        Result register
*  rbx        Must be preserved
*  rcx                          Fourth argument    First argument
*  rdx                          Third argument     Second argument
*  rsp        Stack pointer, must be preserved
*  rbp        Frame pointer, must be preserved
*  rsi                          Second argument    Must be preserved
*  rdi                          First argument     Must be preserved
*  r8                           Fifth argument     Third argument
*  r9                           Sixth argument     Fourth argument
*  r10-r11    Volatile
*  r12-r15    Must be preserved
*  xmm0-5     Volatile
*  xmm6-15                      Volatile           Must be preserved
*  fpcsr      Non volatile
*  mxcsr      Non volatile
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* Thus for the two architectures we get slightly different lists of registers
* to preserve.
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* Registers "owned" by caller:
*  Unix:      rbx, rsp, rbp, r12-r15, mxcsr (control bits), x87 CW
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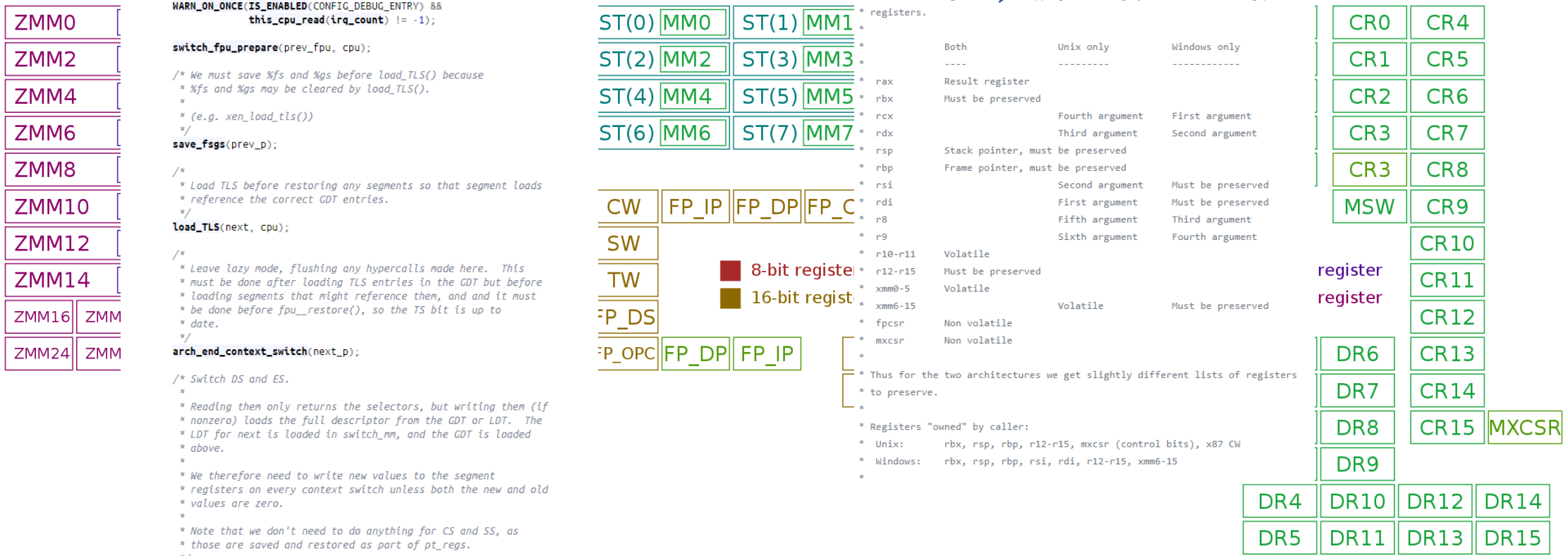

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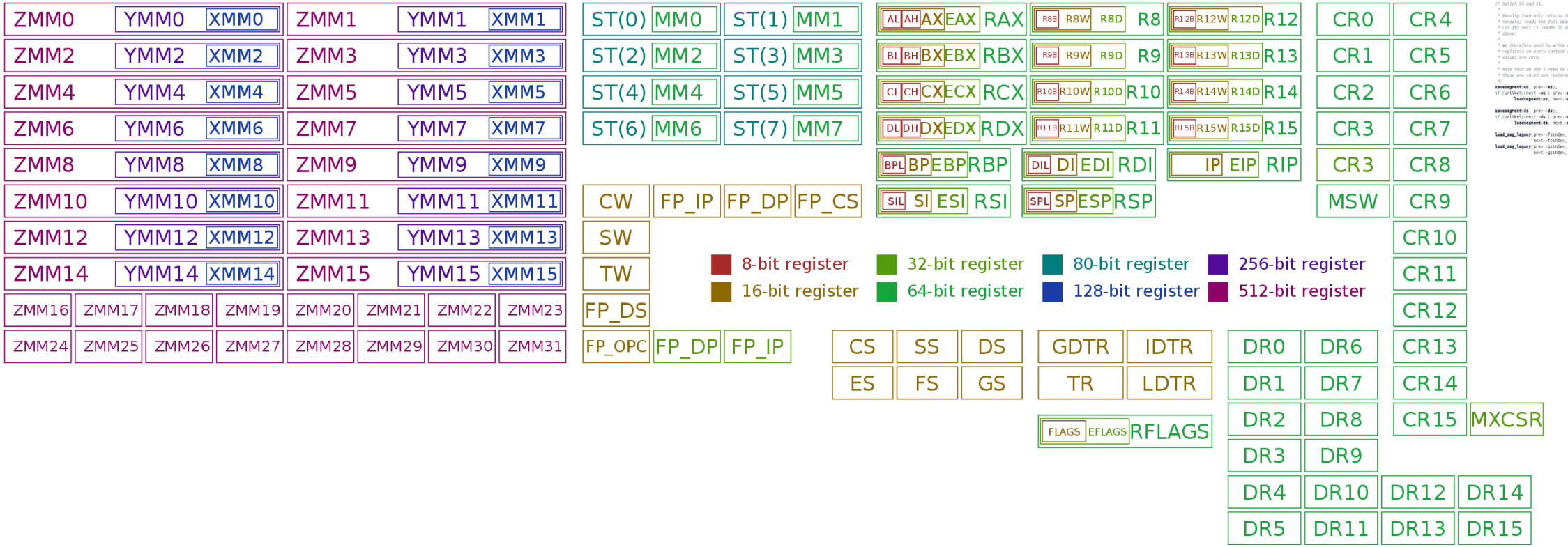
x86_64 Registers and Threads



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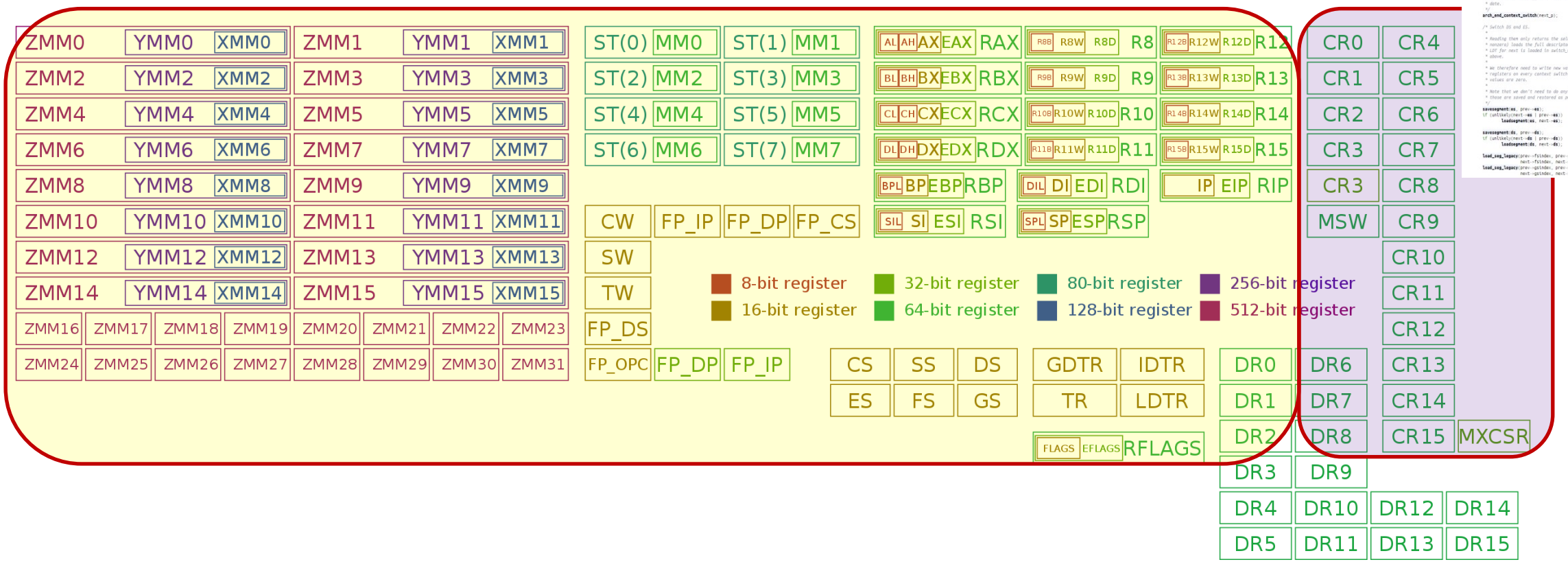

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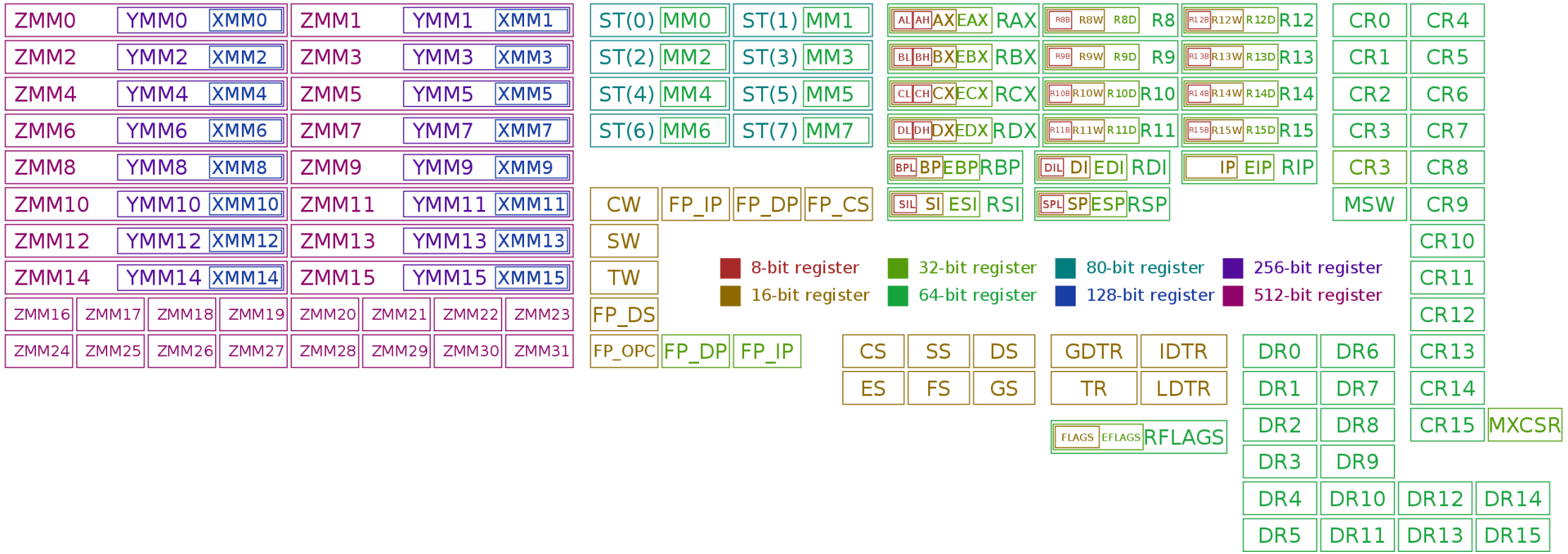

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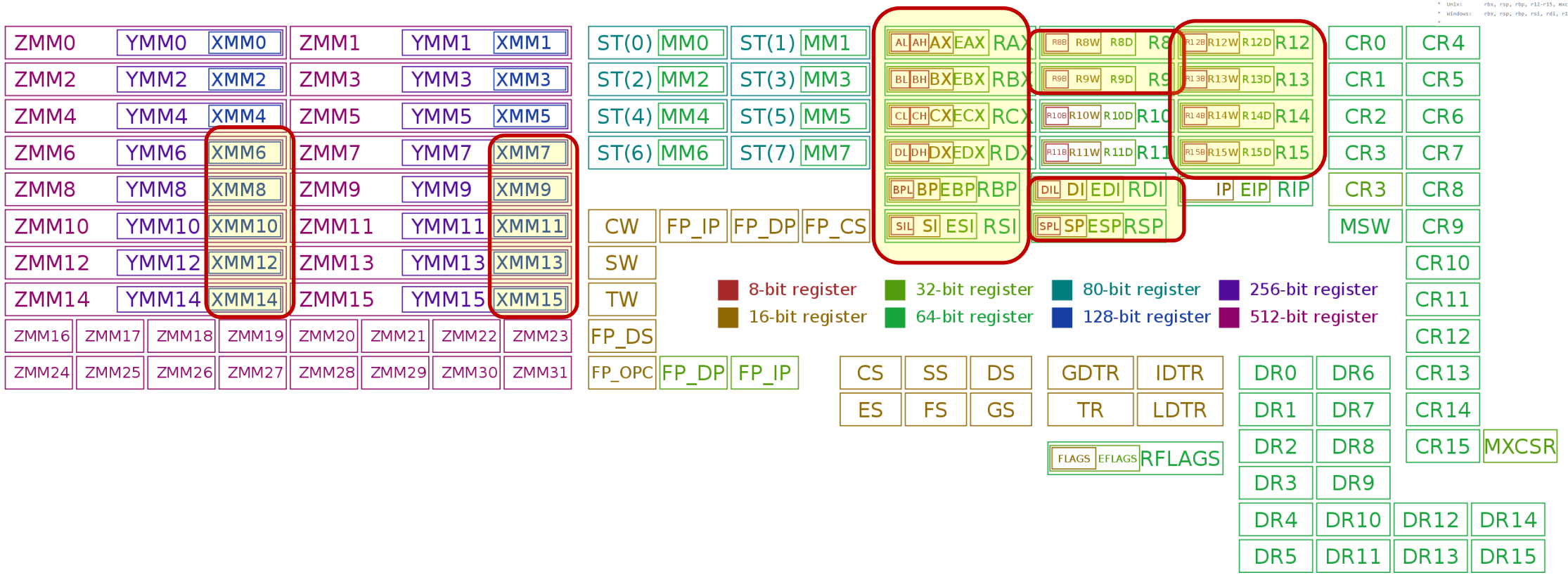


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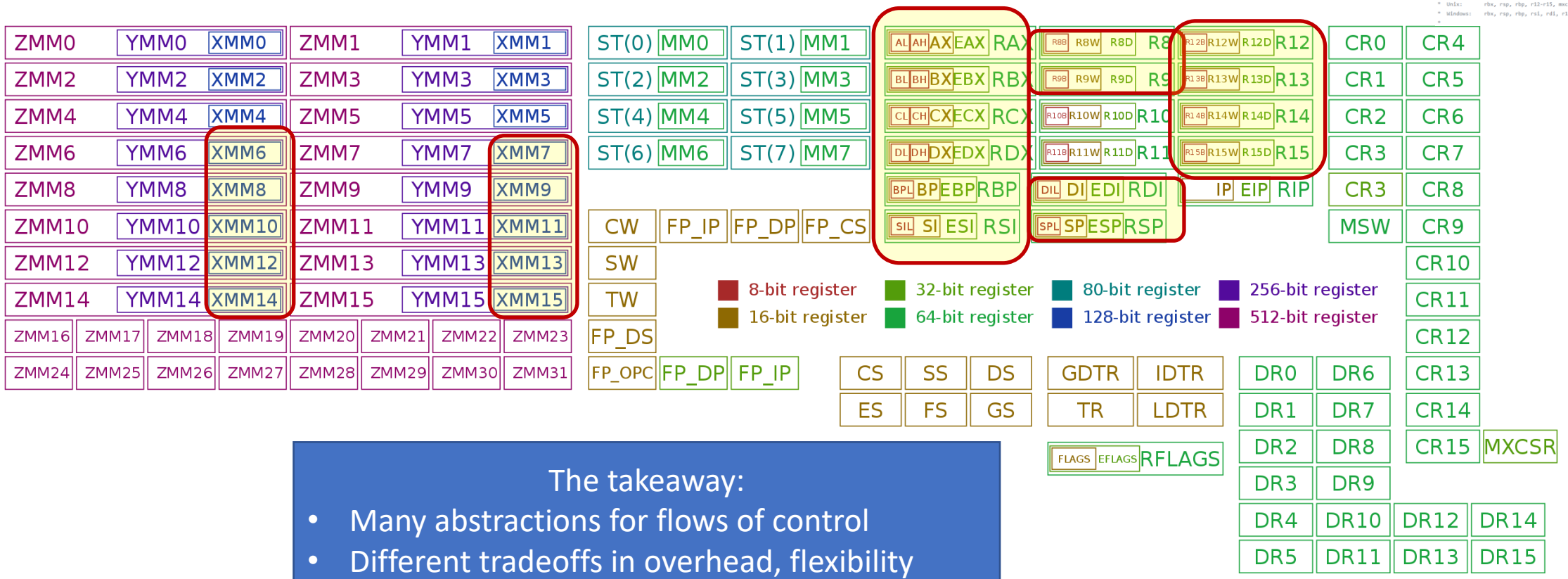

The takeaway:

- Many abstractions for flows of control
- Different tradeoffs in overhead, flexibility
- Matters for concurrency: exercised heavily

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Pthreads

- POSIX standard thread model,
- Specifies the API and call semantics.
- Popular – most thread libraries are Pthreads-compatible

Can you find the bug here?

What is printed for myNum?

```
void *threadFunc(void *pArg) {
  int* p = (int*)pArg;
  int myNum = *p;
  printf( "Thread number %d\n", myNum);
}
. . .
// from main():
for (int i = 0; i < numThreads; i++) {
   pthread_create(&tid[i], NULL, threadFunc, &i);
}
```

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- Important: Mutex scope must be visible to all threads!

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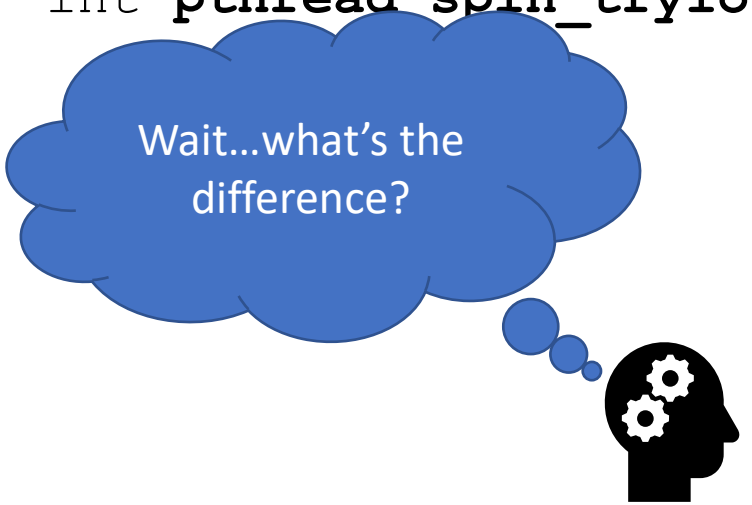


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    Entry section
    Critical section
    Exit section
    Non-critical section
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  - *If a thread i is in entry section, then there is a bound on the number of times that other threads are allowed to enter the critical section before thread i's request is granted*

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while(1) {
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Review: correctness conditions

- Safety
  - Only one thread in the critical region
- Liveness
  - Some thread that enters the entry section eventually enters the critical region
  - Even if other thread takes forever in non-critical region
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Theorem: Every property is a combination of a safety property and a liveness property.
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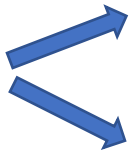
Mutex, spinlock, etc. are ways to implement these



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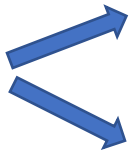

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Did we get all the important conditions?
Why is correctness defined in terms of locks?

Implementing Locks

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int lock_value = 0;
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Completely and utterly broken.
How can we fix it?

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HW Support for Read-Modify-Write (RMW)

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IDEA: hardware implements something like:

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  - Test&Set
  - CAS: Compare & swap
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More on this later…

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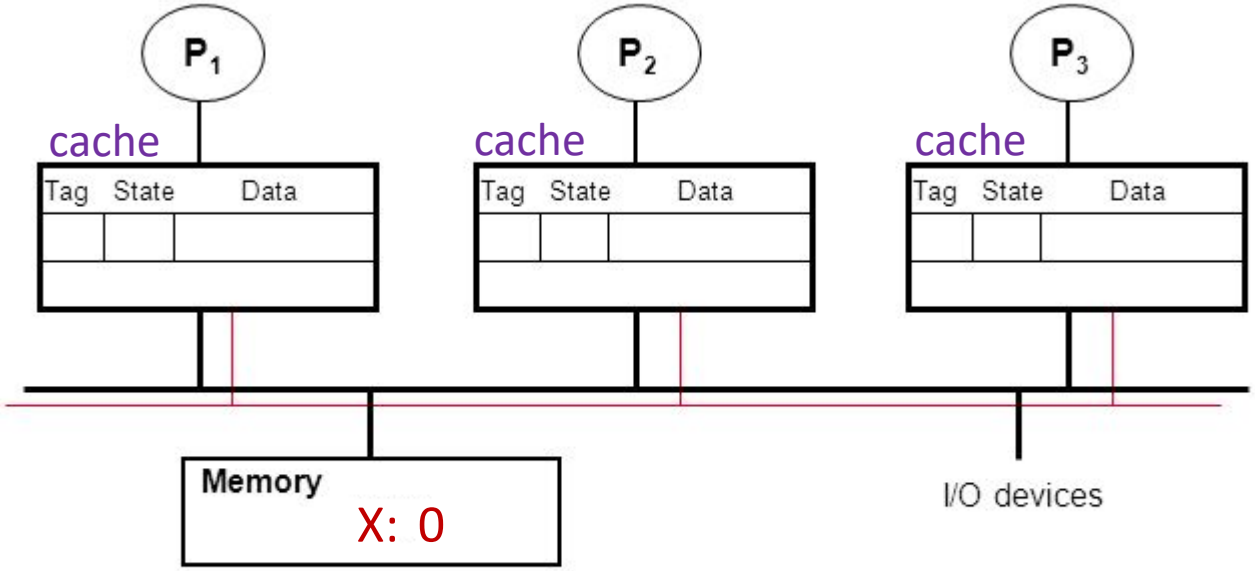
Multiprocessor Cache Coherence

$$F = ma$$

Multiprocessor Cache Coherence

Physics	Concurrency
F = ma	*~ coherence*

Multiprocessor Cache Coherence



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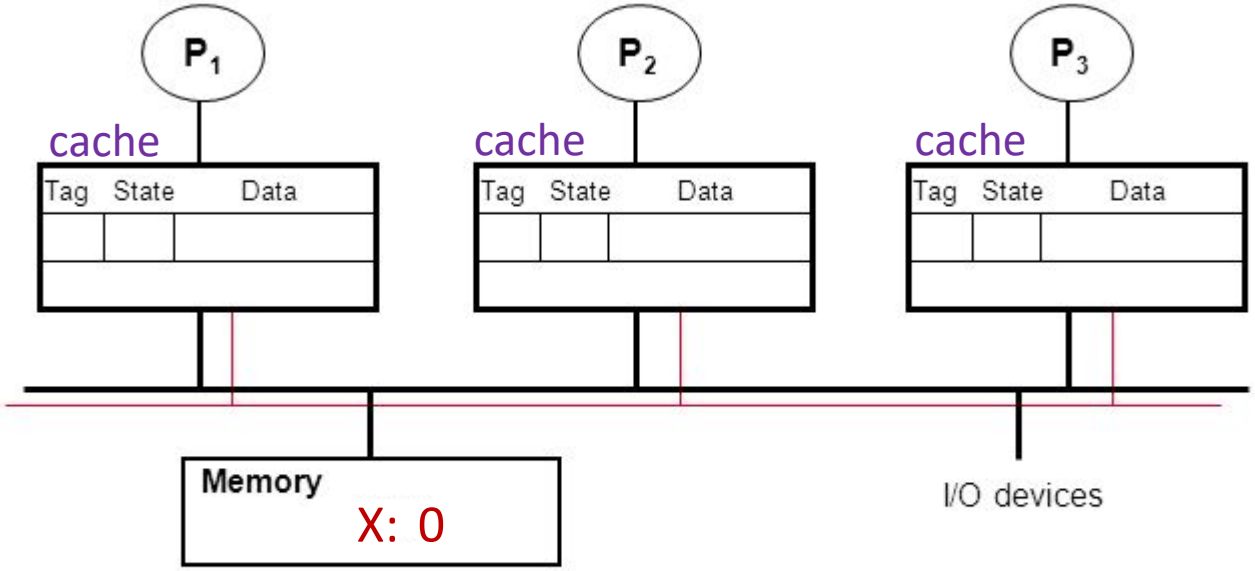

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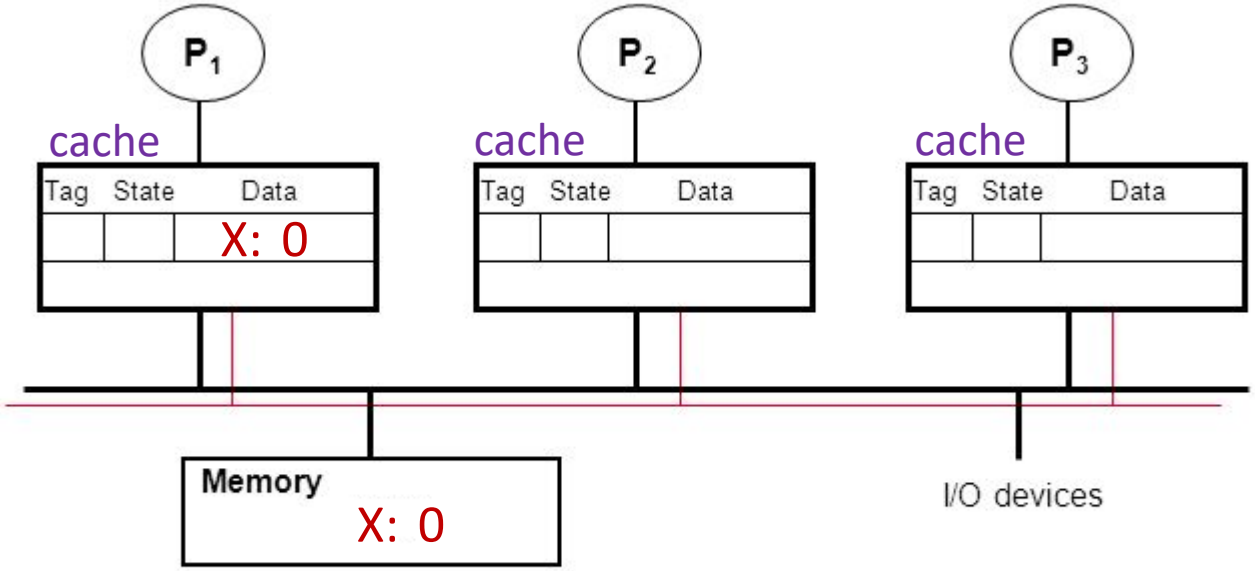

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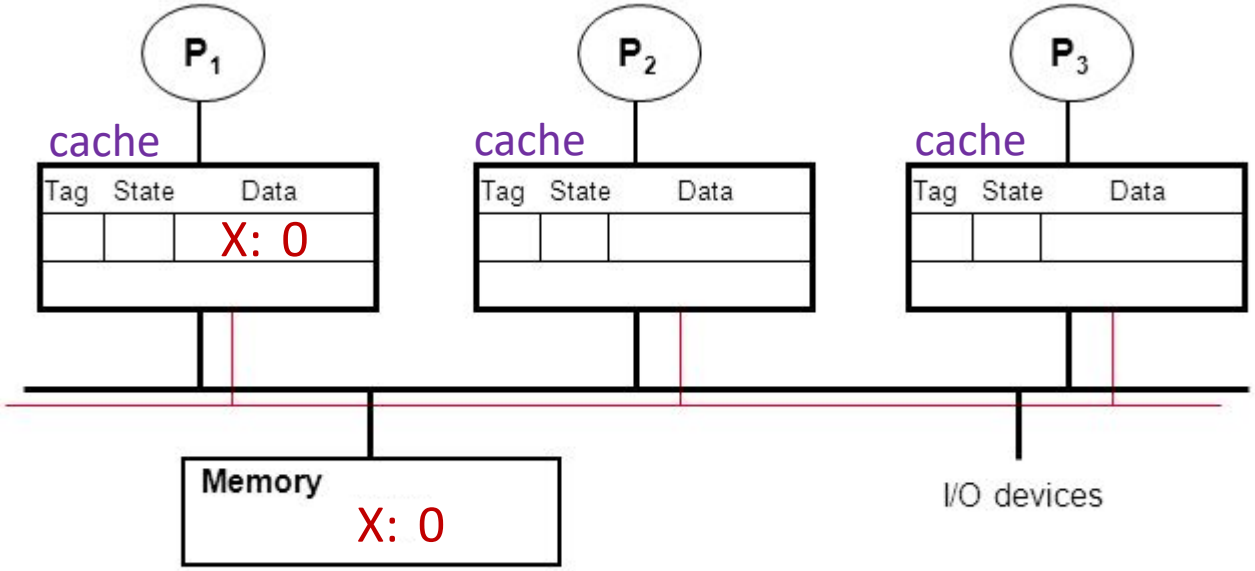

- P1: read X
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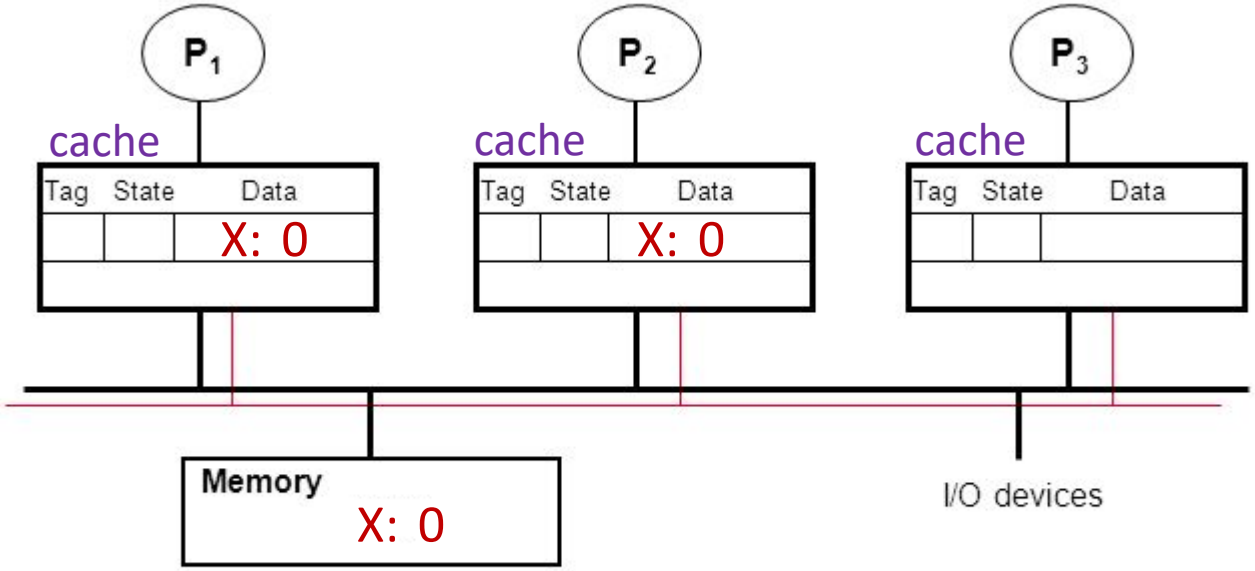

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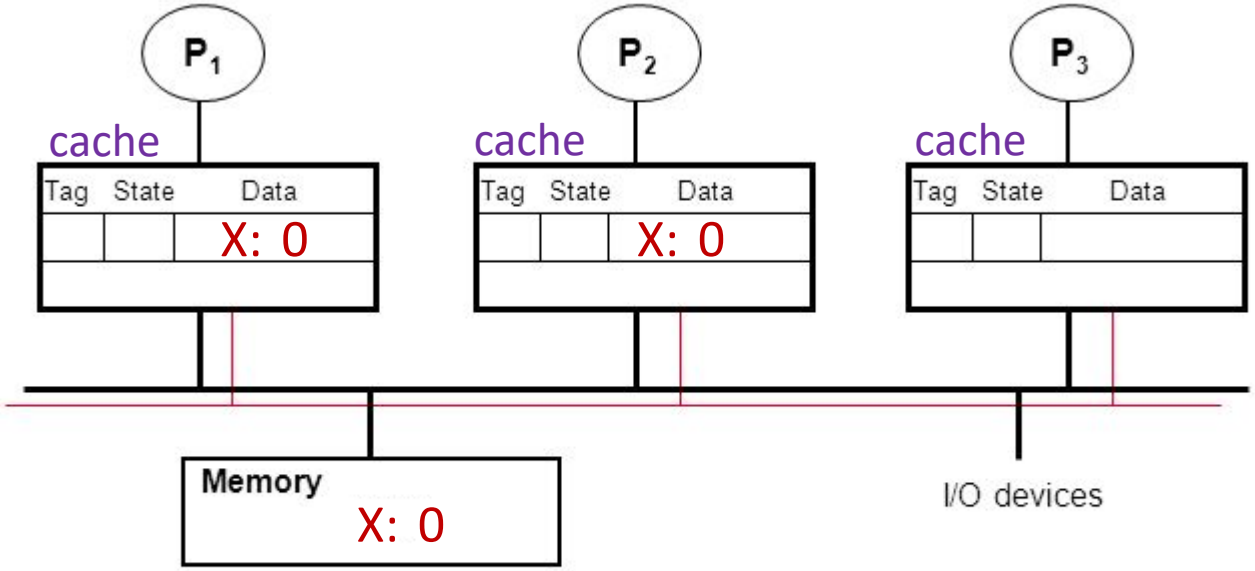

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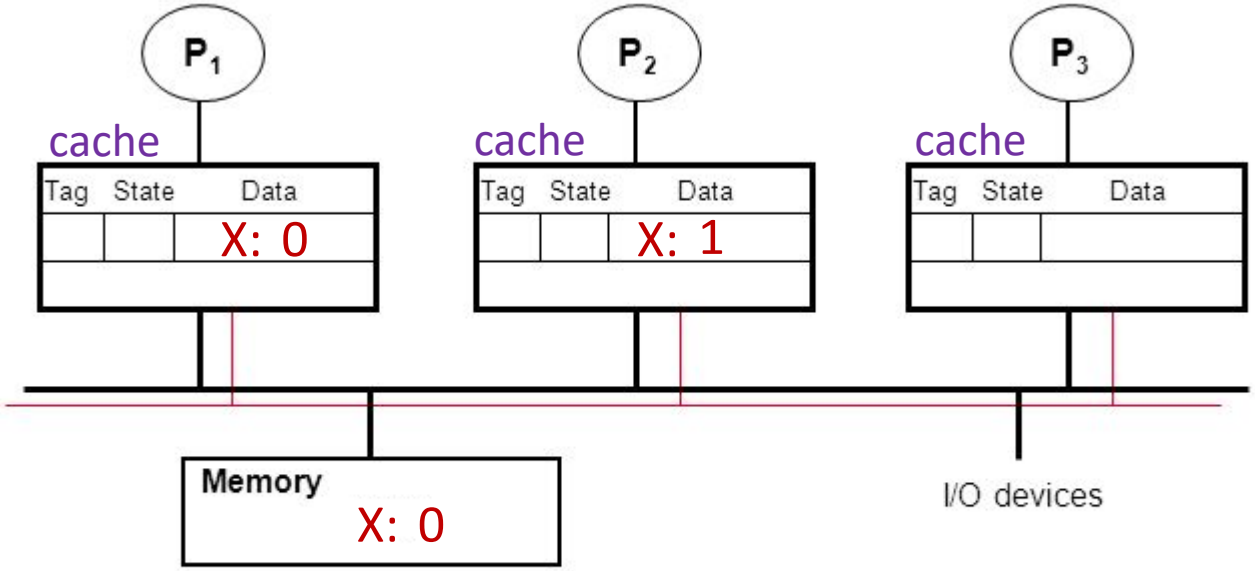

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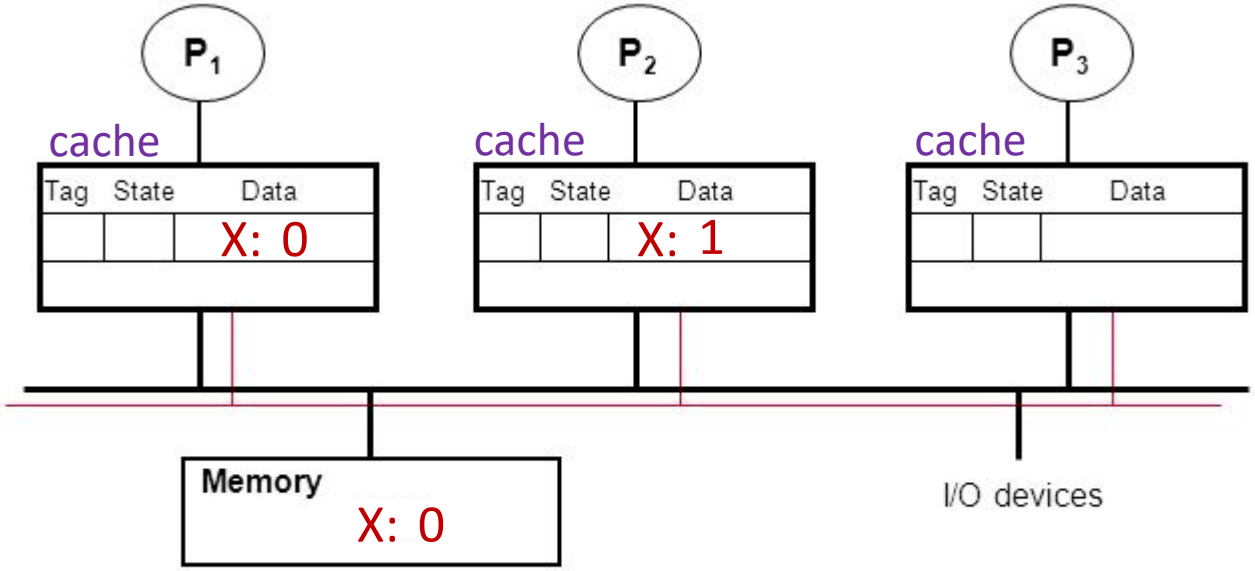

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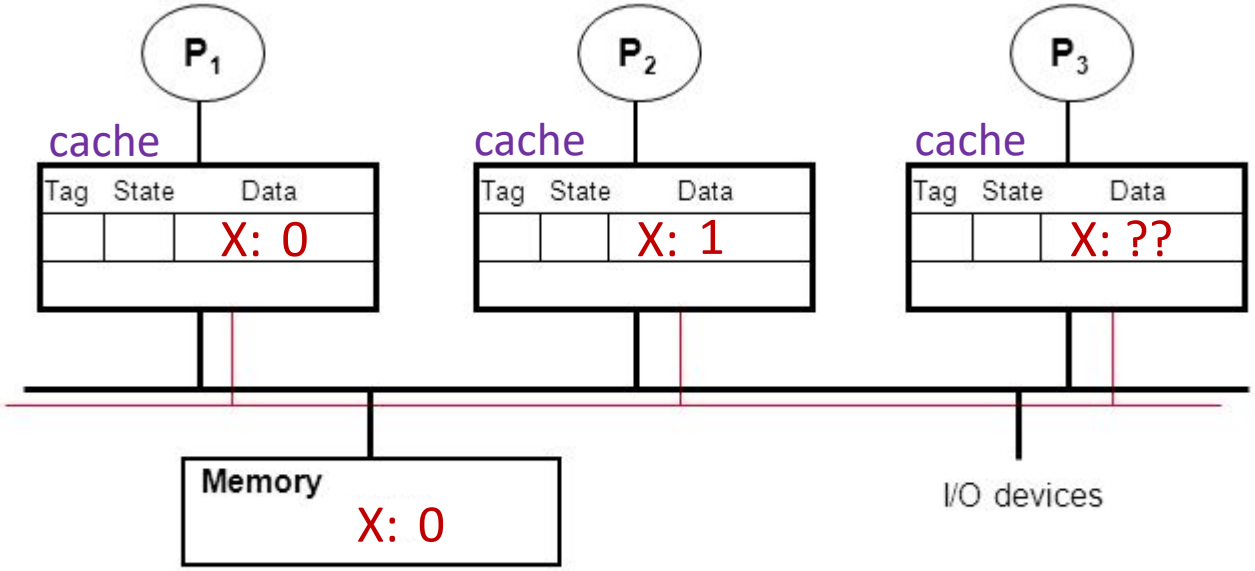

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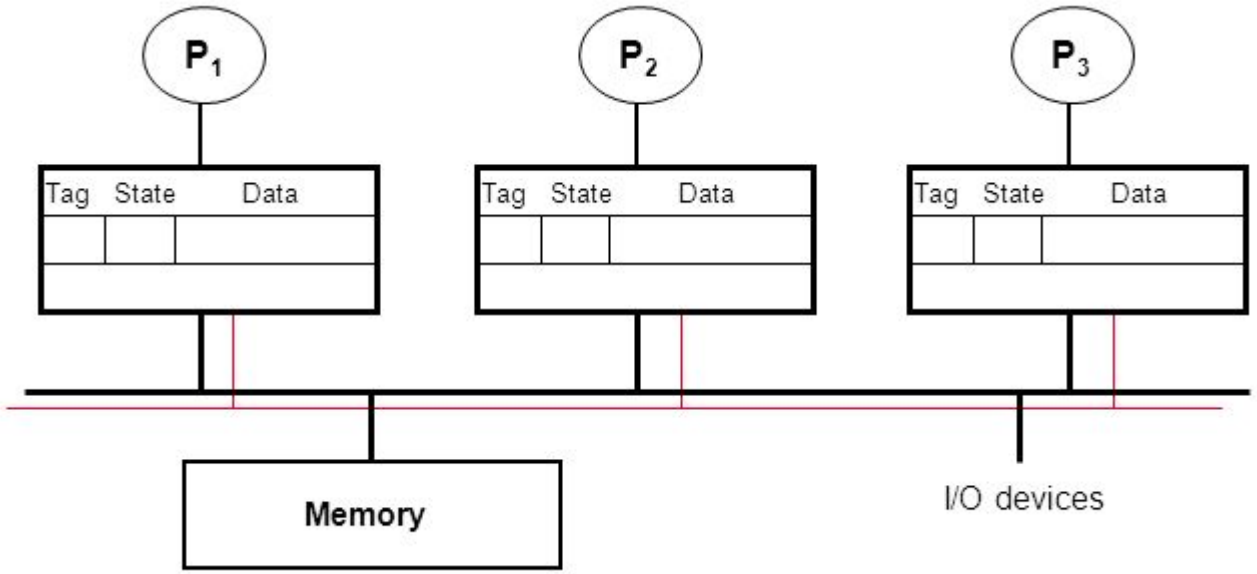

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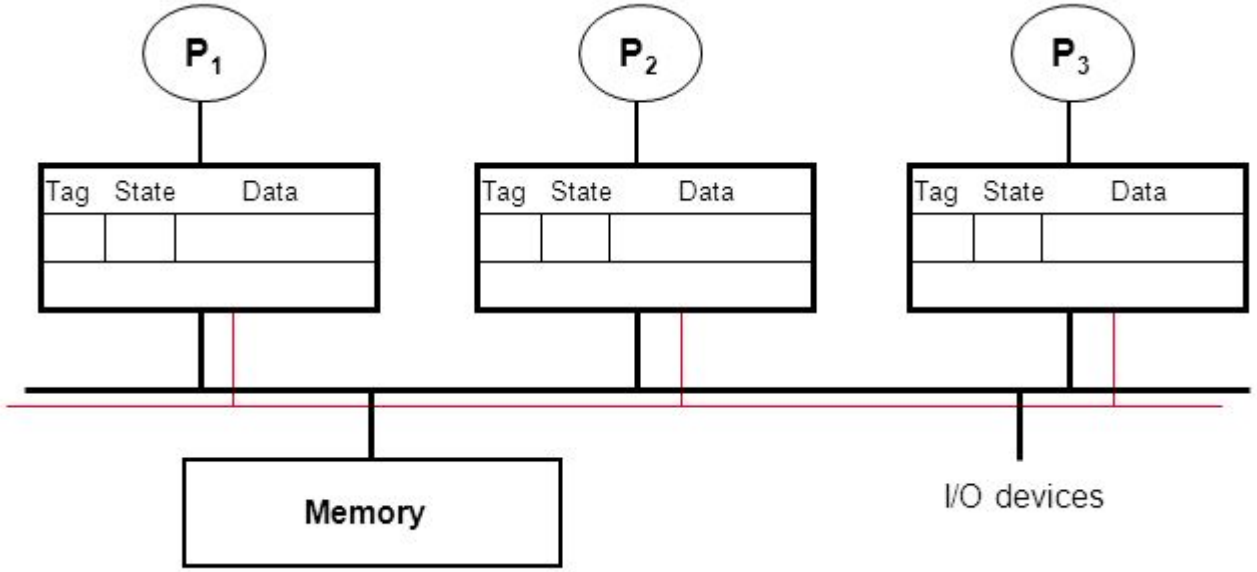

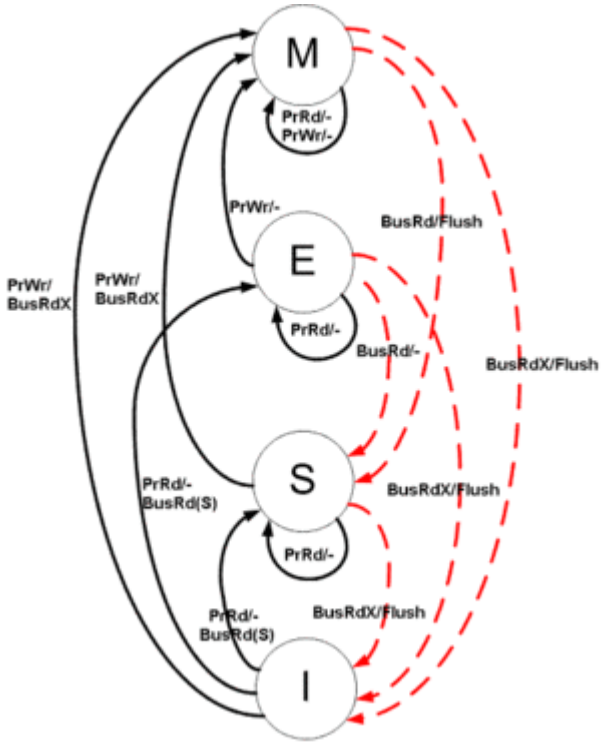

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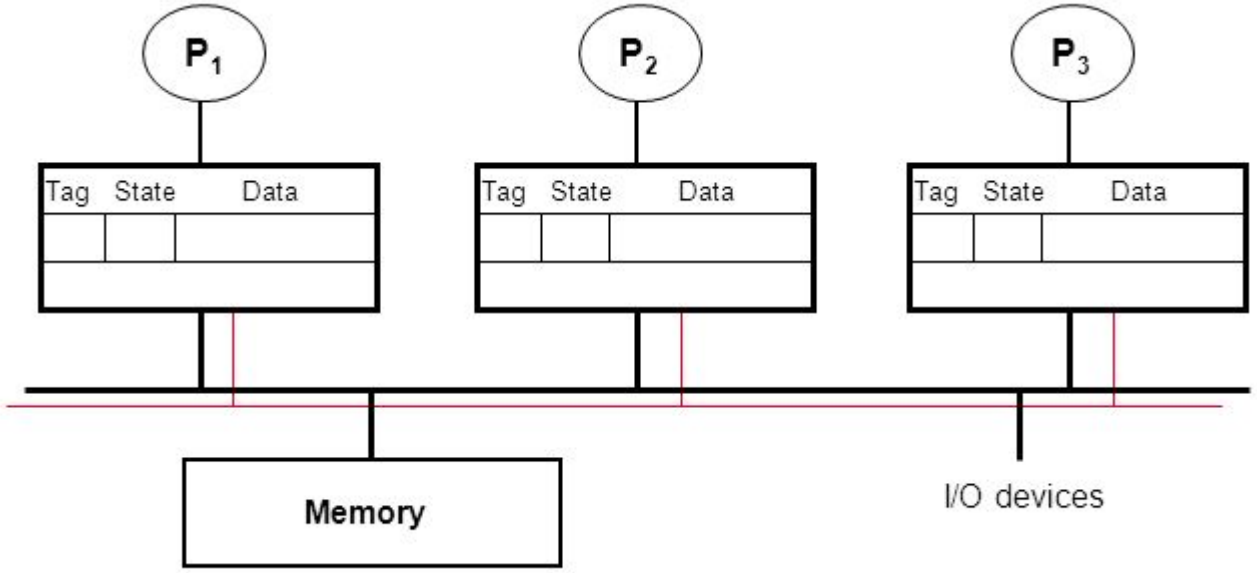

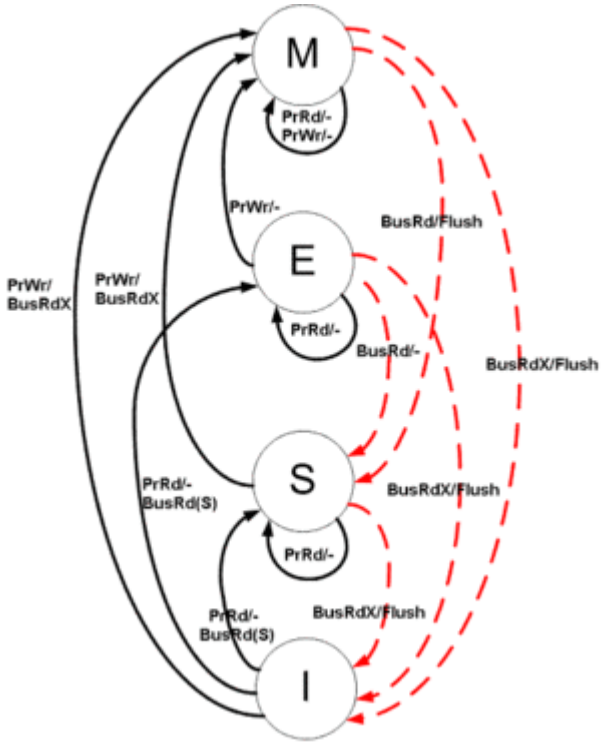

Each cache line has a state (M, E, S, I)

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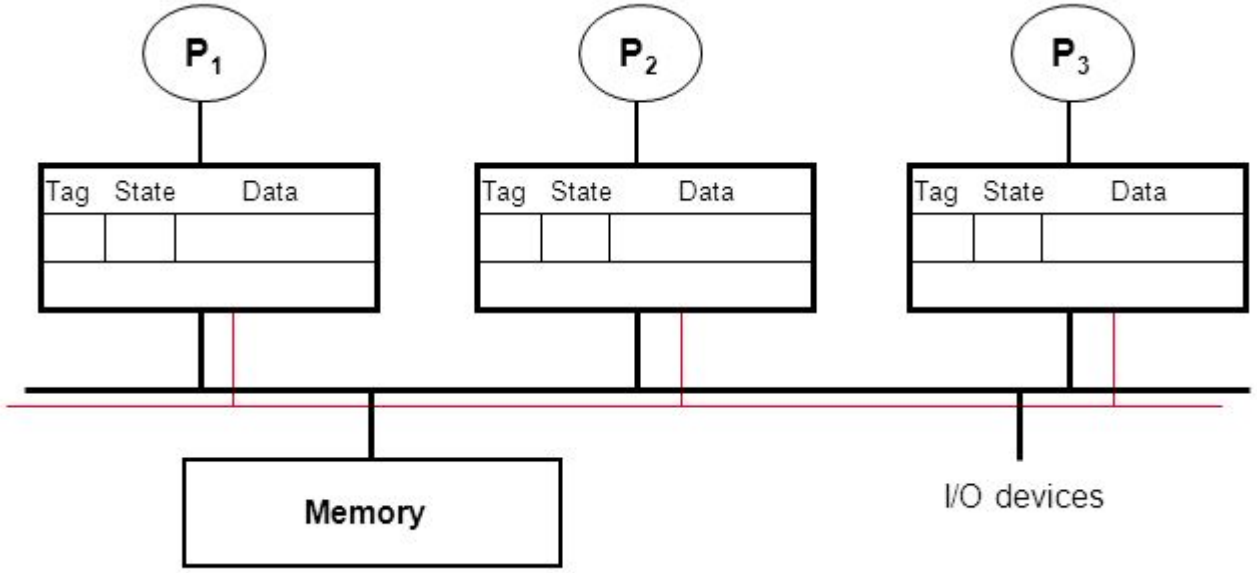

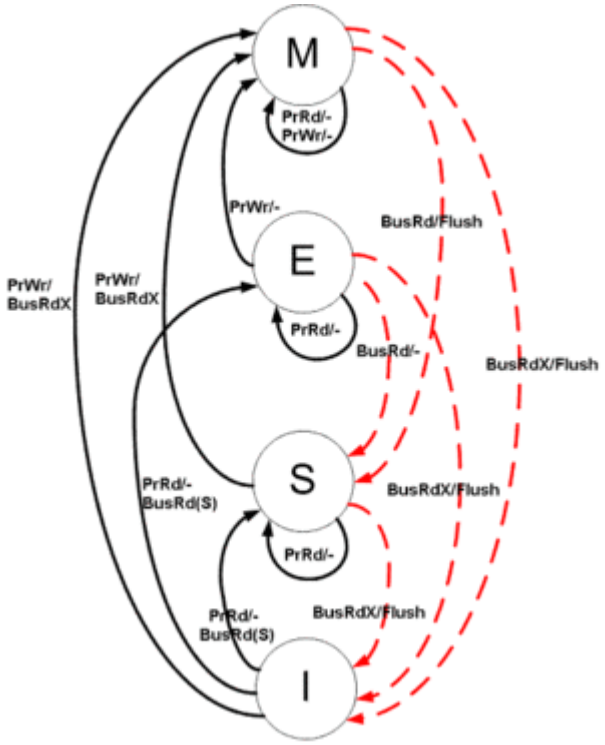

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- Processors “snoop” bus to maintain states

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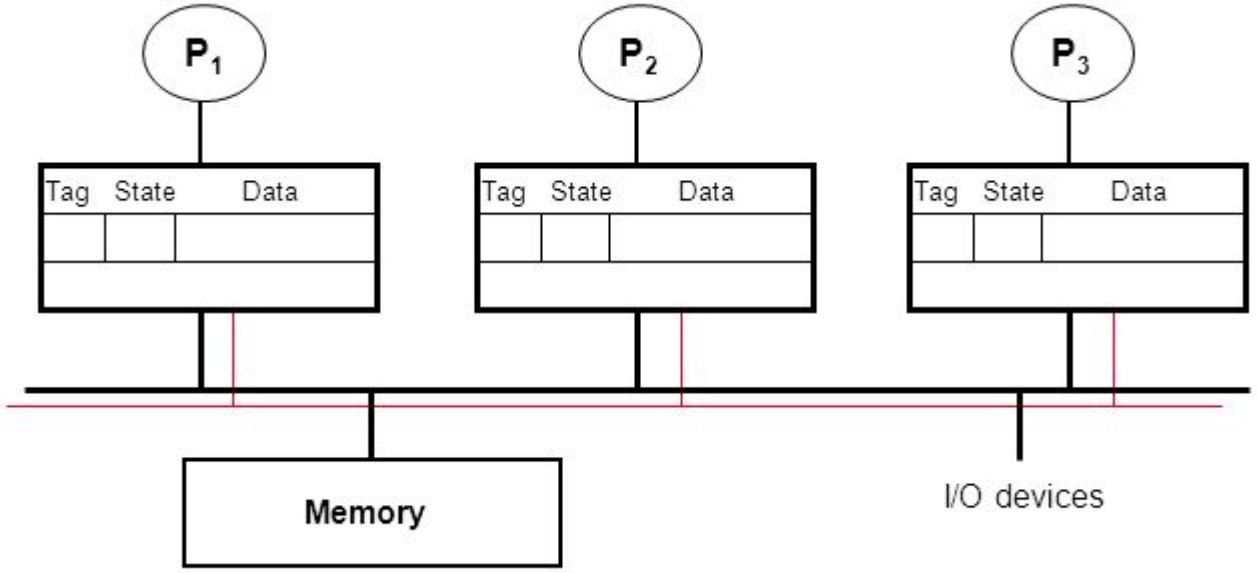

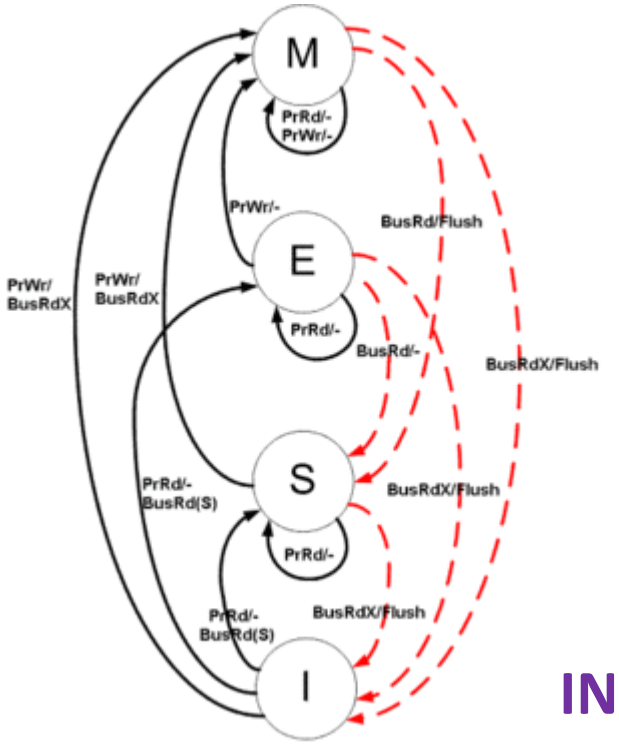

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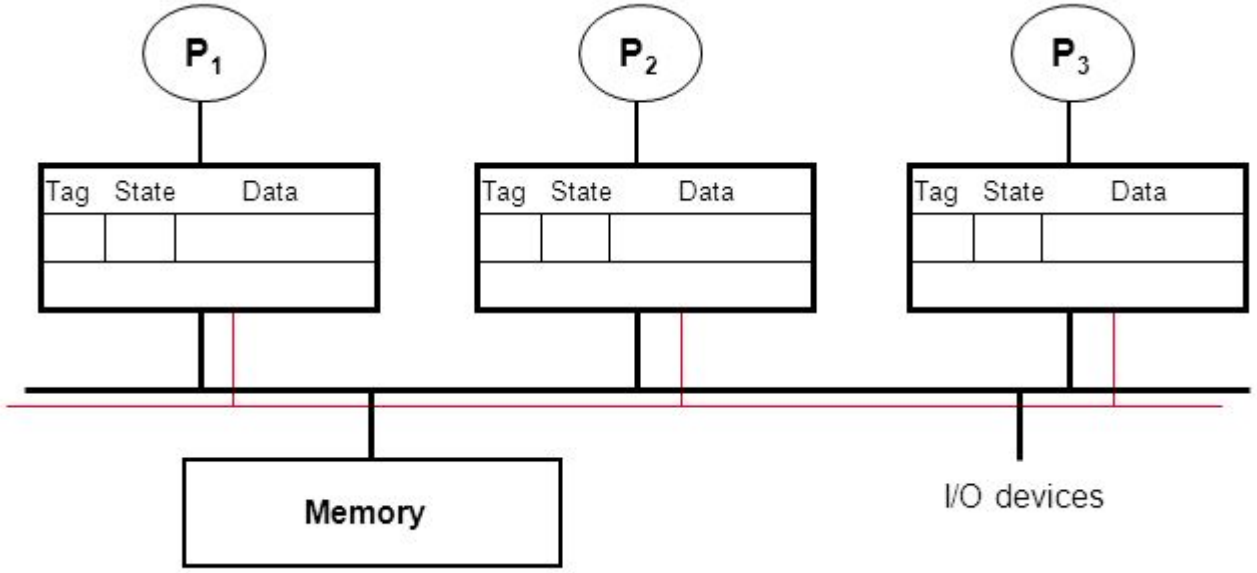
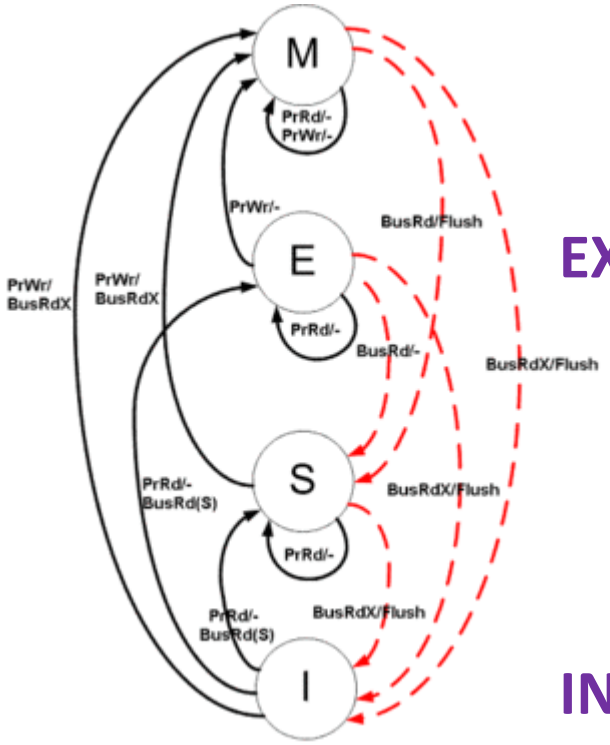
INVALID

Multiprocessor Cache Coherence





EXCLUSIVE

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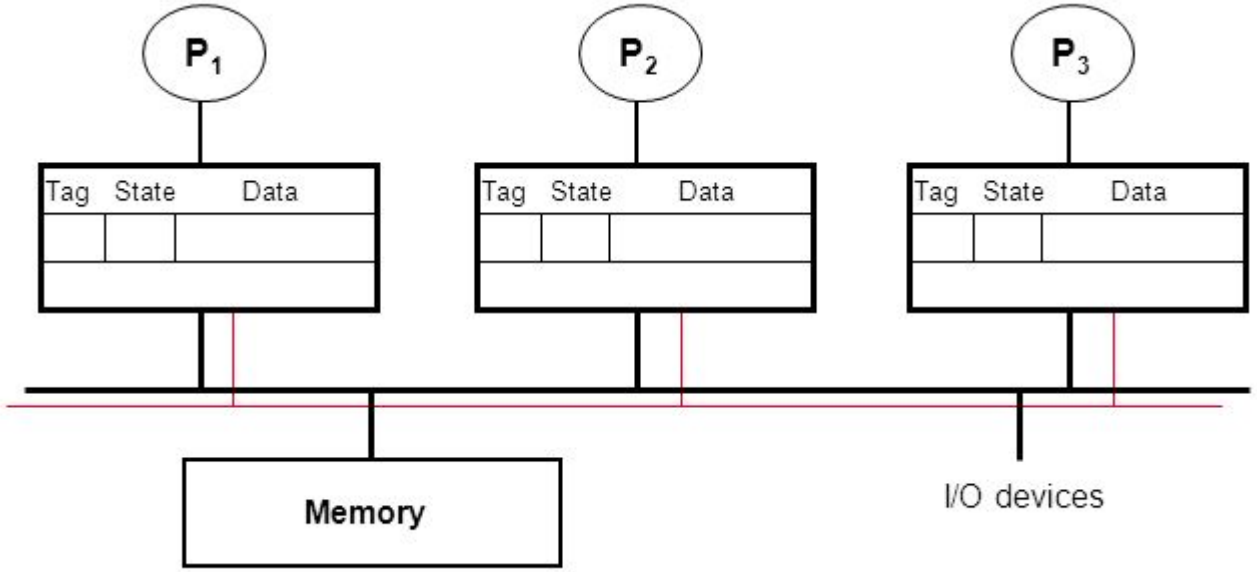

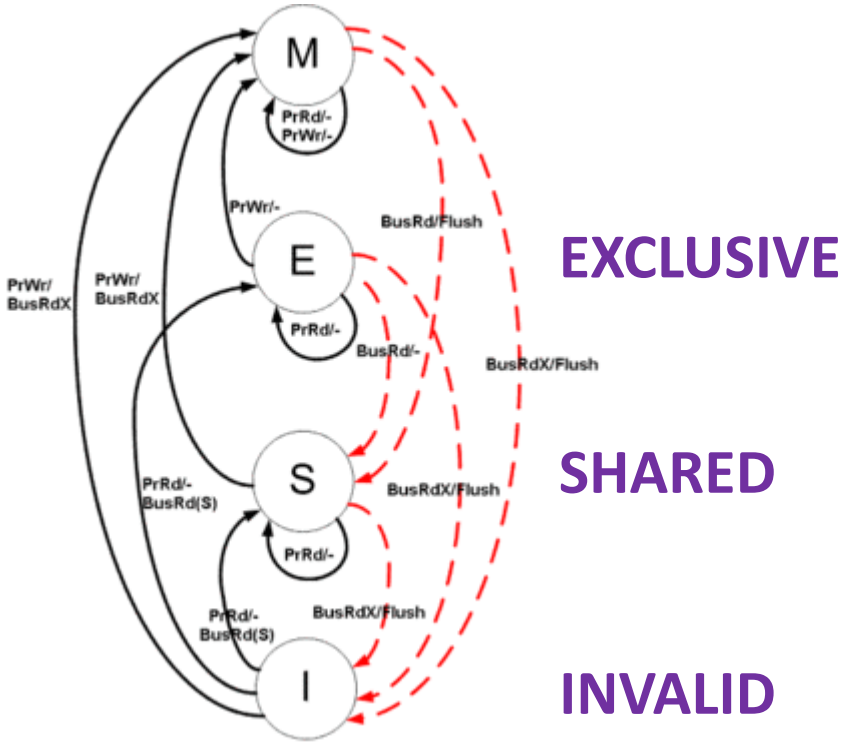

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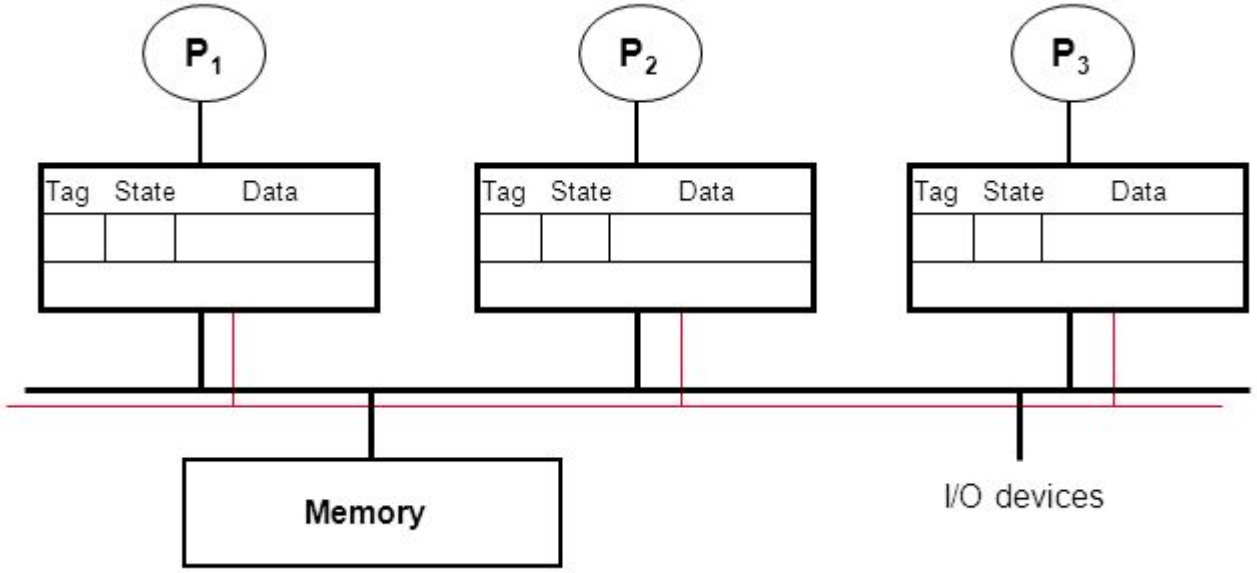

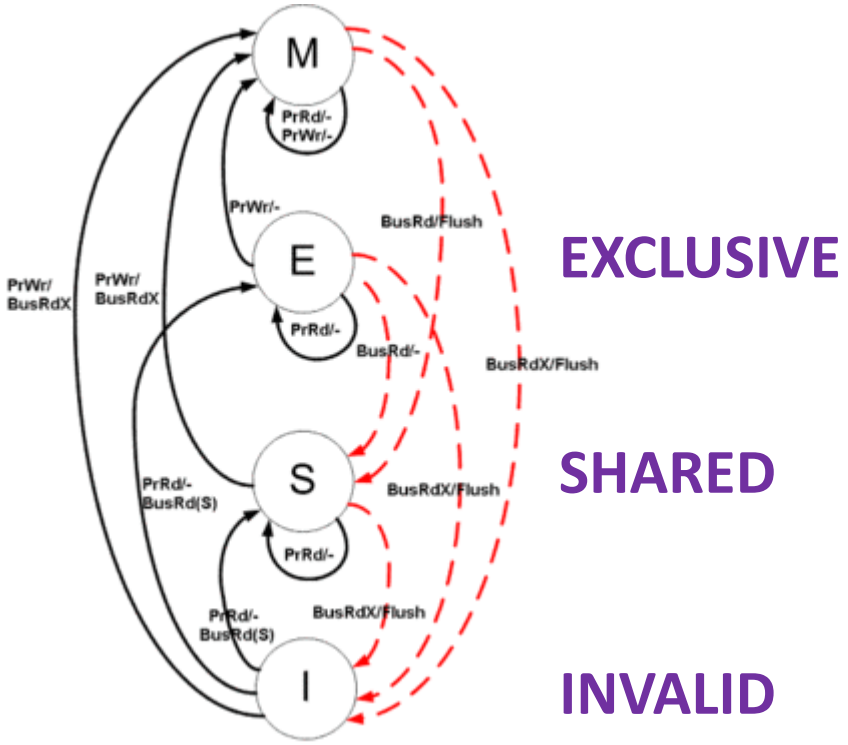

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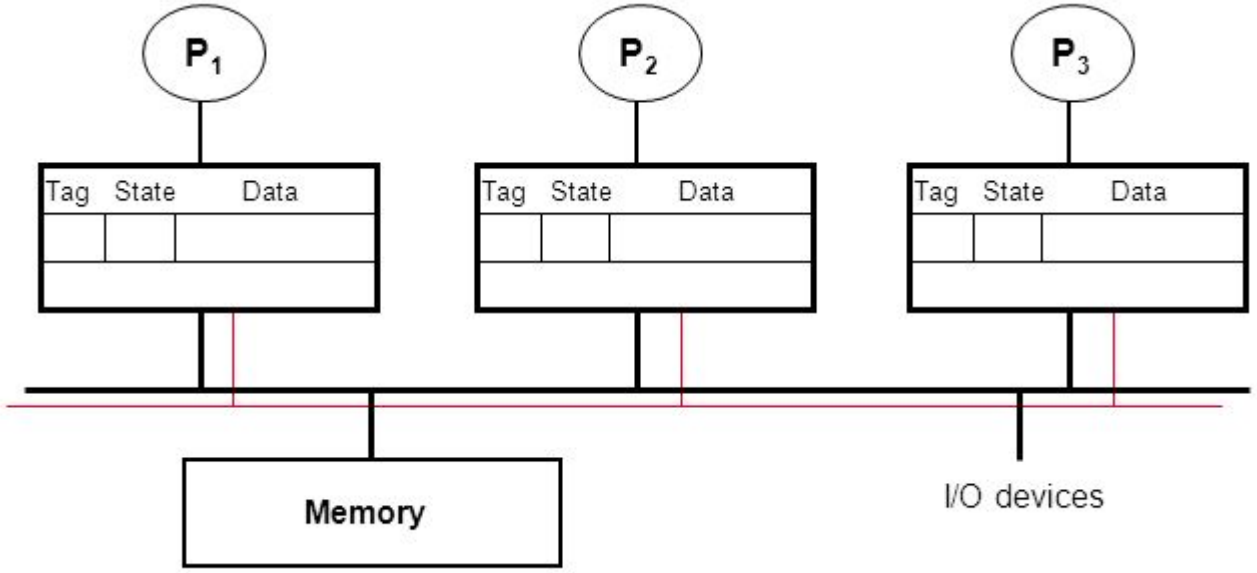

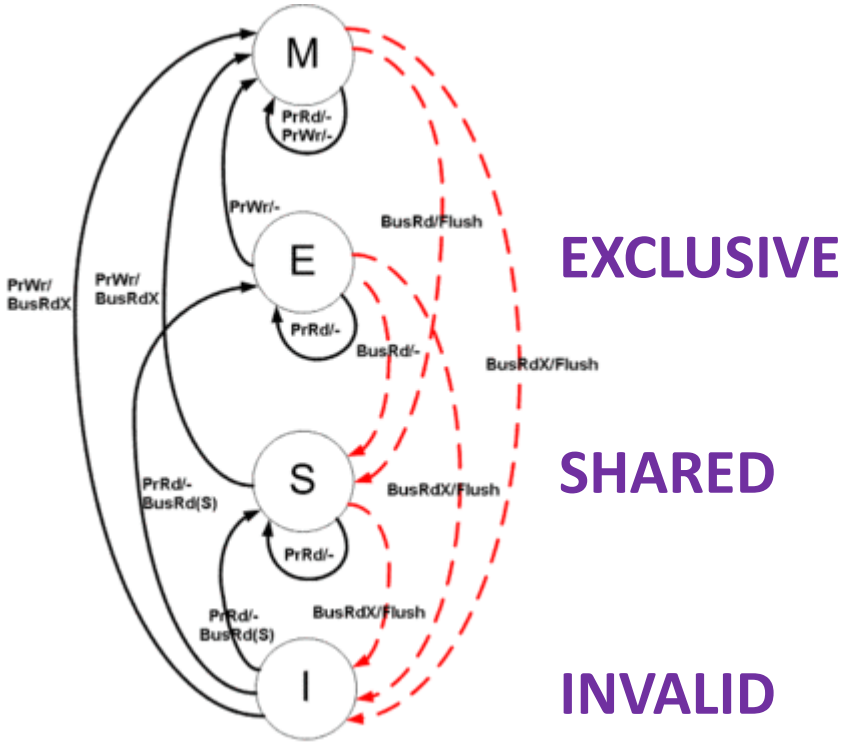

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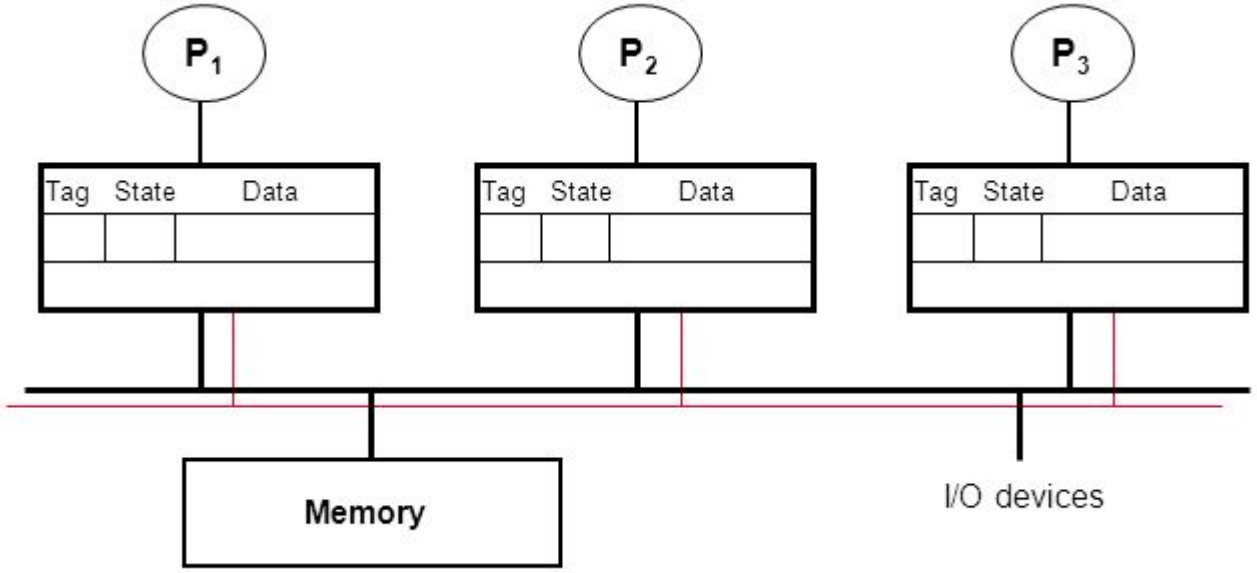

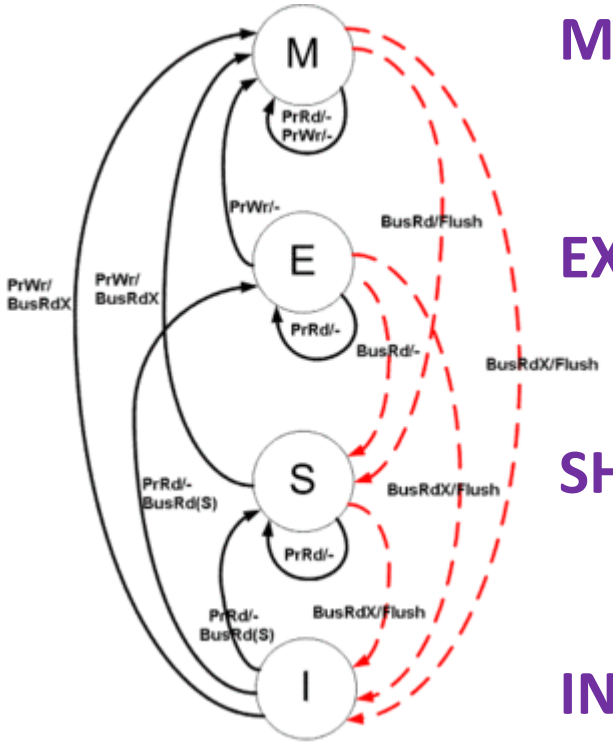

MODIFIED

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SHARED

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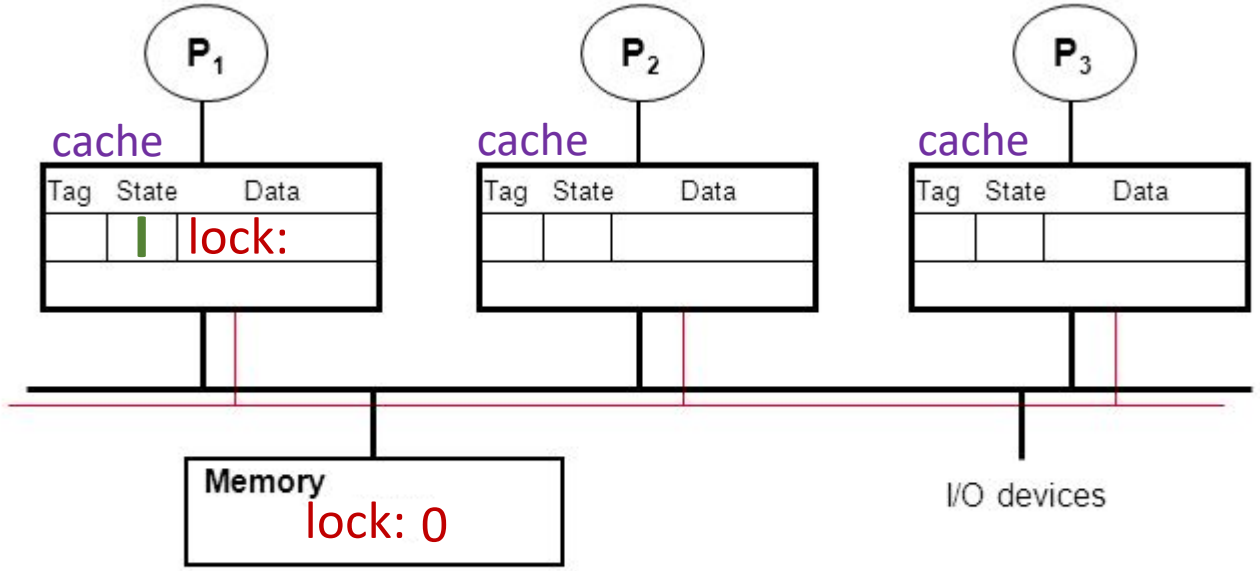
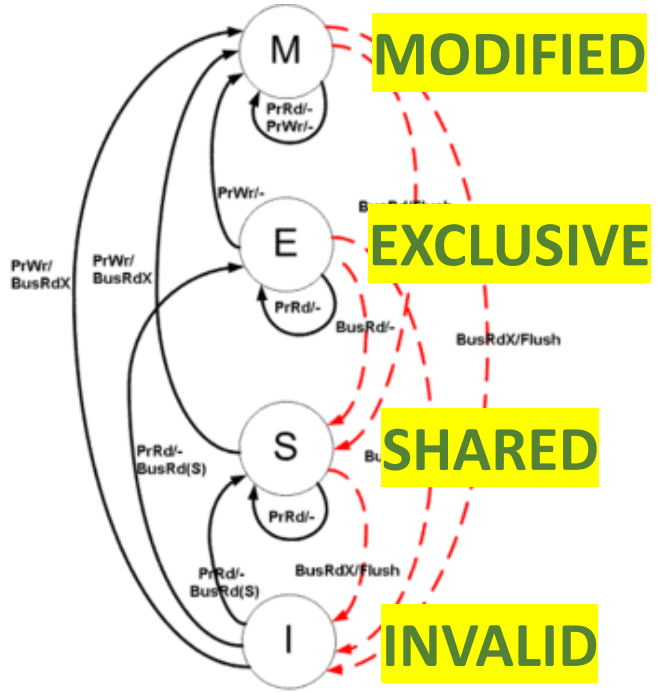
Cache Coherence: single-thread

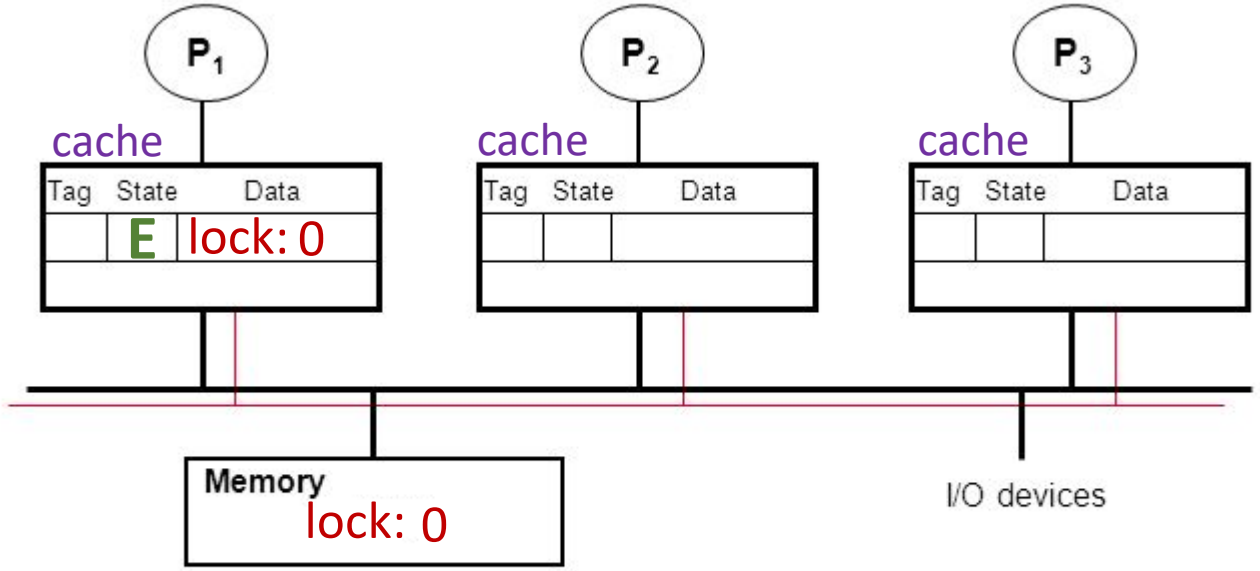


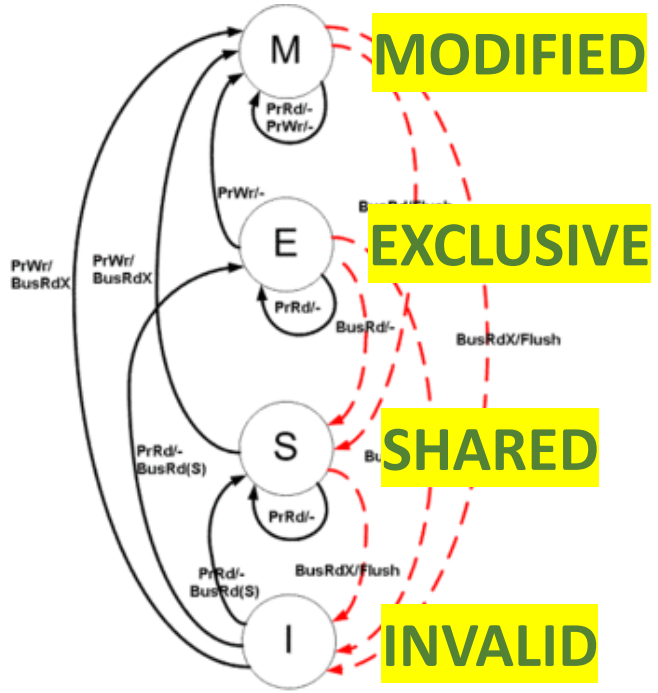


P1

```
// (straw-person lock impl)
// Initially, lock == 0 (unheld)
lock() {
try:  load lock, R0
        test R0
        bnz try
        store lock, 1
}
```

Cache Coherence: single-thread





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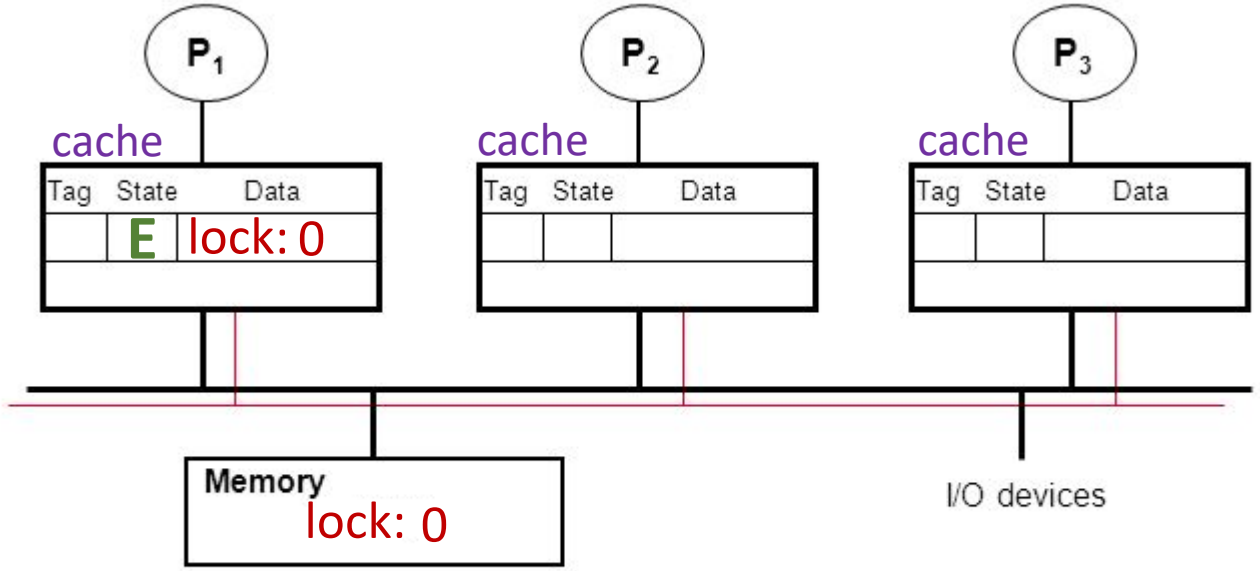
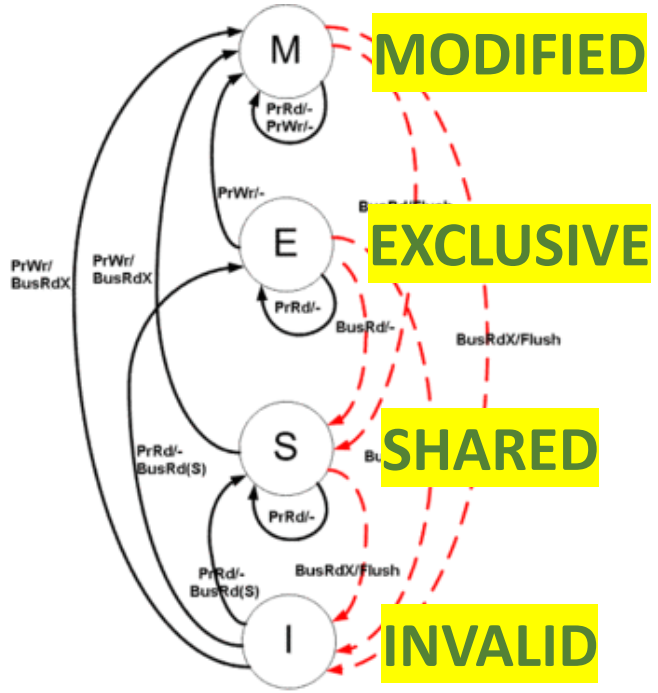
        store lock, 1
}
```

Cache Coherence: single-thread





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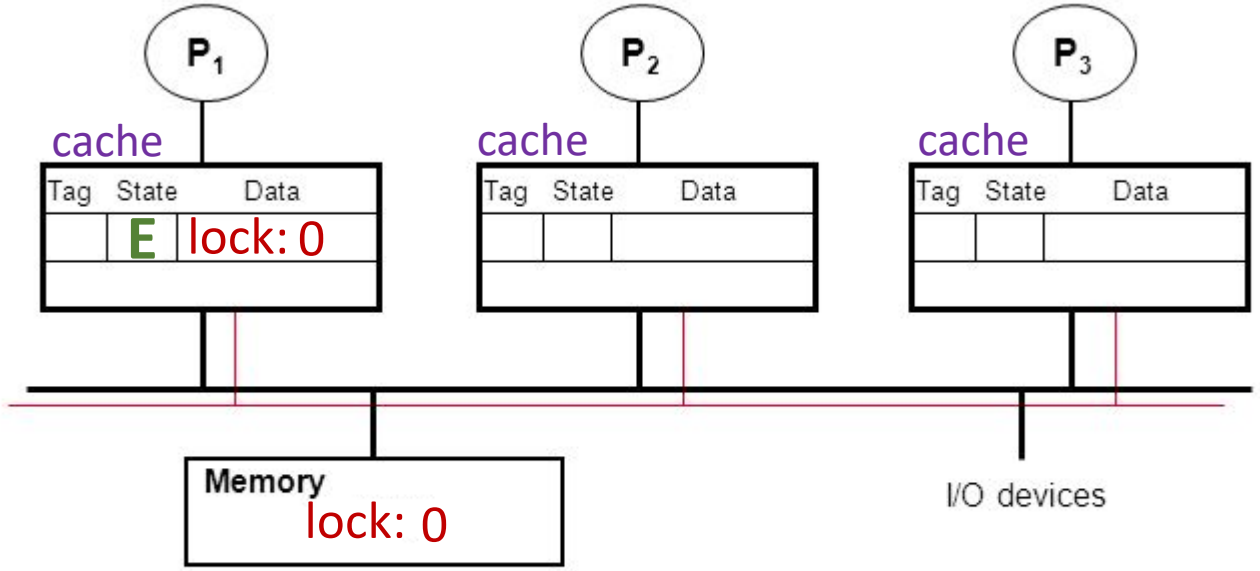
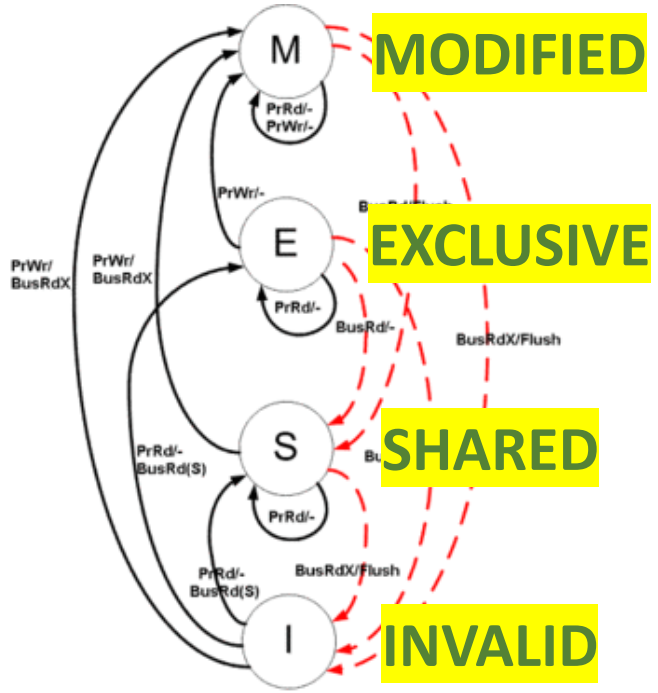
Cache Coherence: single-thread





P1

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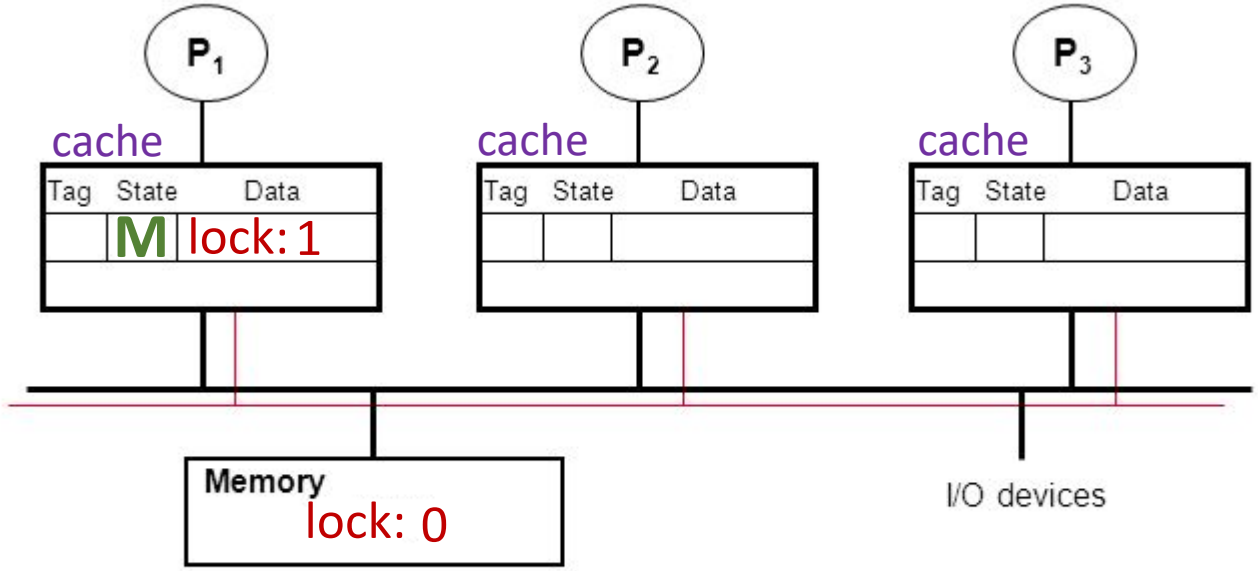
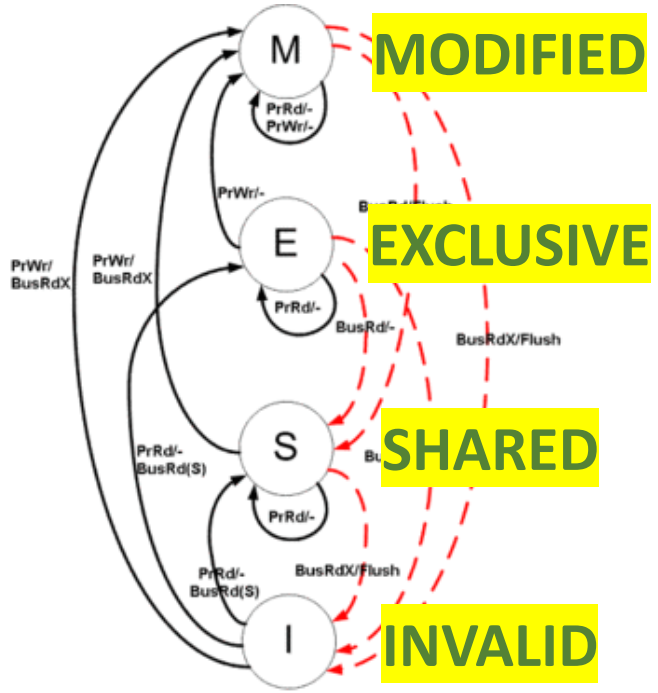
Cache Coherence: single-thread





P1

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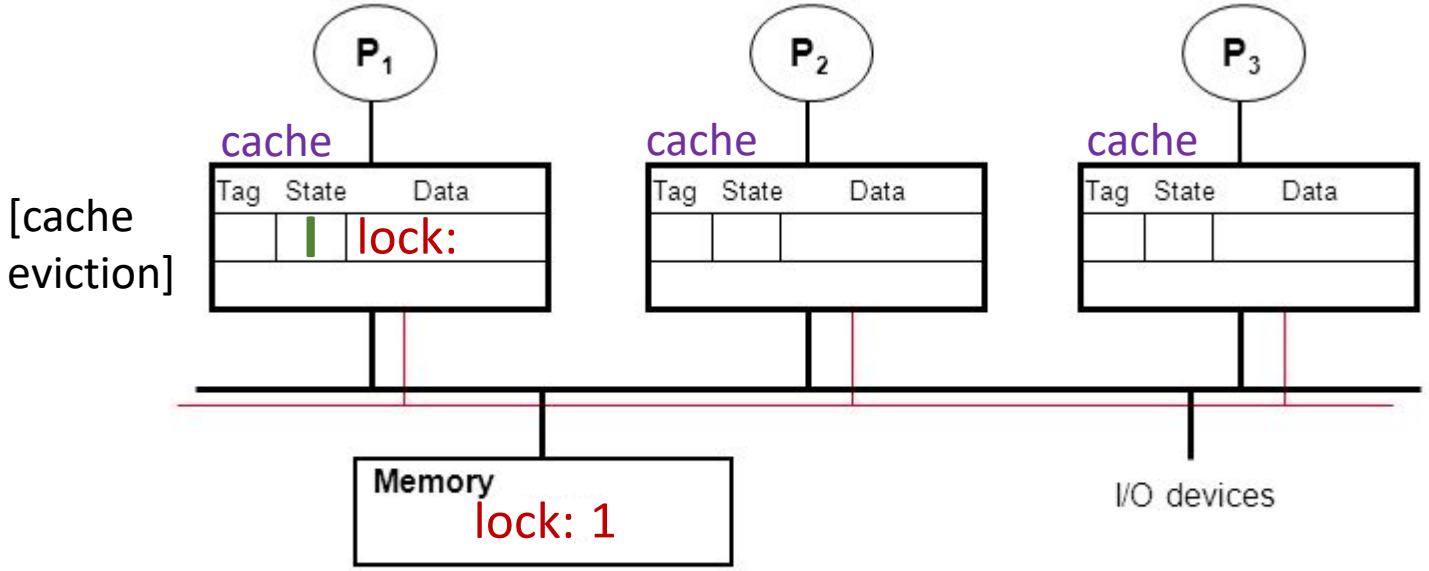
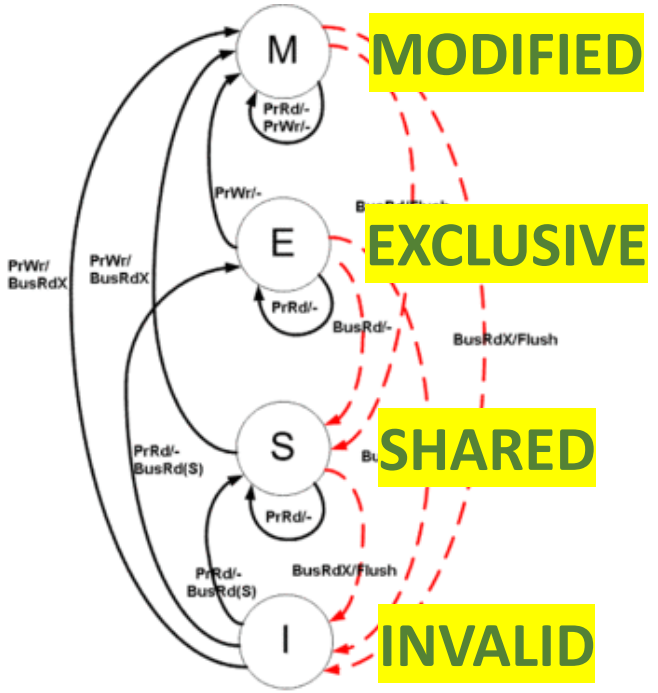
Cache Coherence: single-thread





P1

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```
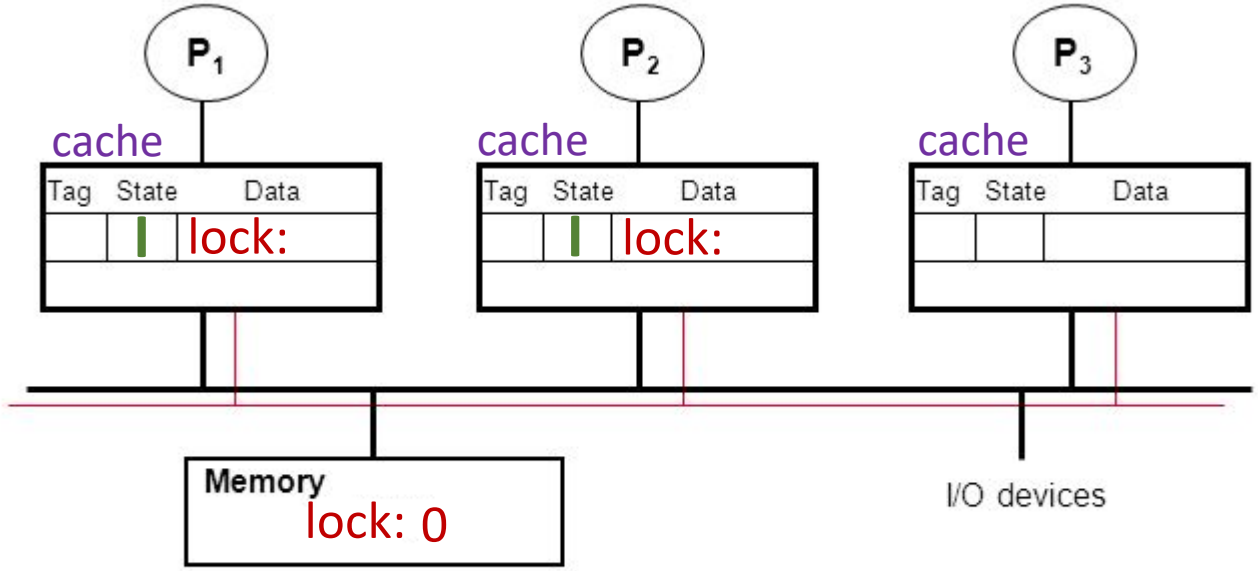
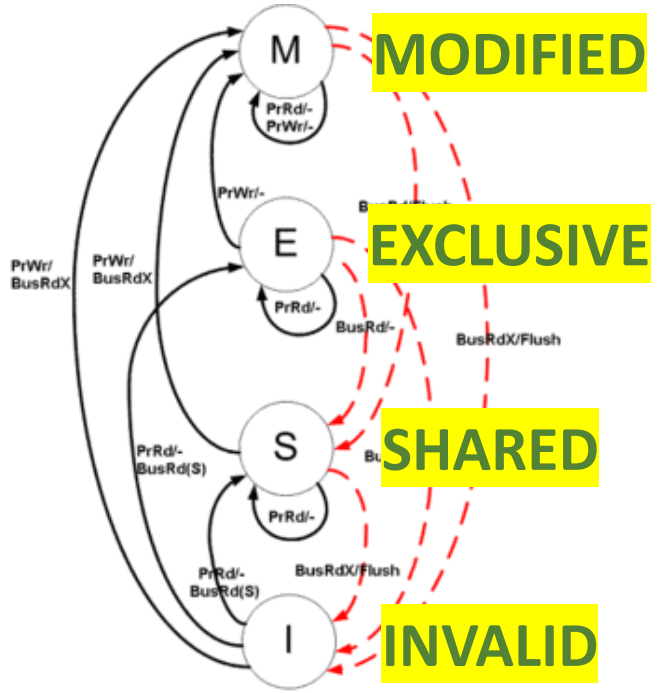

Cache Coherence Action Zone





P1

```
// (straw-person lock impl)
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        store lock, 1
}
```
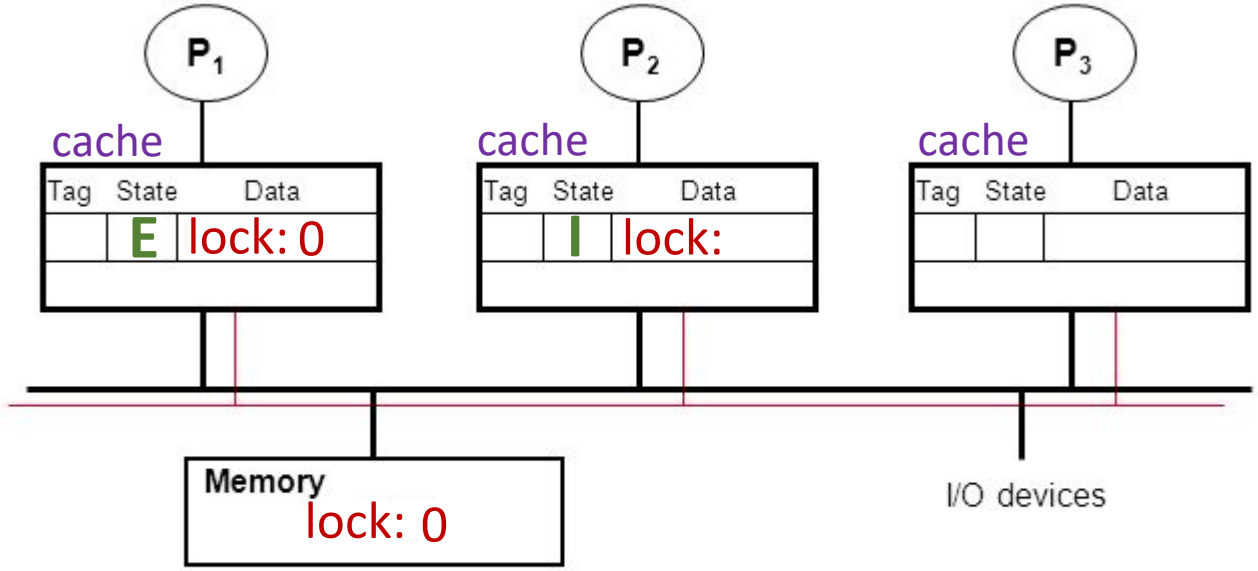
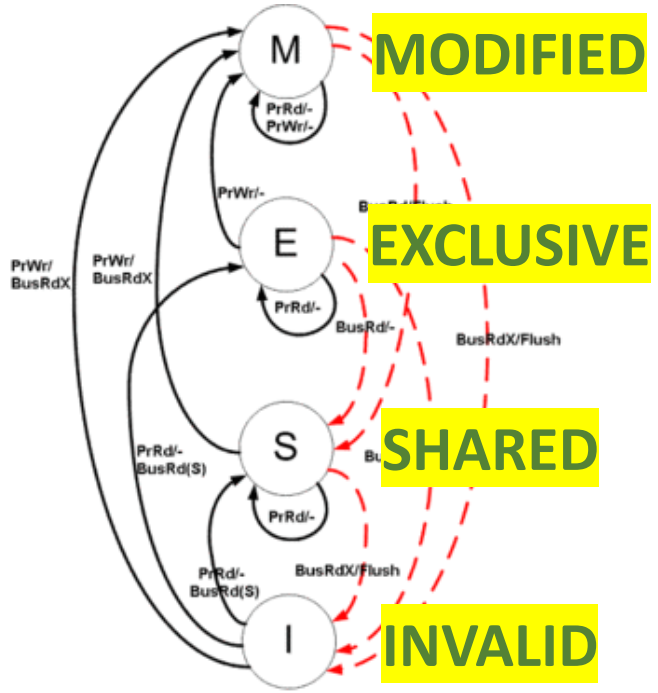

P2

```
// (straw-person lock impl)
// Initially, lock == 0 (unheld)
lock() {
try:  load lock, R0
        test R0
        bnz try
        store lock, 1
}
```

Cache Coherence Action Zone





P1

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```

P2

```
// (straw-person lock impl)
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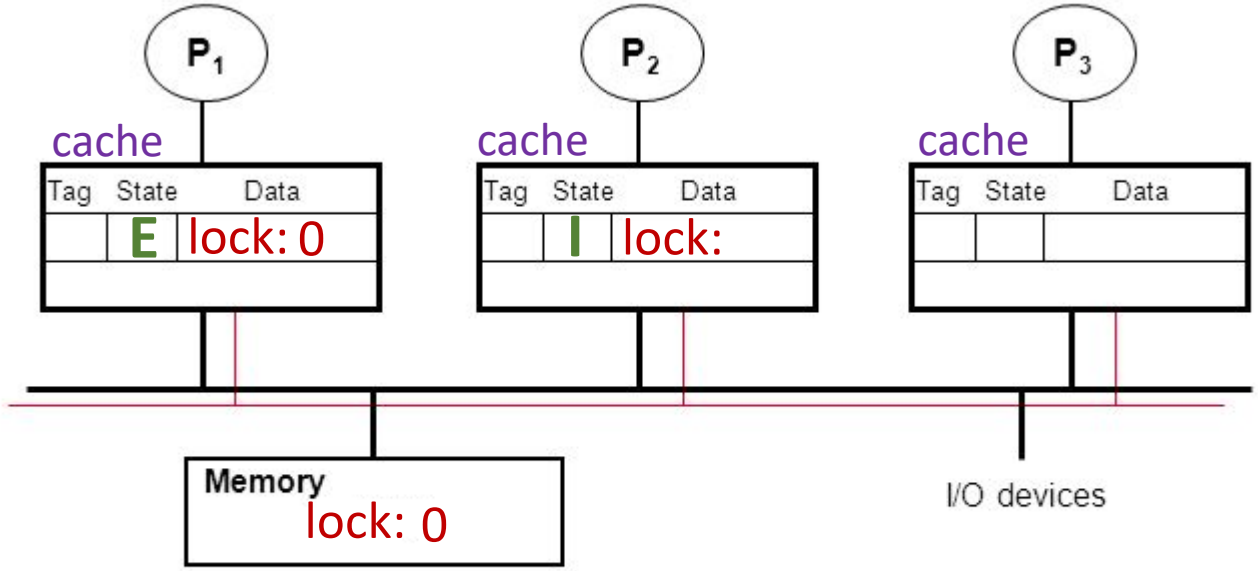
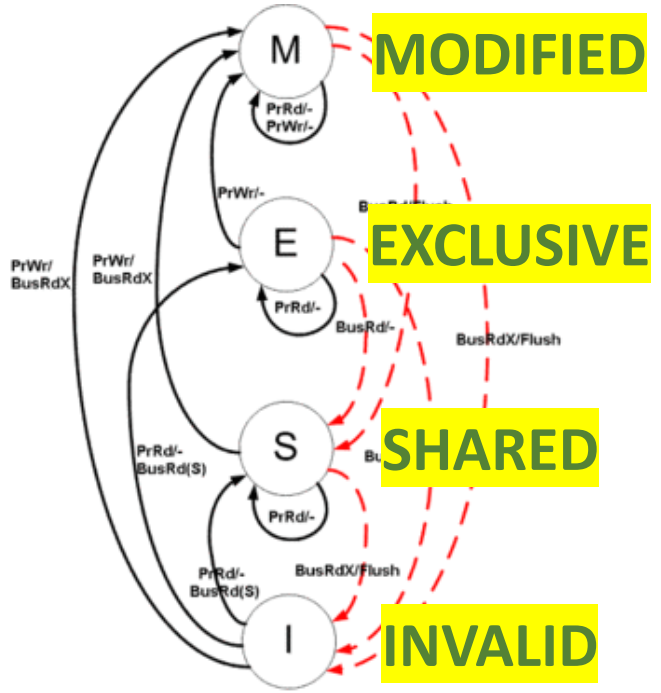
lock() {
try:  load lock, R0
        test R0
        bnz try
        store lock, 1
}
```

Cache Coherence Action Zone





P1

```
// (straw-person lock impl)
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P2

```
// (straw-person lock impl)
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lock() {
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        bnz try
        store lock, 1
}
```
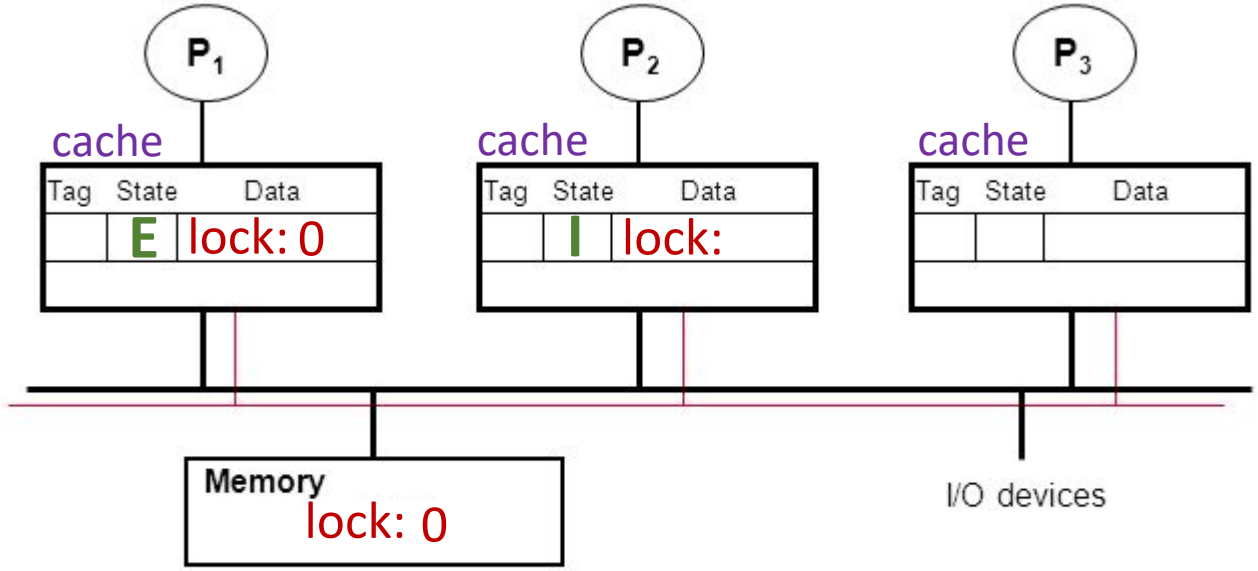
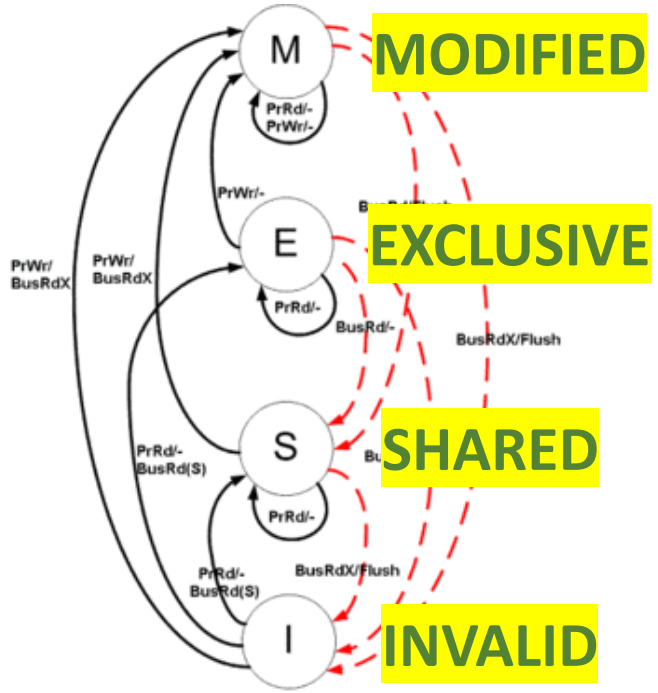

Cache Coherence Action Zone





P1

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P2

```
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        store lock, 1
}
```
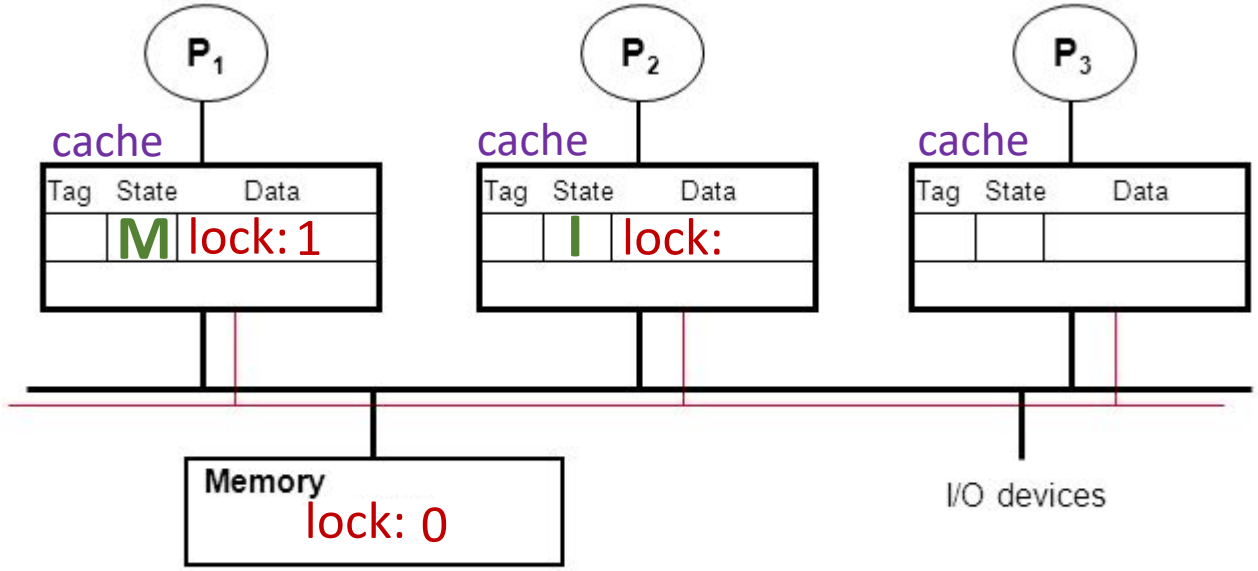
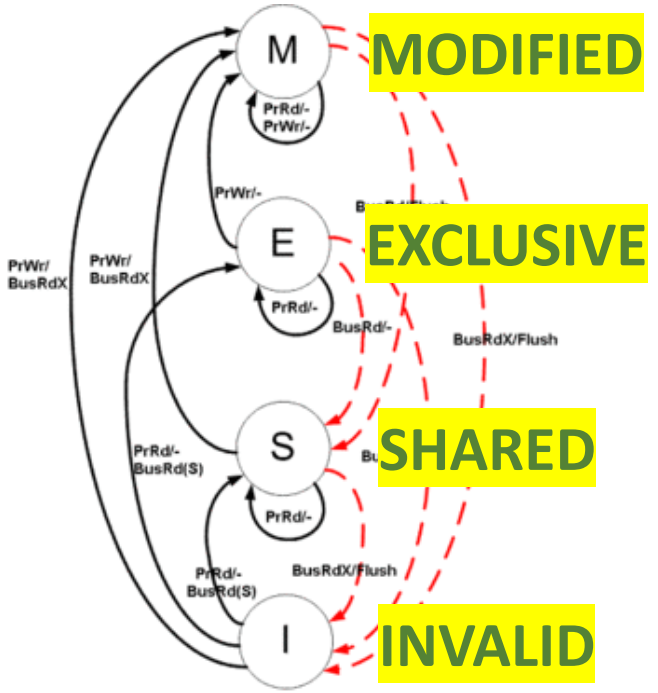

Cache Coherence Action Zone





P1

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// (straw-person lock impl)
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P2

```
// (straw-person lock impl)
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lock() {
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```
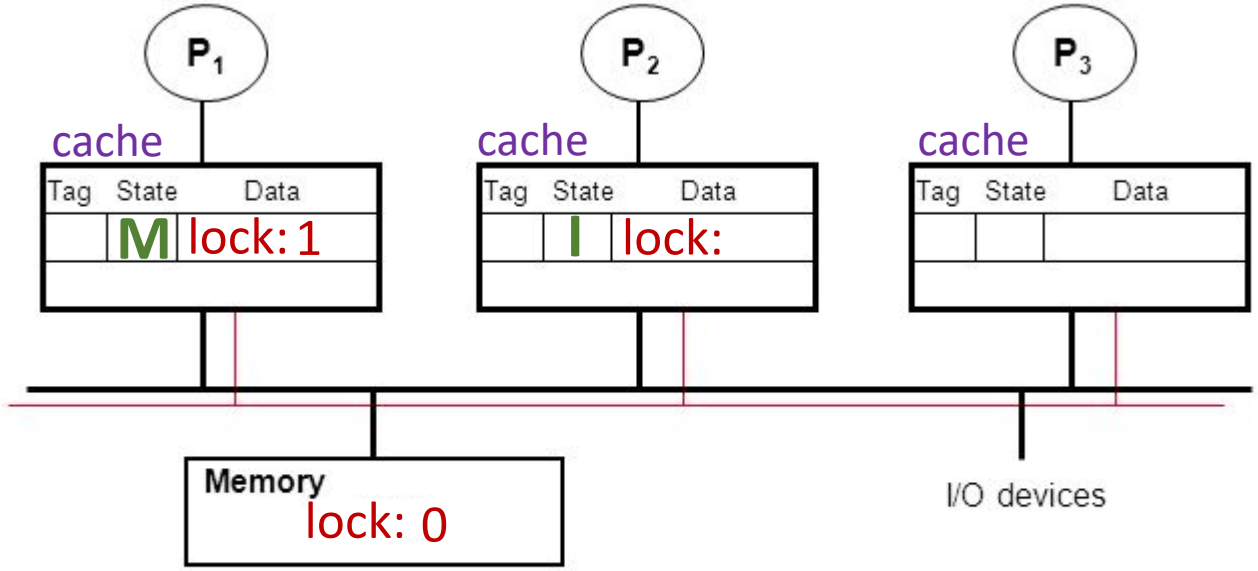
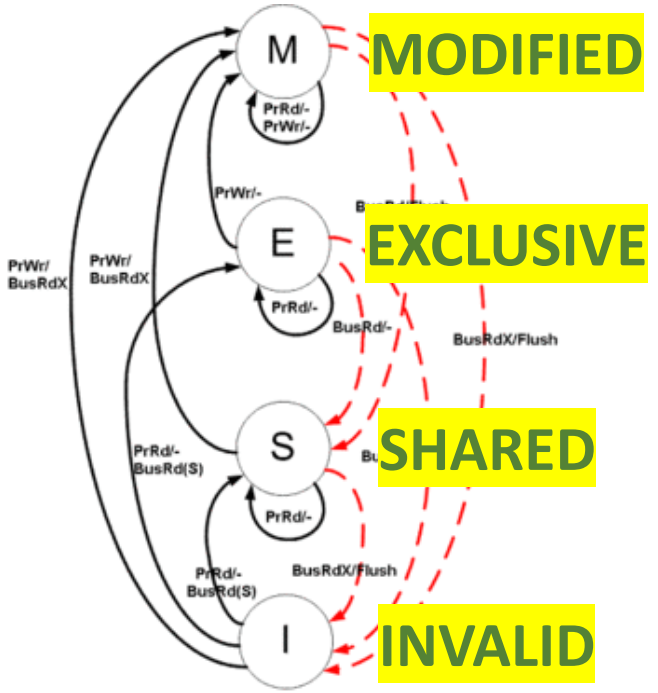

Cache Coherence Action Zone





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P2

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// (straw-person lock impl)
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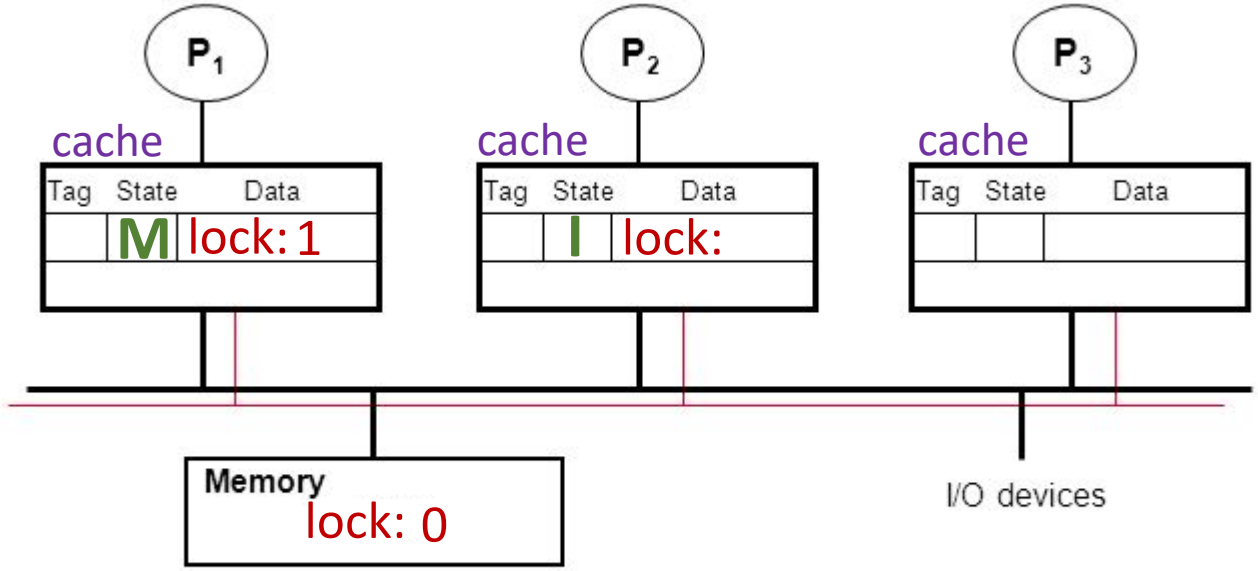
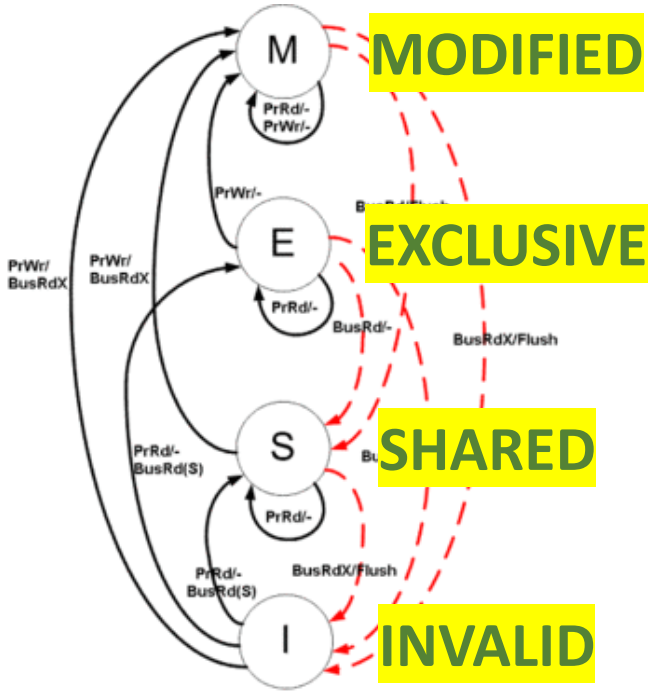
Cache Coherence Action Zone





P1

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P2

```
// (straw-person lock impl)
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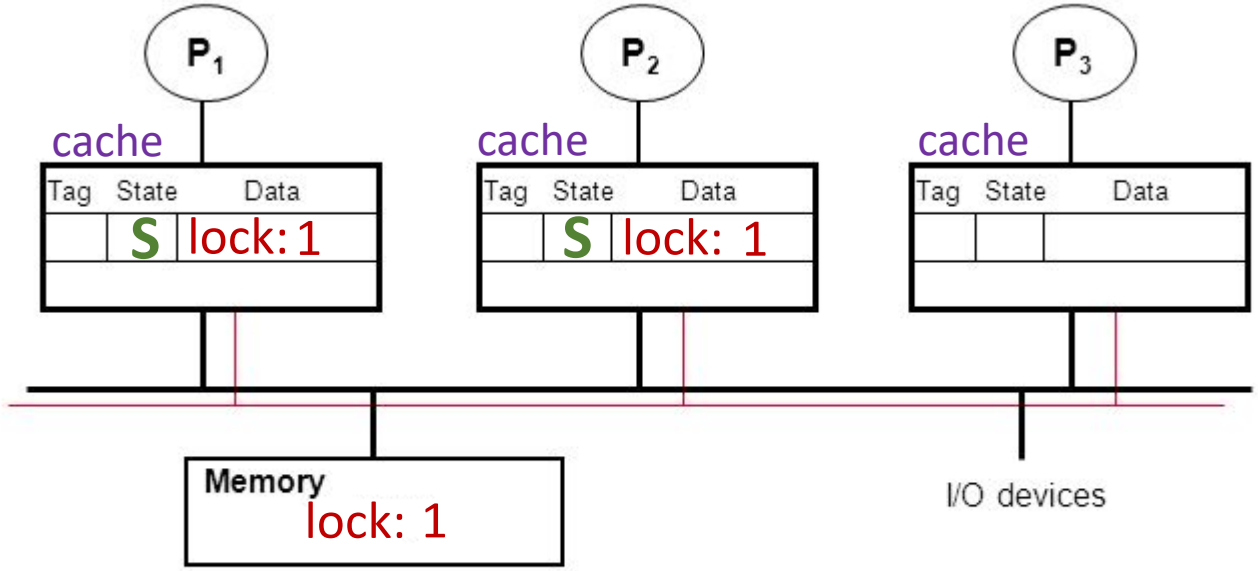
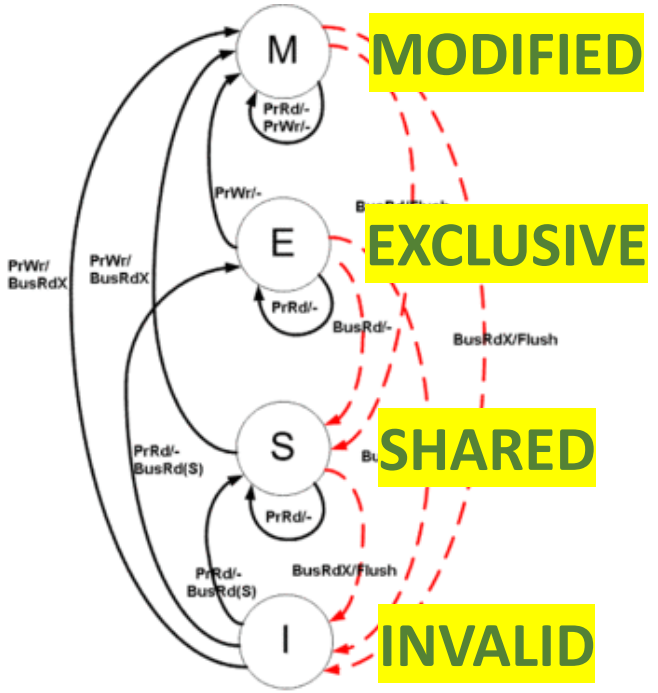
Cache Coherence Action Zone





P1

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P2

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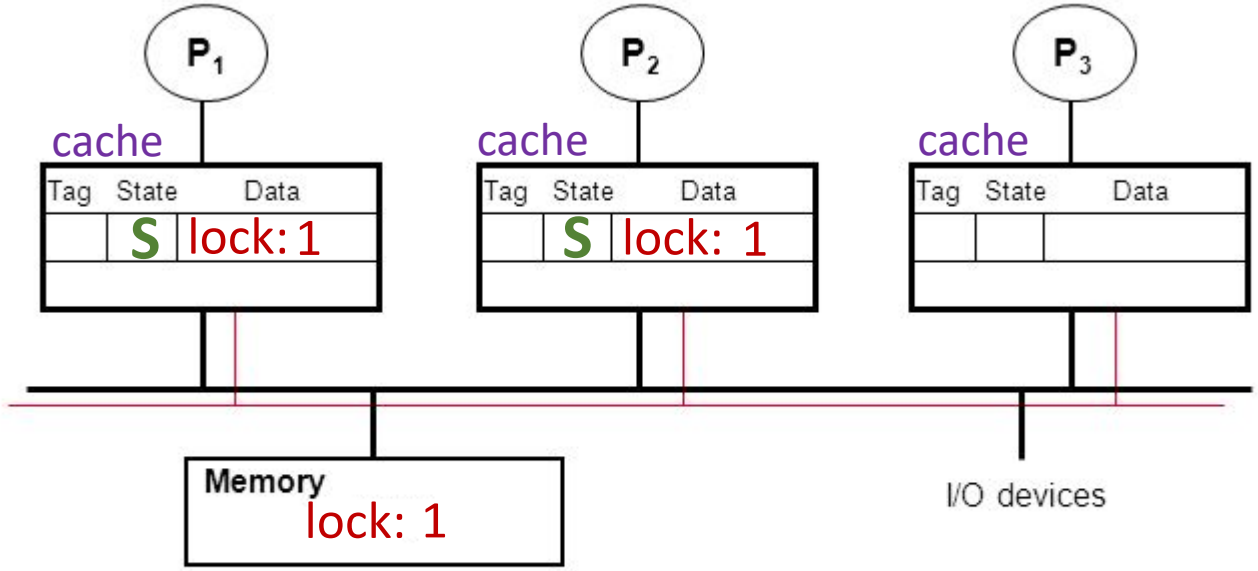
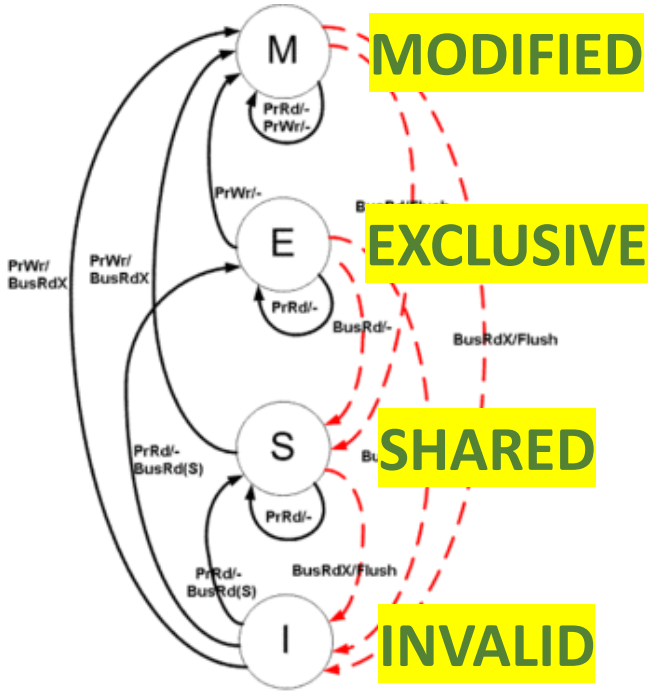
Cache Coherence Action Zone





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P2

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```
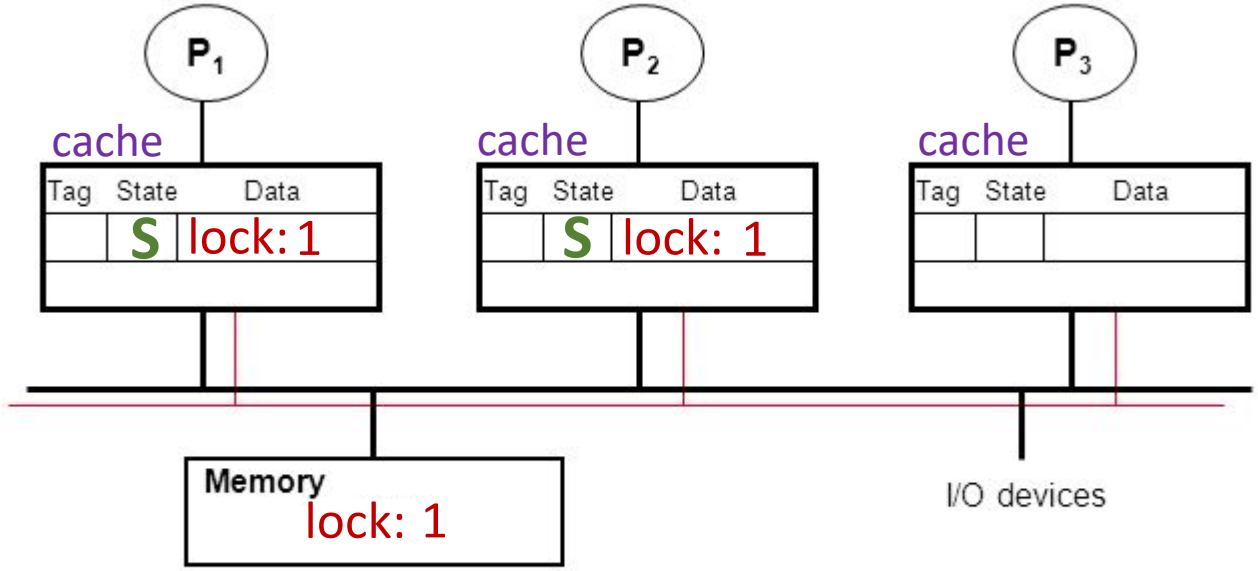
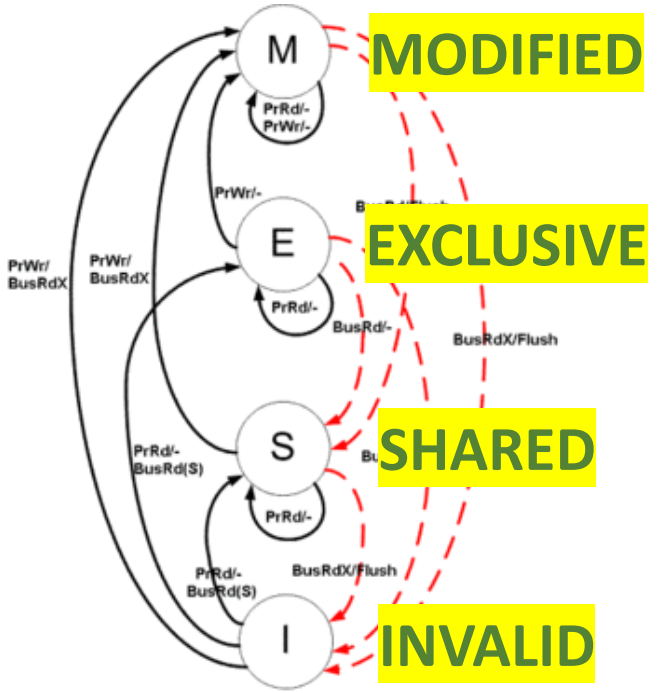

Cache Coherence Action Zone





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P2

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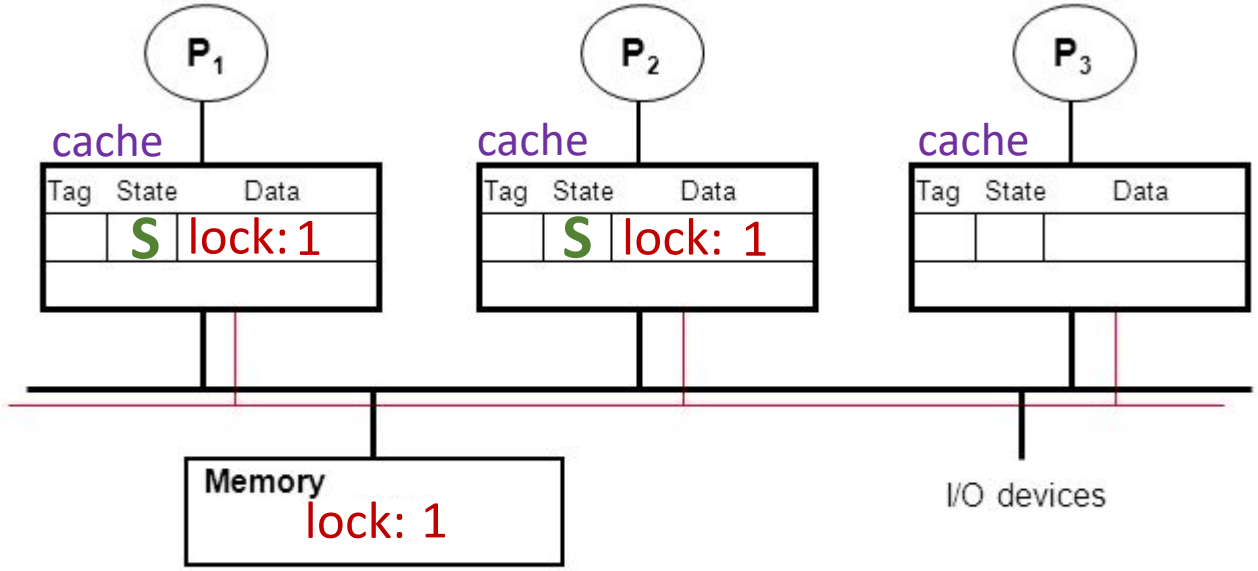
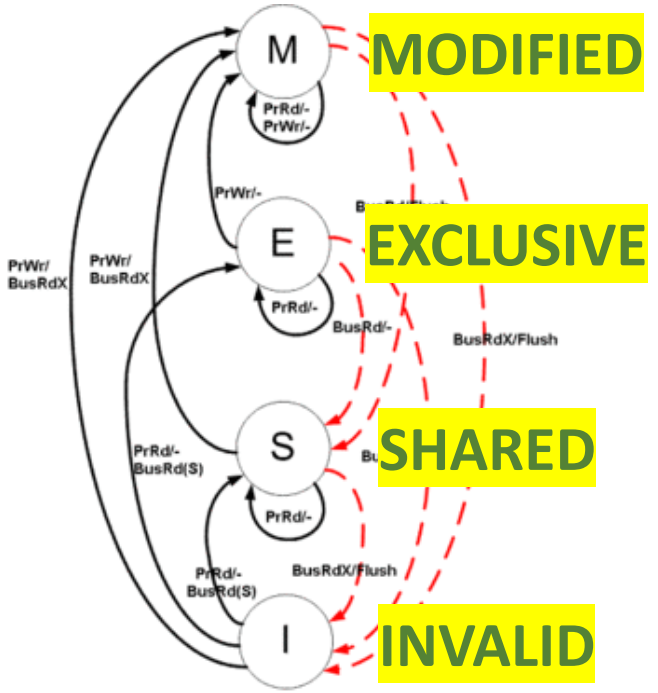
Cache Coherence Action Zone





P1

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}
```

SAFE!

P2

```
// (straw-person lock impl)
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try:  load lock, R0
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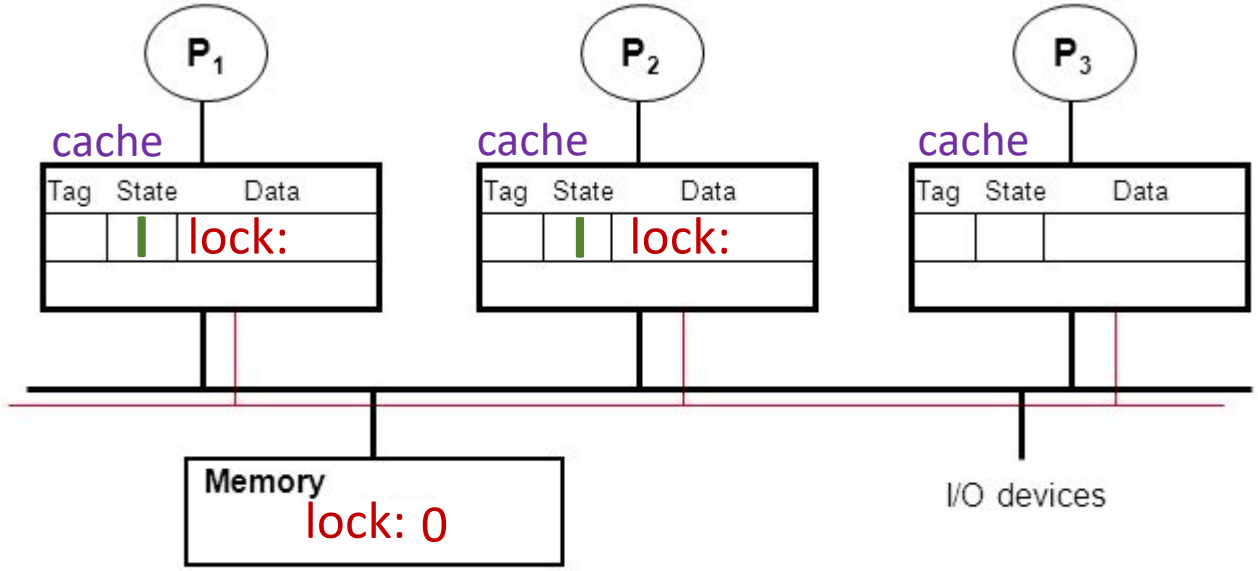
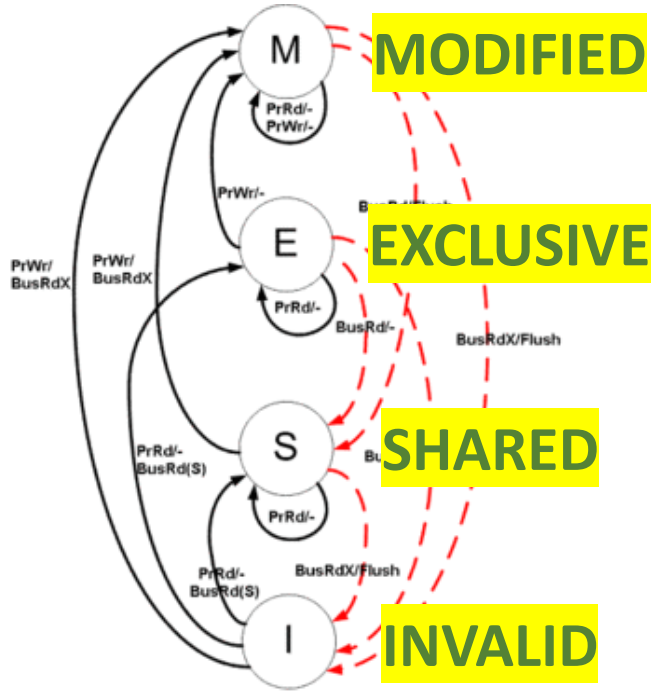
```

Cache Coherence Action Zone II





P1

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P2

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// (straw-person lock impl)
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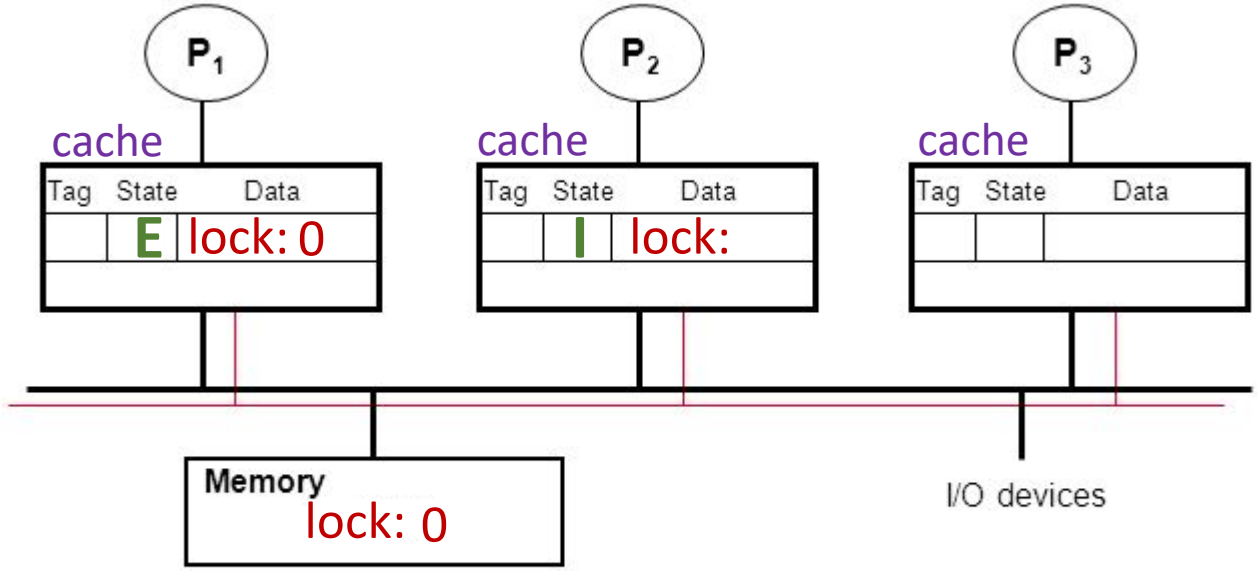
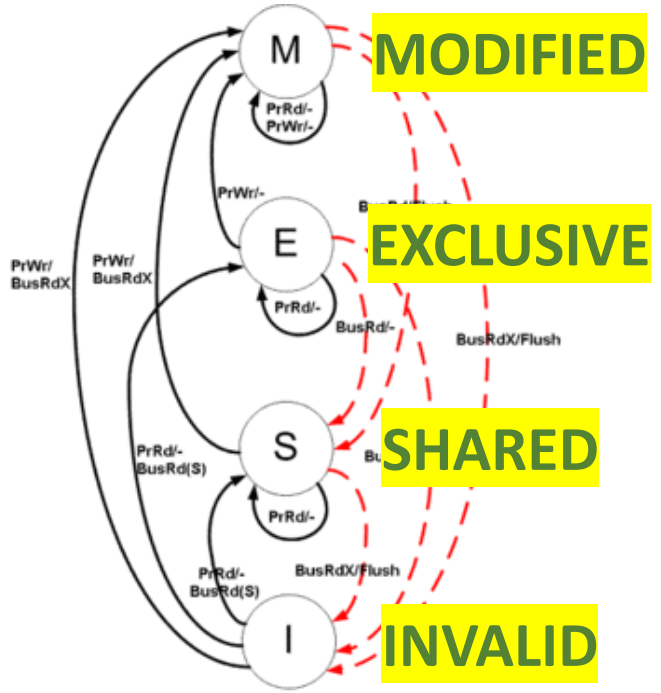
Cache Coherence Action Zone II





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P2

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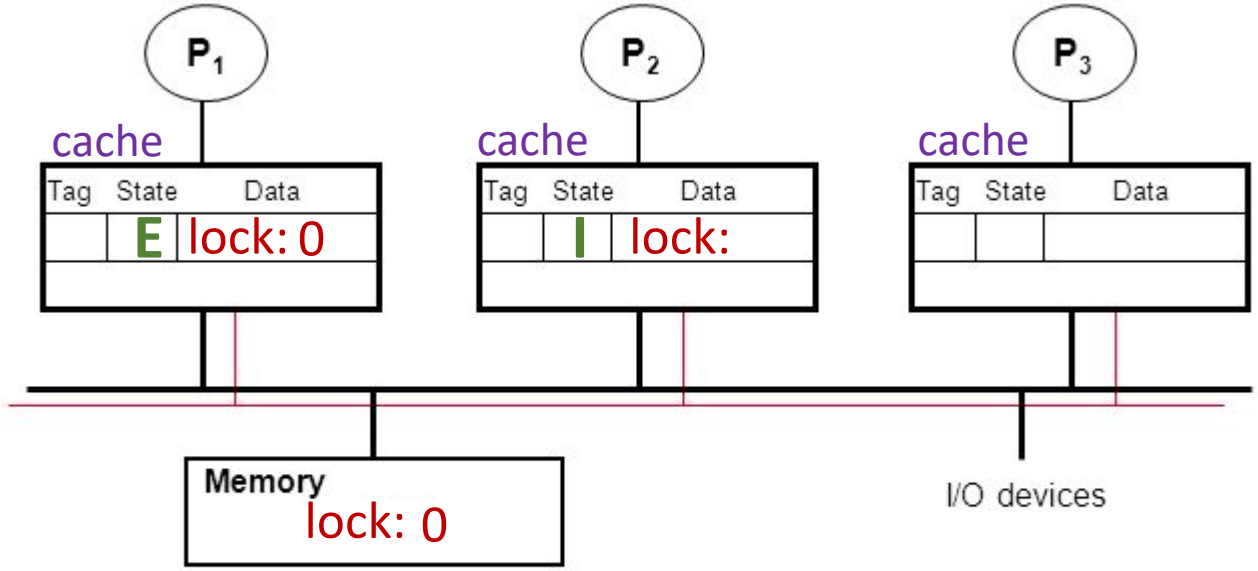
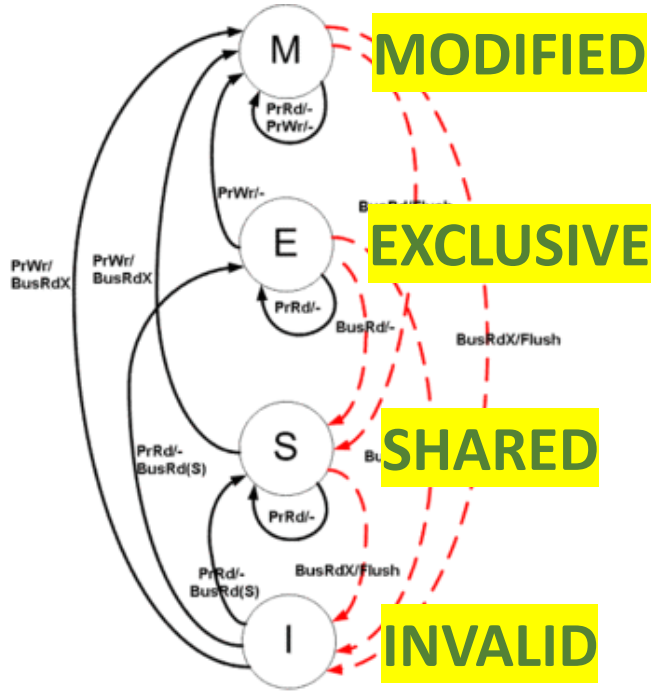
Cache Coherence Action Zone II





P1

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P2

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}
```
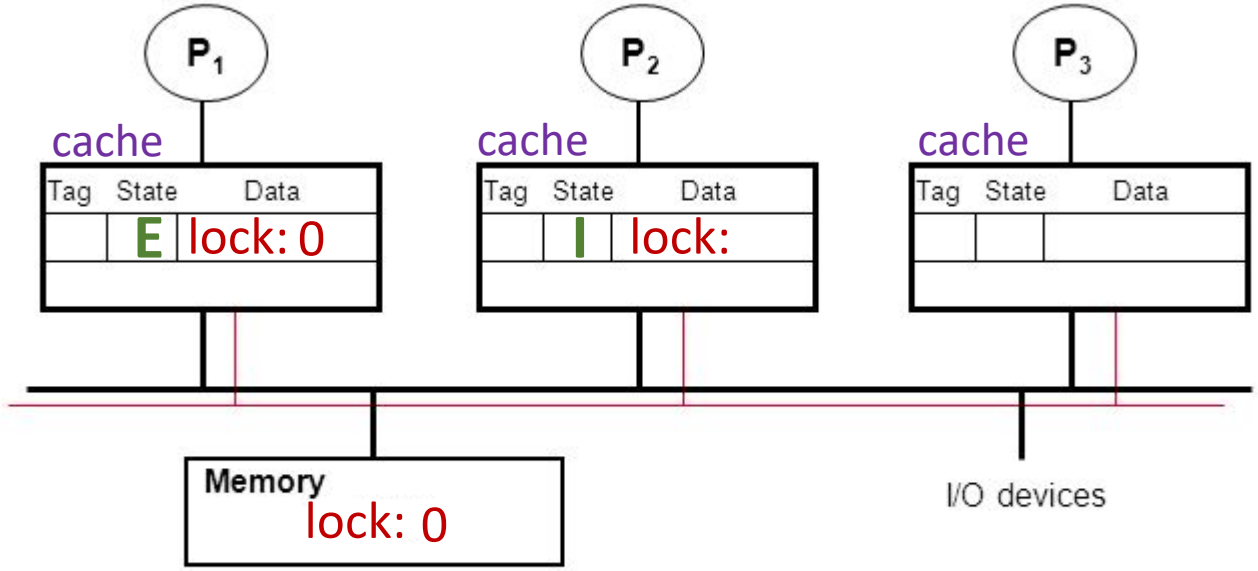
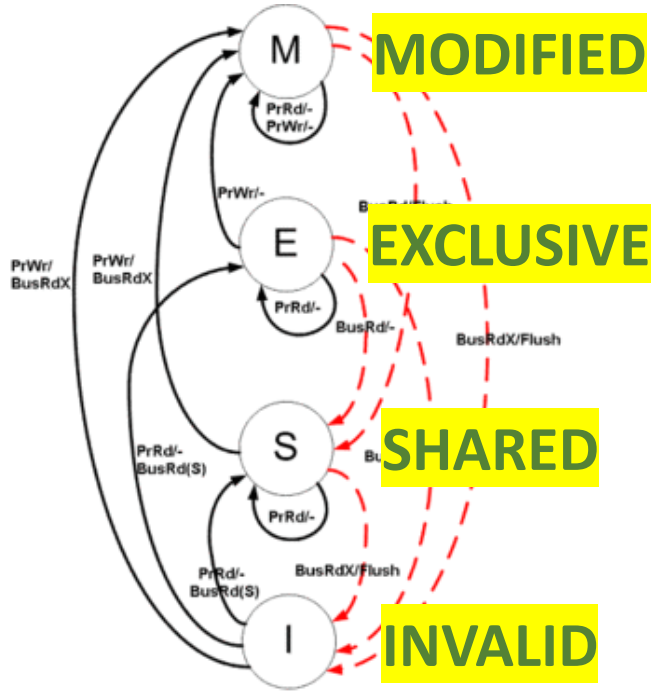

Cache Coherence Action Zone II





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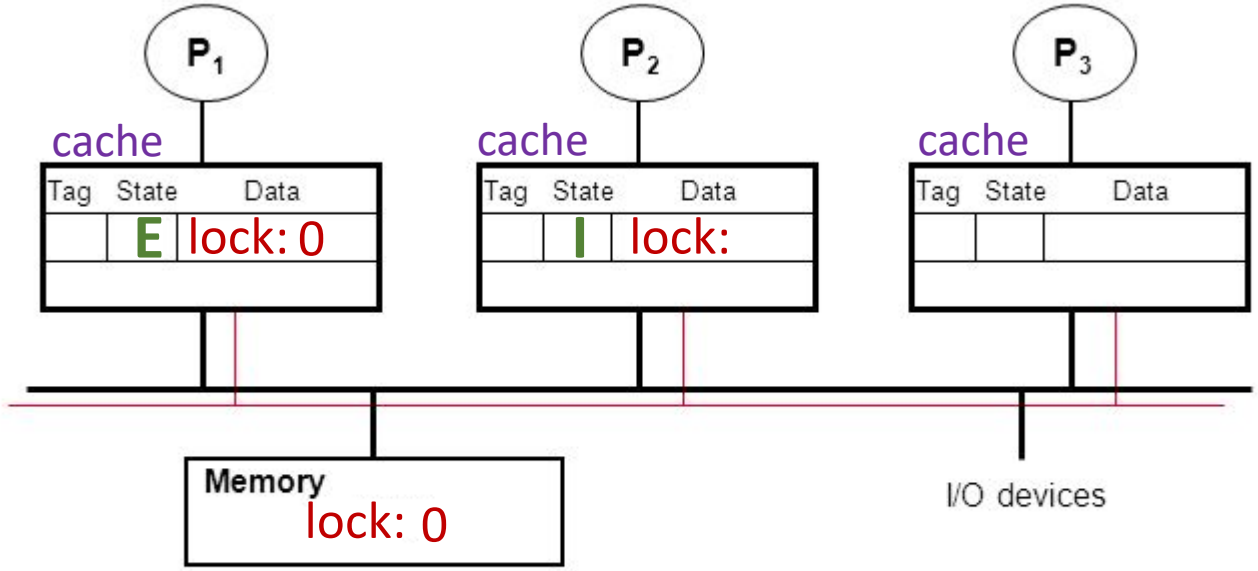
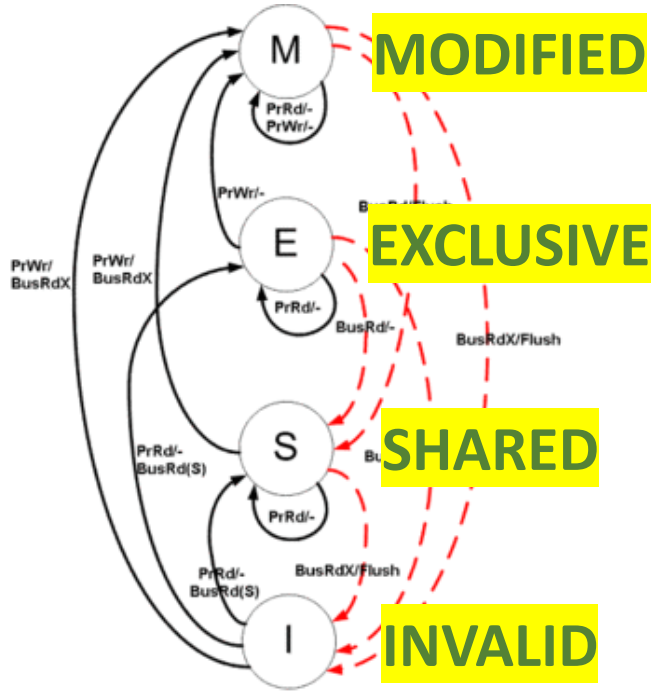
        test R0
        bnz try
        store lock, 1
}
```

P2

```
// (straw-person lock impl)
// Initially, lock == 0 (unheld)
lock() {
try:  load lock, R0
        test R0
        bnz try
        store lock, 1
}
```

Cache Coherence Action Zone II





P1

```
// (straw-person lock impl)
// Initially, lock == 0 (unheld)
lock() {
try:  load lock, R0
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```

P2

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// (straw-person lock impl)
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        test R0
        bnz try
        store lock, 1
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```
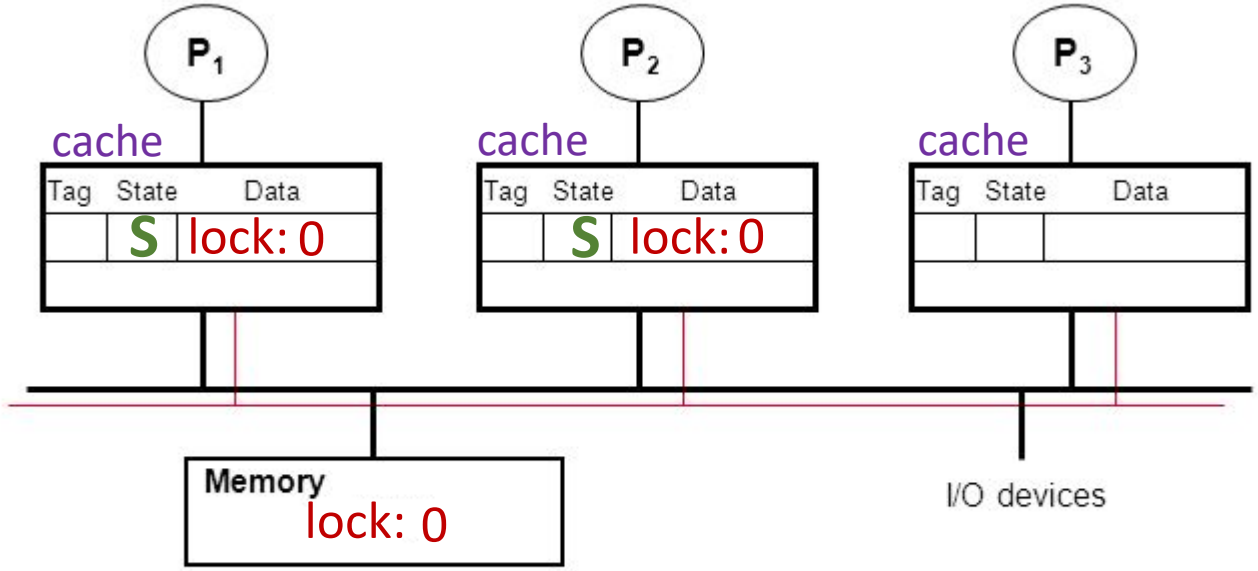
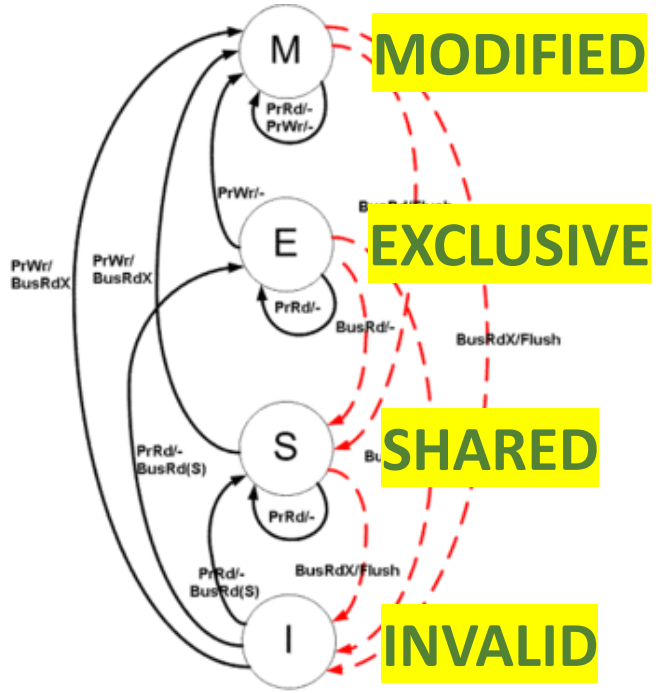

Cache Coherence Action Zone II





P1

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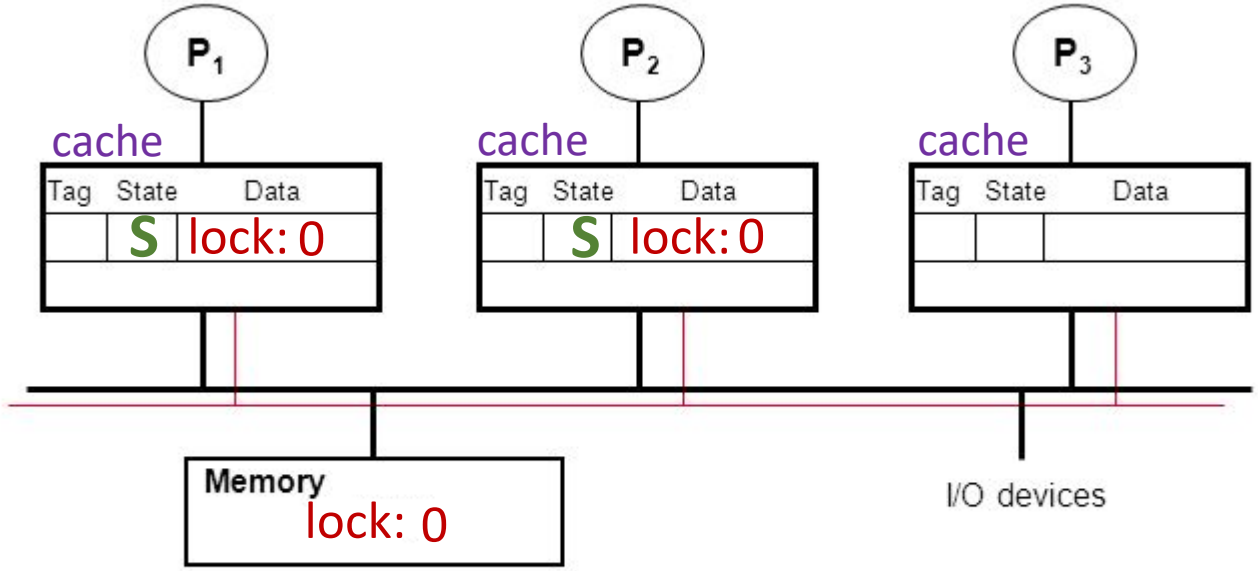
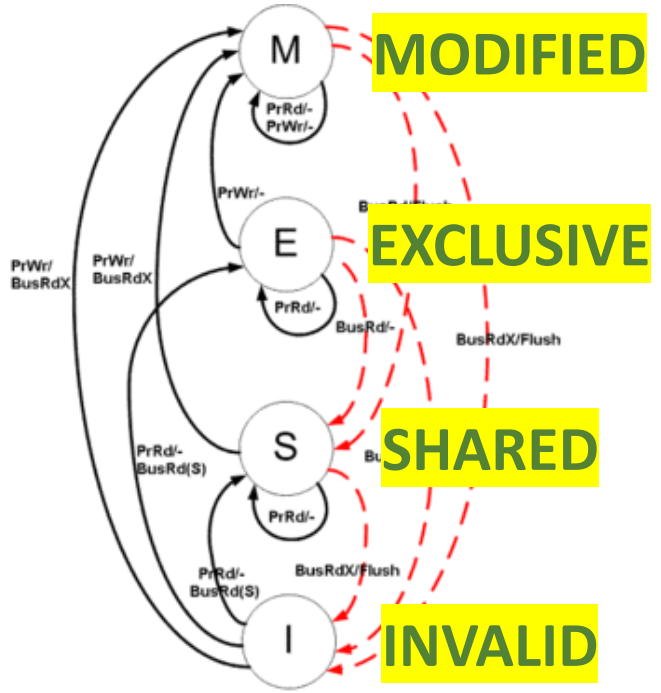
```

Cache Coherence Action Zone II





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```
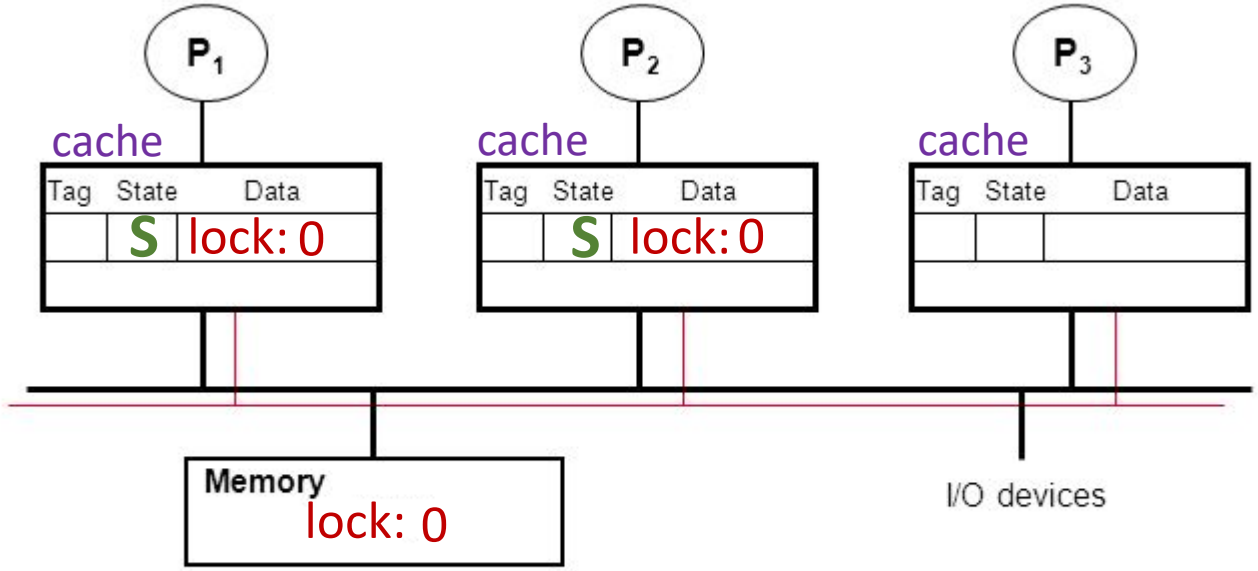
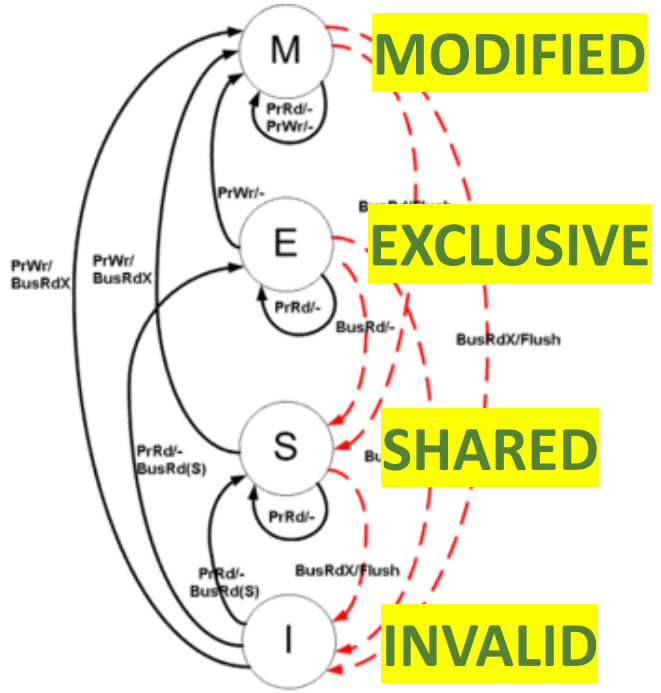

Cache Coherence Action Zone II





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P2

```
// (straw-person lock impl)
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```
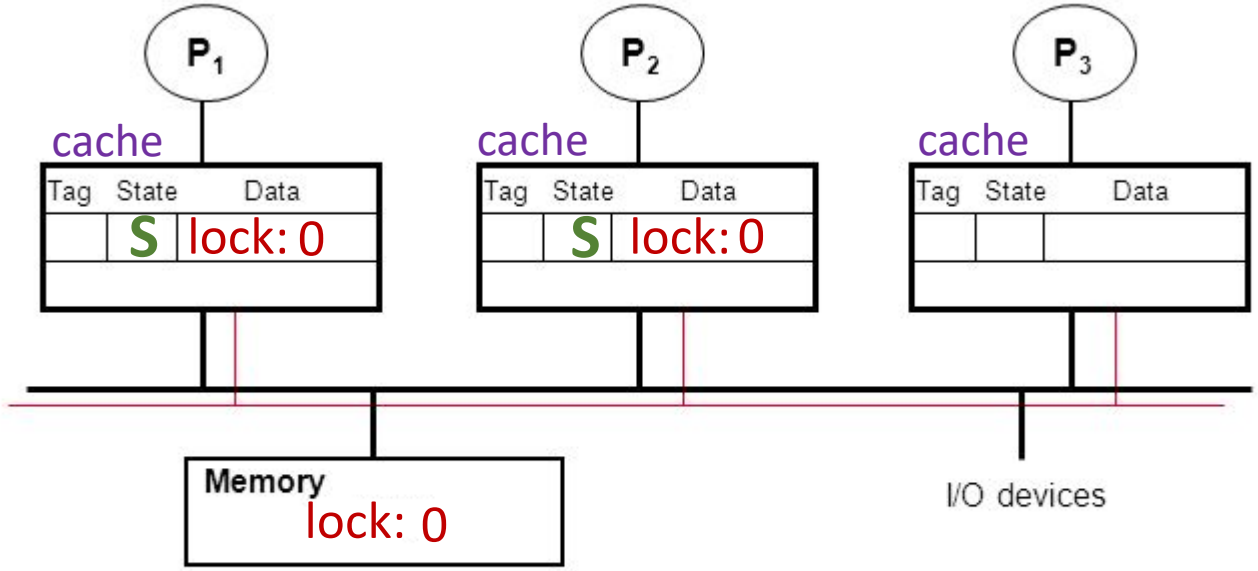
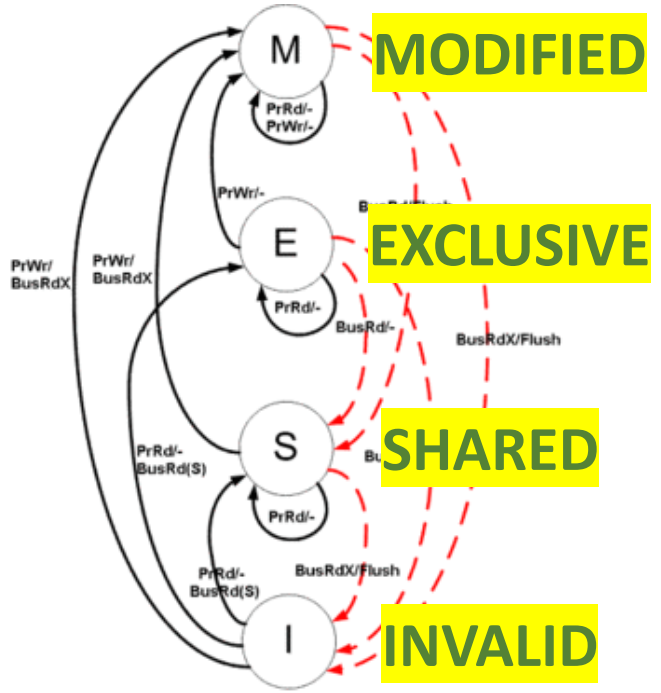

Cache Coherence Action Zone II





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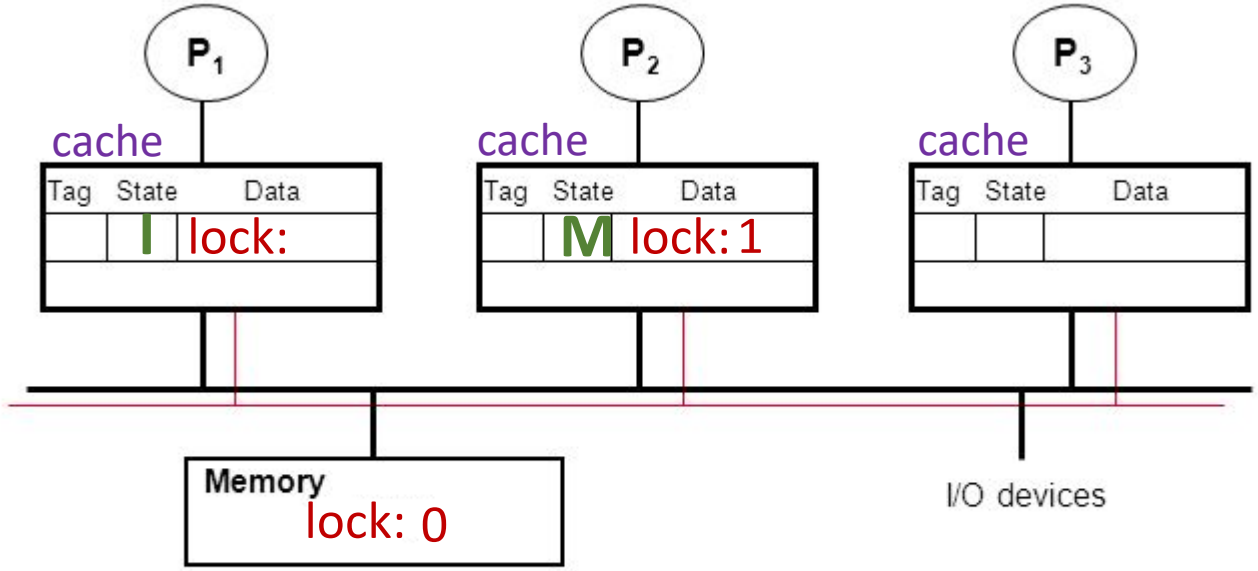
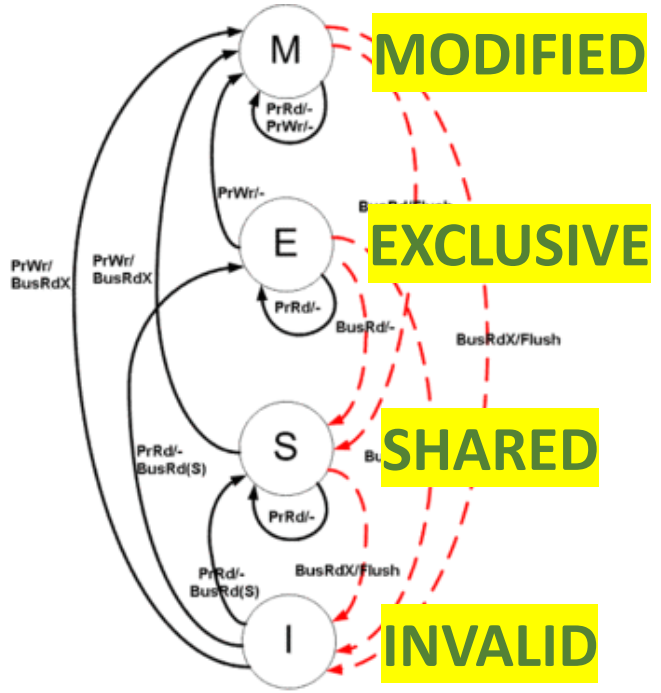
Cache Coherence Action Zone II





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        bnz try
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```

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}
```
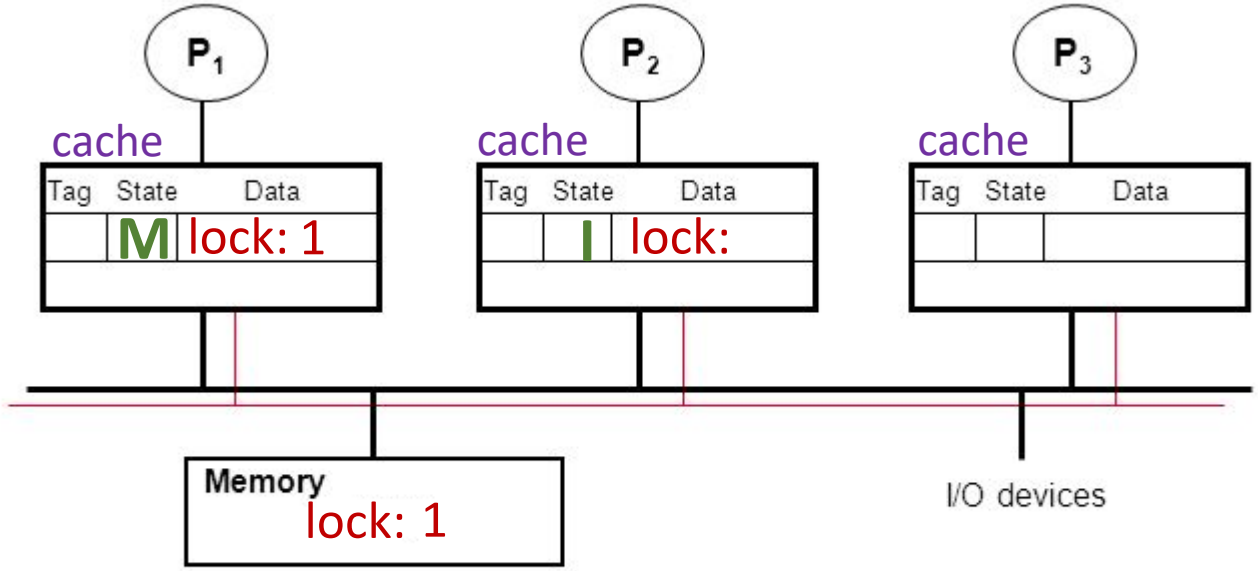
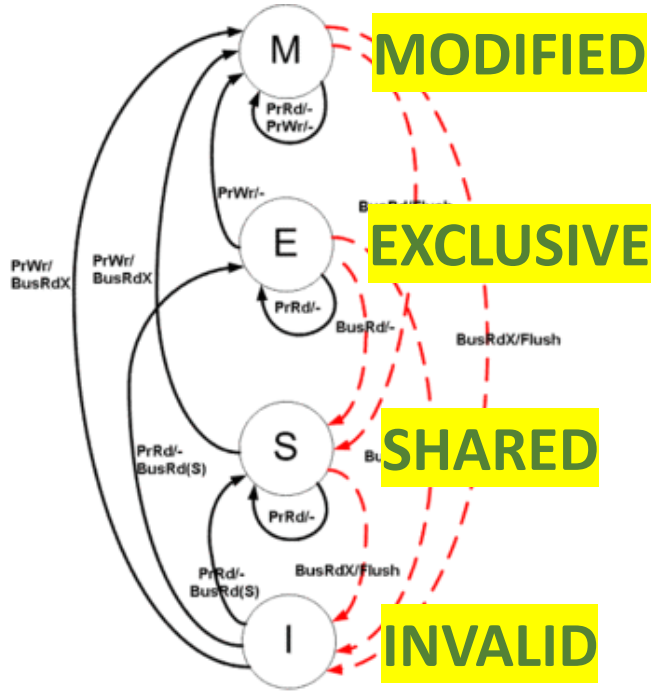

Cache Coherence Action Zone II





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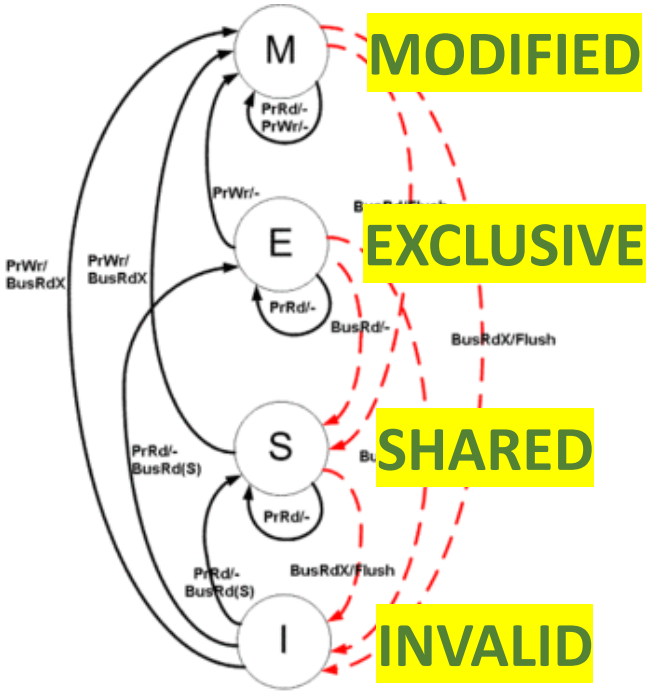
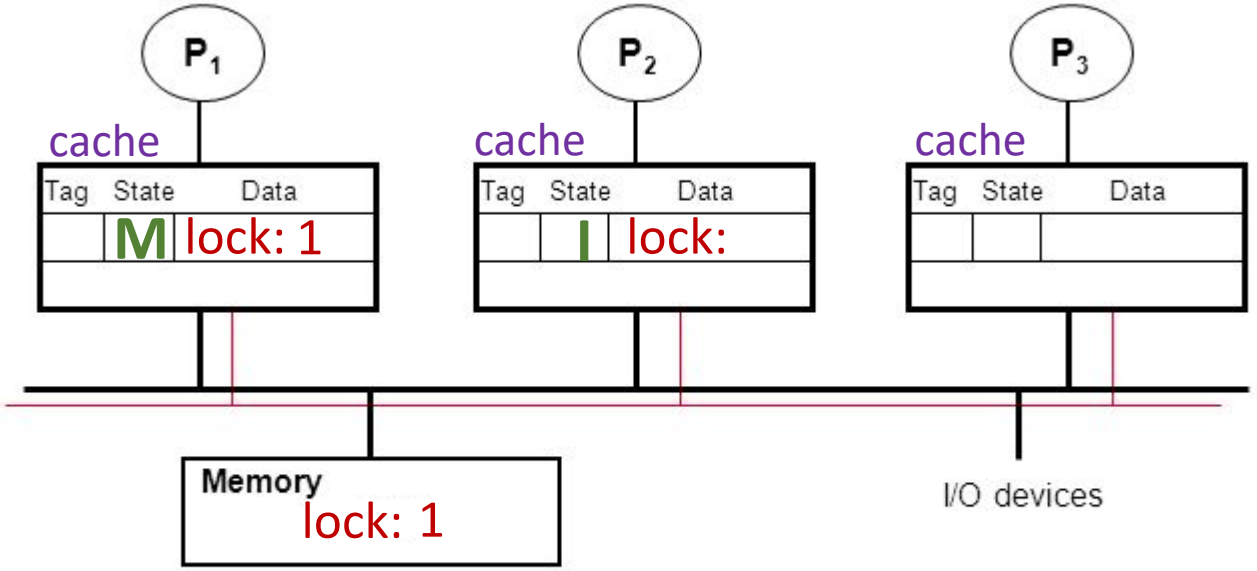
Cache Coherence Action Zone II



NOT SAFE!



P1

P2

```
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        bnz try
        store lock, 1
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// (straw-person lock impl)
// Initially, lock == 0 (unheld)
lock() {
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        store lock, 1
}
```
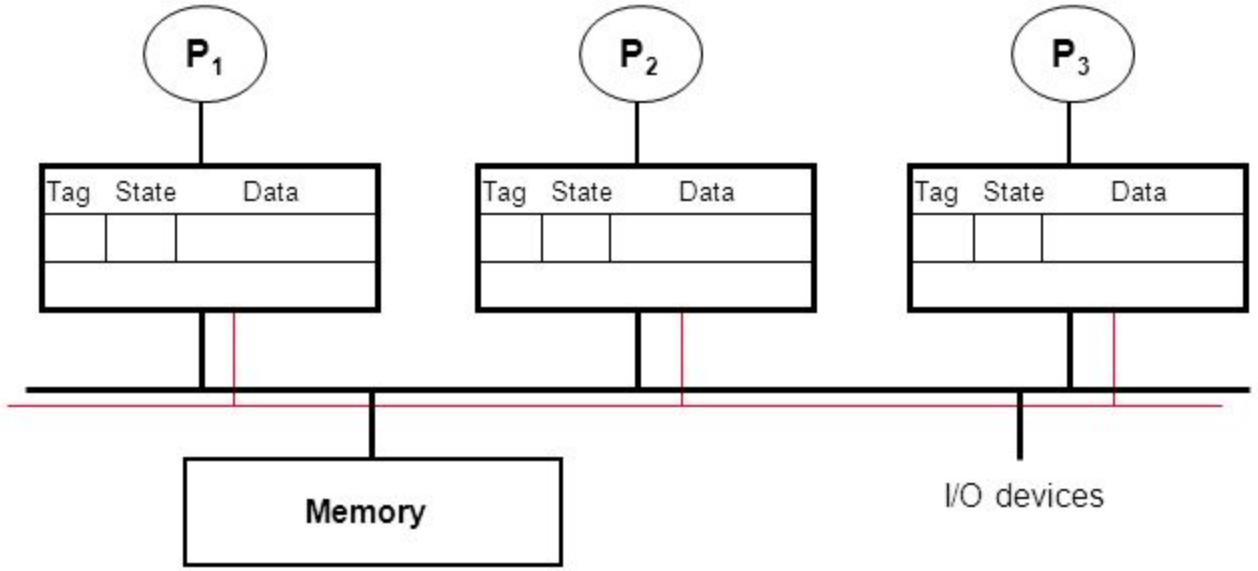

Read-Modify-Write (RMW)

- Implementing locks requires read-modify-write operations
- Required effect is:
  - An atomic and isolated action
    1. read memory location **AND**
    2. write a new value to the location
  - RMW is *very tricky* in multi-processors
  - Cache coherence alone doesn't solve it

```
// (straw-person lock impl)
// Initially, lock == 0 (unheld)
lock() {
try:  load lock, R0
      test R0
      bnz try
      store lock, 1
}
```



Essence of HW-supported RMW

```
// (straw-person lock impl)
// Initially, lock == 0 (unheld)
lock() {
try:  load lock, R0
      test R0
      bnz try
      store lock, 1
}
```

Make this into a single
(atomic hardware instruction)

HW Support for Read-Modify-Write (RMW)

Test & Set	CAS	Exchange, locked increment/decrement,	LLSC: load-linked store-conditional
Most architectures	Many architectures	x86	PPC, Alpha, MIPS

```
int TST(addr) {
  atomic {
    ret = *addr;
    if(!*addr)
      *addr = 1;
    return ret;
  }
}
```

```
bool cas(addr, old, new) {
  atomic {
    if(*addr == old) {
      *addr = new;
      return true;
    }
    return false;
  }
}
```

```
int XCHG(addr, val) {
  atomic {
    ret = *addr;
    *addr = val;
    return ret;
  }
}
```

```
bool LLSC(addr, val) {
 ret = *addr;
 atomic {
   if(*addr == ret) {
     *addr = val;
     return true;
  }
  return false;
}
```

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bool cas(addr, old, new) {
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      return true;
    }
    return false;
  }
}
```

```
int XCHG(addr, val) {
  atomic {
    ret = *addr;
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```
bool LLSC(addr, val) {
 ret = *addr;
 atomic {
   if(*addr == ret) {
     *addr = val;
     return true;
  }
  return false;
}
```

```
void CAS_lock(lock) {
  while(CAS(&lock, 0, 1) != true);
}
```

HW Support for Read-Modify-Write (RMW)

Test & Set	CAS	Exchange, locked increment/decrement,	LLSC: load-linked store-conditional
Most architectures	Many architectures	x86	PPC, Alpha, MIPS

```
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```
bool cas(addr, old, new) {
  atomic {
    if(*addr == old) {
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      return true;
    }
    return false;
  }
}
```

```
int XCHG(addr, val) {
  atomic {
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HW Support for RMW: LL-SC

LLSC: load-linked store-conditional

PPC, Alpha, MIPS

```
bool LLSC(addr, val) {
 ret = *addr;
 atomic {
   if(*addr == ret) {
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}
```

- load-linked is a load that is “linked” to a subsequent store-conditional
- Store-conditional only succeeds if value from linked-load is unchanged

HW Support for RMW: LL-SC

LLSC: load-linked store-conditional

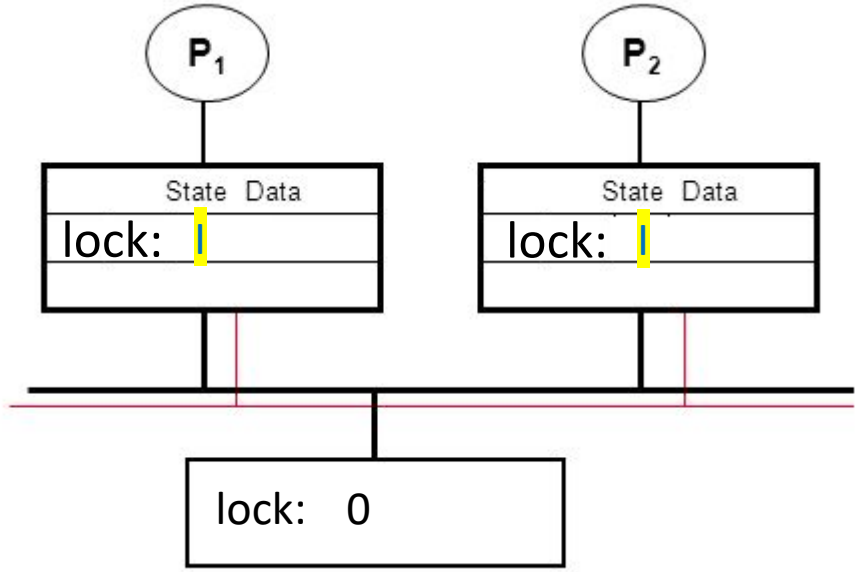
PPC, Alpha, MIPS

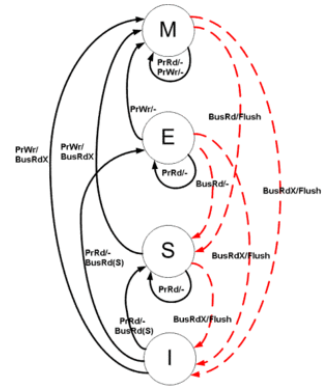
```
bool LLSC(addr, val) {
 ret = *addr;
 atomic {
   if(*addr == ret) {
     *addr = val;
     return true;
  }
  return false;
}
```

```
void LLSC_lock(lock) {
  while(1) {
    old = load-linked(lock);
    if(old == 0 && store-cond(lock, 1))
      return;
  }
}
```

- load-linked is a load that is “linked” to a subsequent store-conditional
- Store-conditional only succeeds if value from linked-load is unchanged

LLSC Lock Action Zone

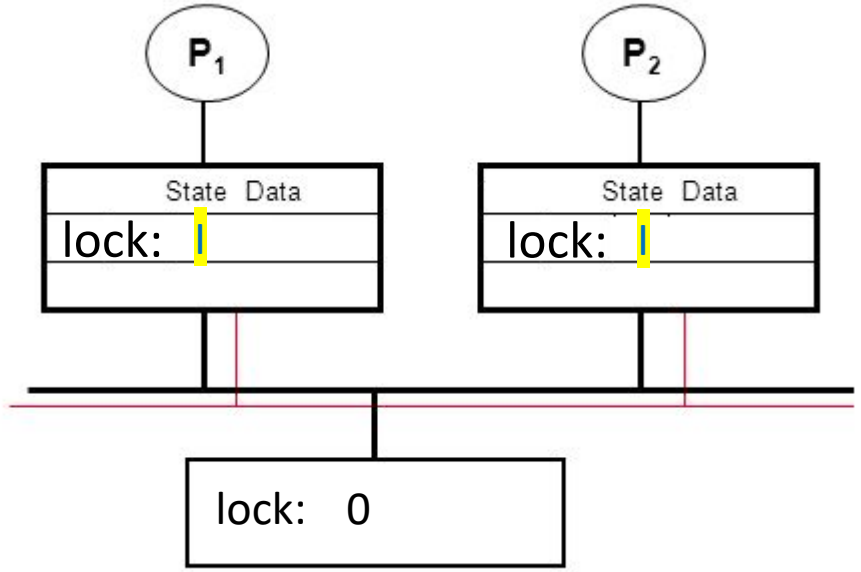


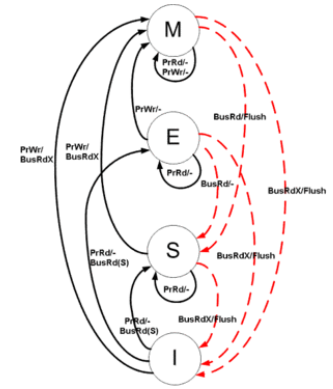



```
_____P1_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

```
_____P2_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

LLSC Lock Action Zone






```
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lock(lock) {
  while(1) {
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      if(sc(lock, 1))
        return;
  }
}
```

```
_______P2_____________
lock(lock) {
  while(1) {
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    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```
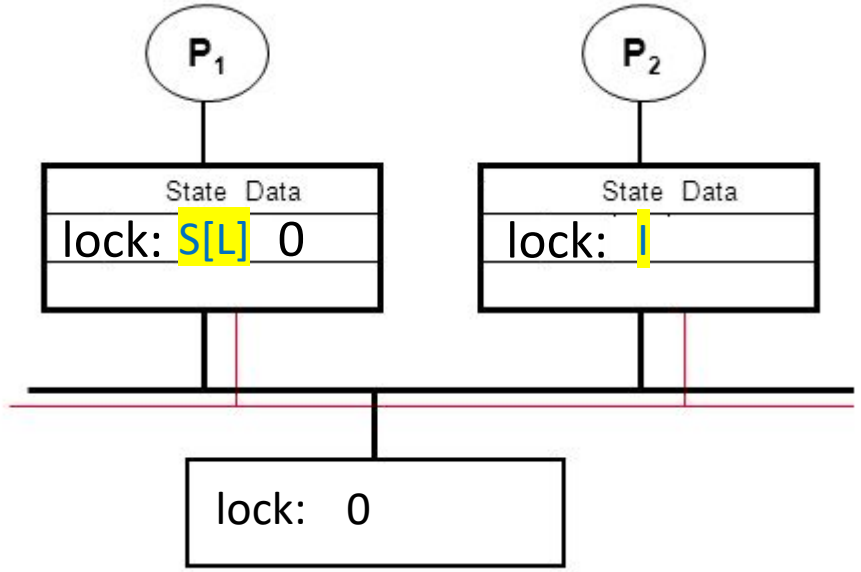
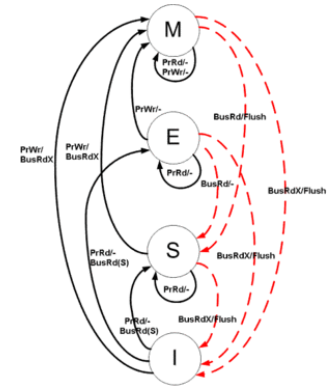

LLSC Lock Action Zone



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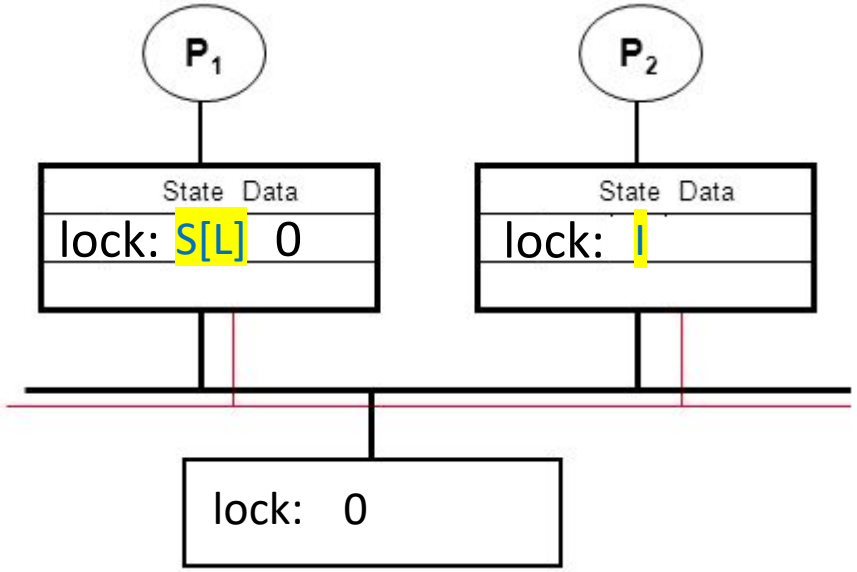
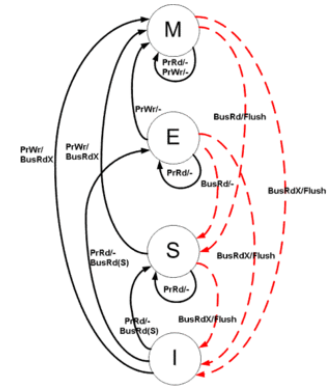
```

LLSC Lock Action Zone



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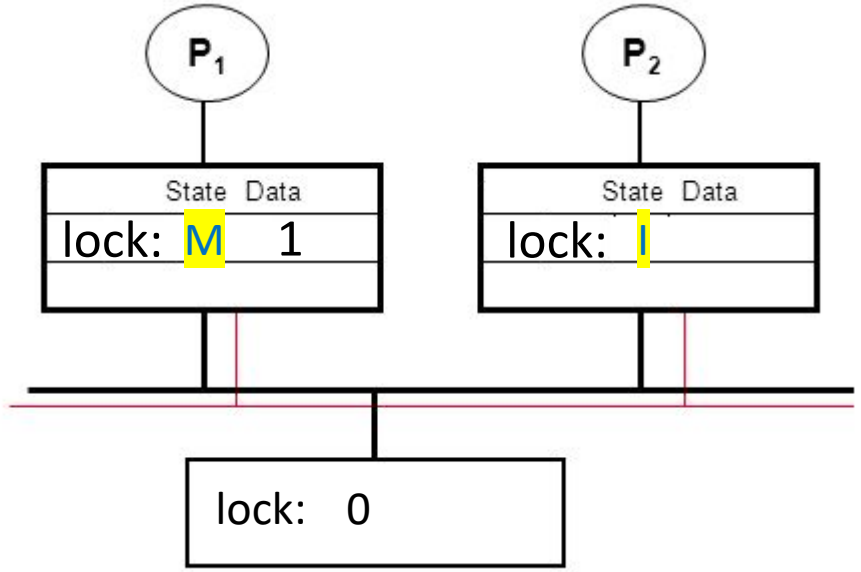
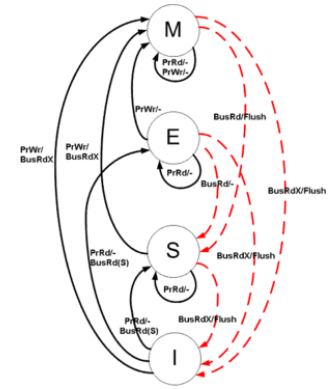
LLSC Lock Action Zone



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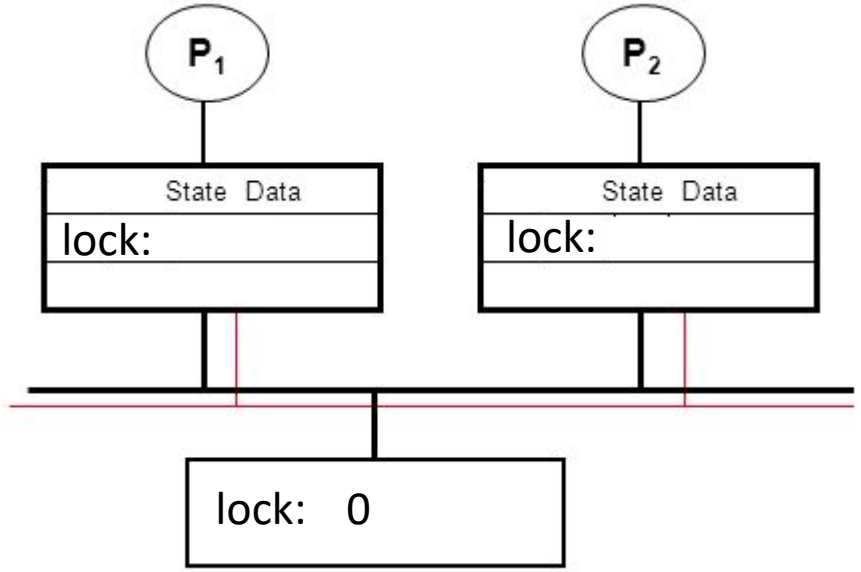

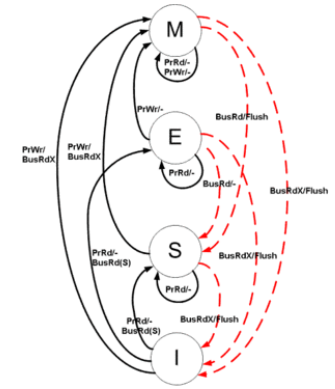


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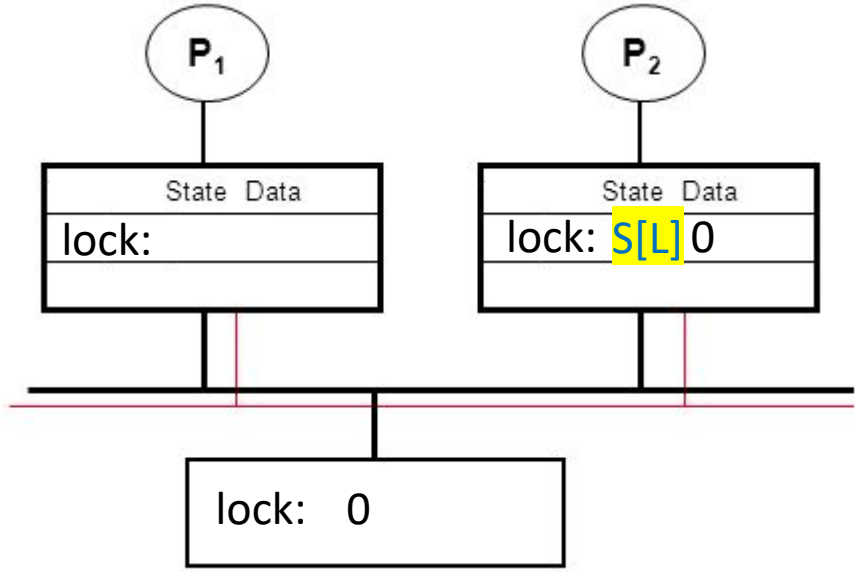
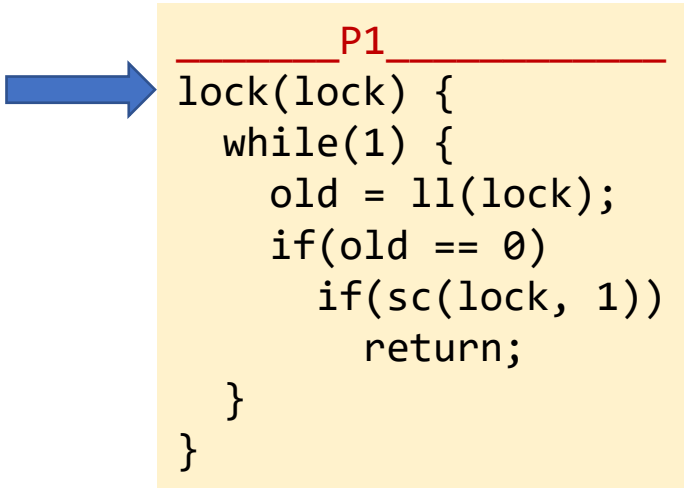
LLSC Lock Action Zone II





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```
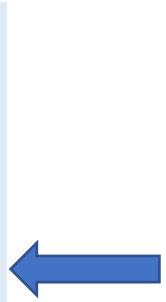
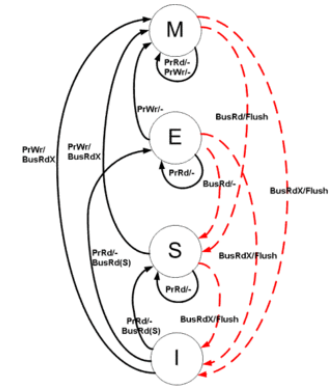
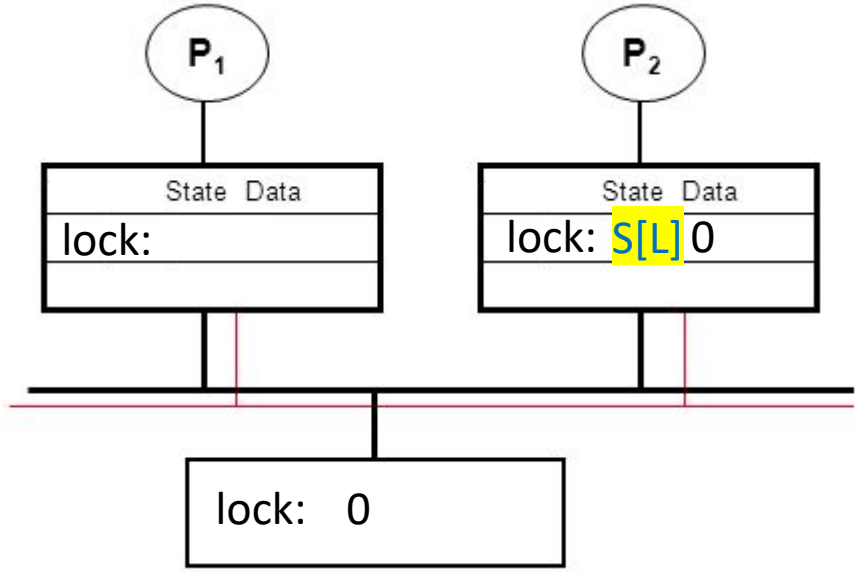
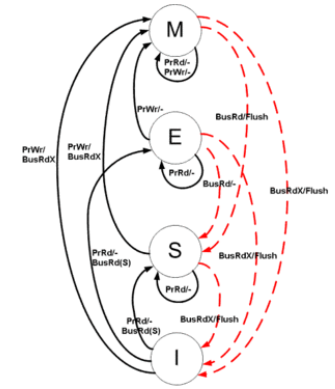





LLSC Lock Action Zone II

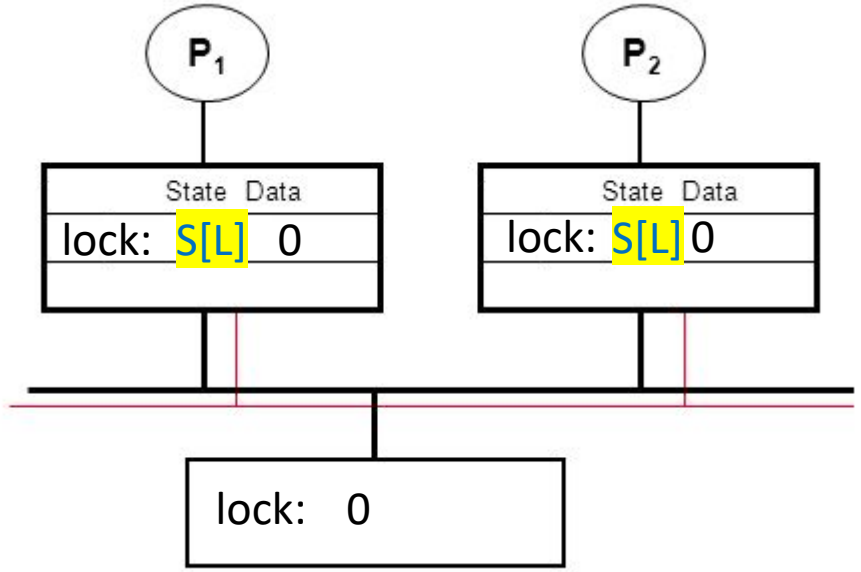


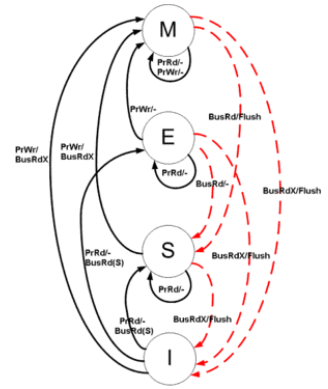


```
_____P1_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

```
_____P2_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

LLSC Lock Action Zone II

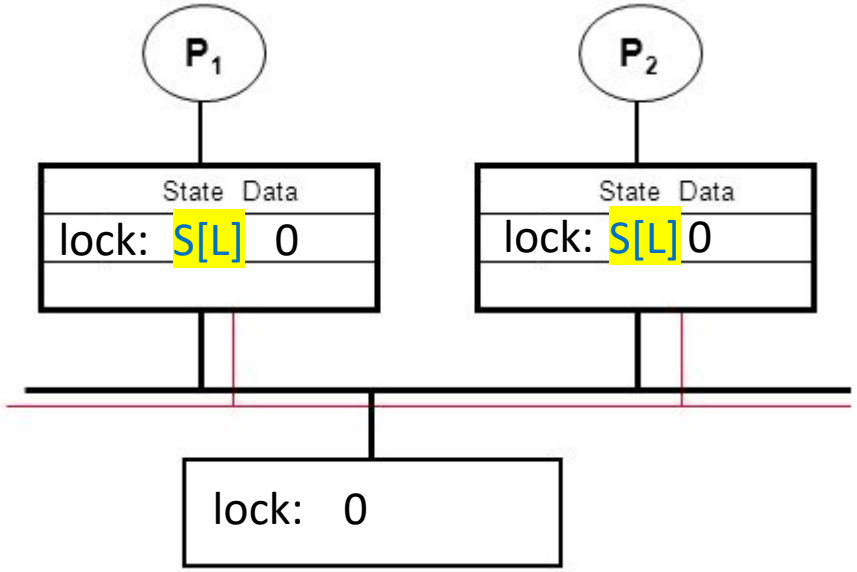


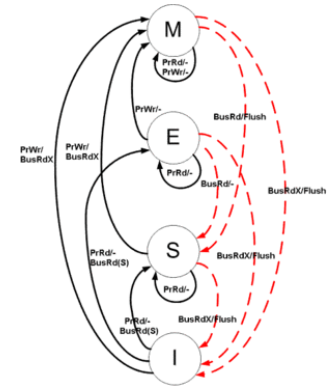



```
_____P1_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

```
_____P2_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

LLSC Lock Action Zone II

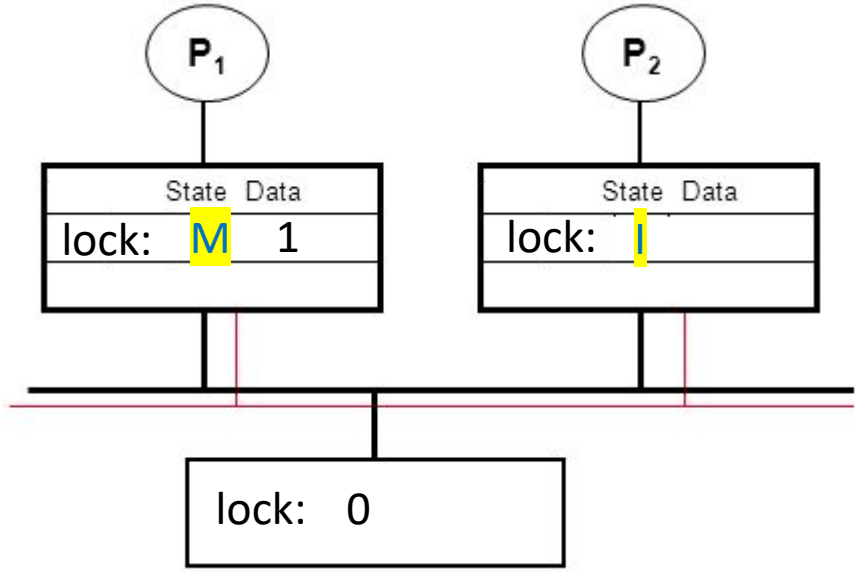


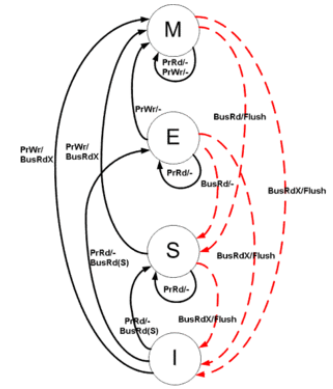



```
_____P1_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

```
_____P2_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

LLSC Lock Action Zone II

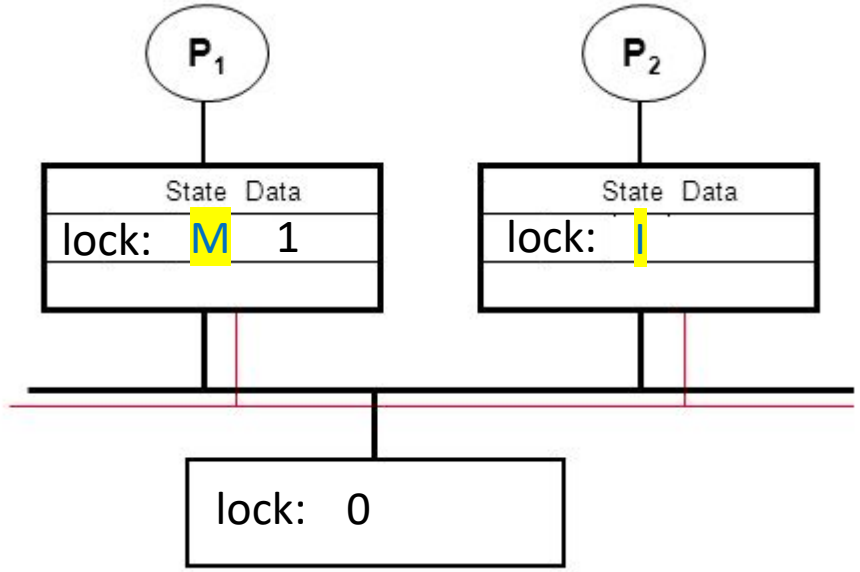


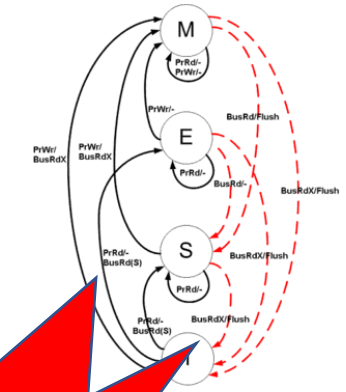



```
_____P1_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

```
_____P2_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

LLSC Lock Action Zone II





Store conditional fails

```
_____P1_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```

```
_____P2_____
lock(lock) {
  while(1) {
    old = ll(lock);
    if(old == 0)
      if(sc(lock, 1))
        return;
  }
}
```