Consistency
Transactions
Transactional Memory

Chris Rossbach

cs378h

Outline for Today

- Questions?
- Administrivia
  - Comments on Lab 2 due date
  - Comments on the changes to schedule
- Agenda
  - Consistency
  - Transactions
  - Transactional Memory

- Acks: Yoav Cohen for some STM slides

Faux Quiz questions

- How are promises and futures related? Since there is disagreement on the nomenclature, don’t worry about which is which—just describe what the different objects are and how they function.
- How does HTM resemble or differ from Load-linked Stored-Conditional?
- What are some pros and cons of HTM vs STM?
- What is Open Nesting? Closed Nesting? Flat Nesting?
- How does 2PL differ from 2PC?
- Define ACID properties: which, if any, of these properties does TM relax?

Memory Consistency

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- Formal specification of memory semantics
  - Statement of how shared memory will behave with multiple CPUs
  - Ordering of reads and writes

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- Memory Consistency != Cache Coherence
  - Coherence: propagate updates to cached copies
    - Invalidate vs. Update
  - Coherence vs. Consistency?
    - **Coherence:** ordering of ops. at a single location
    - **Consistency:** ordering of ops. at multiple locations

Sequential Consistency

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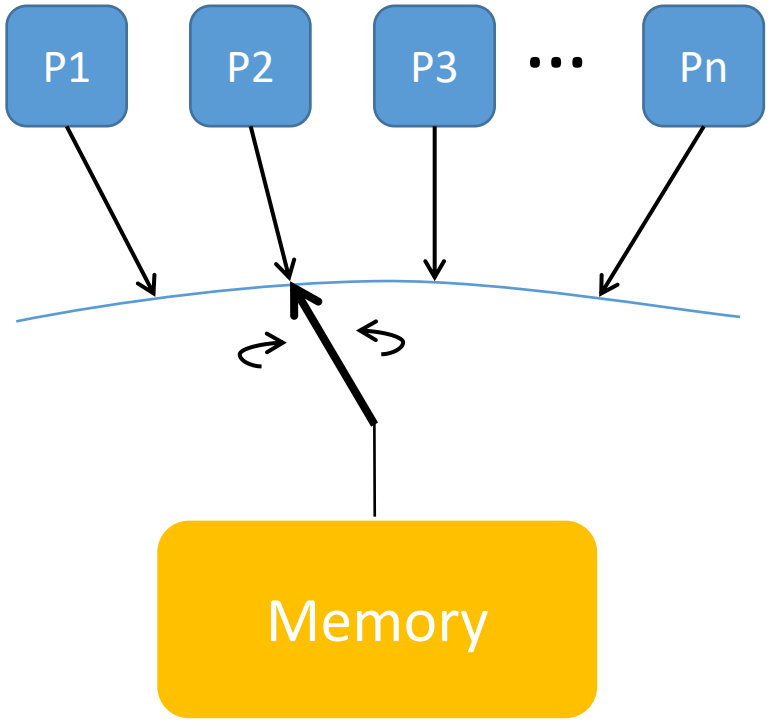

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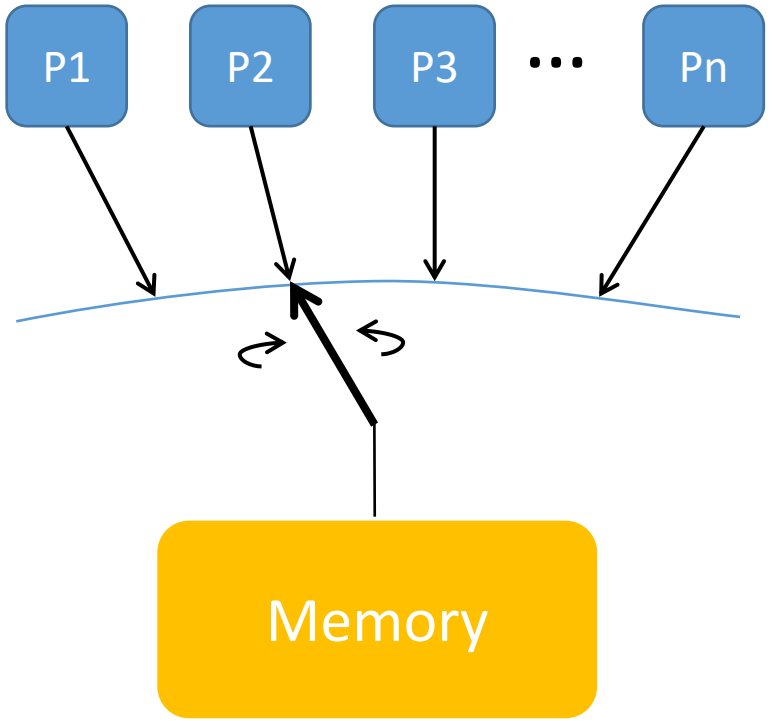
- Result of *any* execution is same as if all operations execute on a uniprocessor



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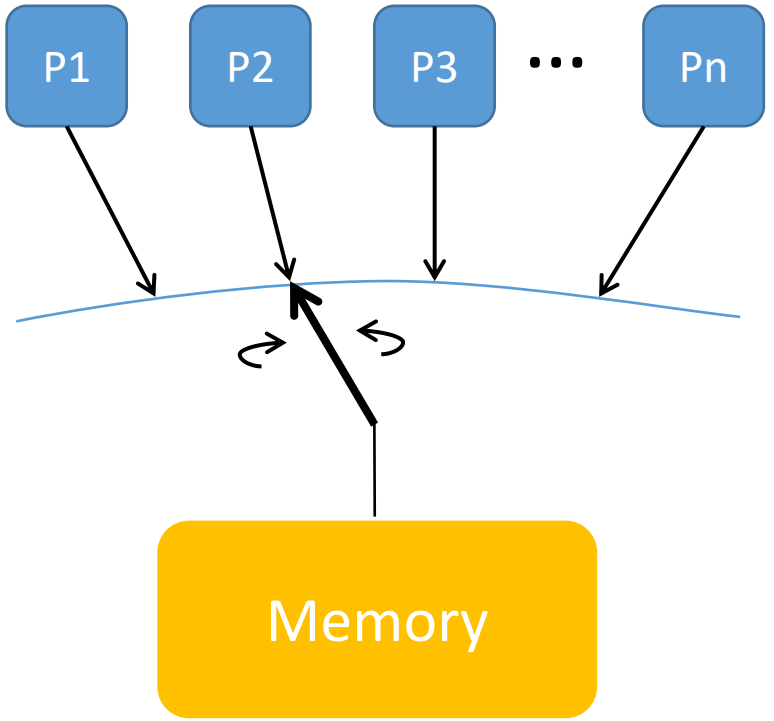
- Operations on each processor are *totally ordered* in the sequence and respect program order for each processor



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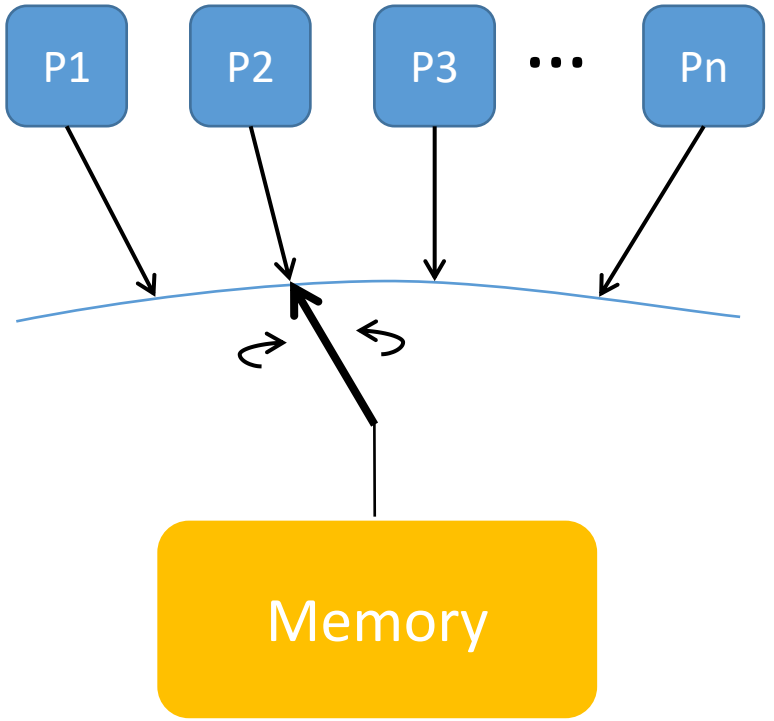

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- Memory operations occur:
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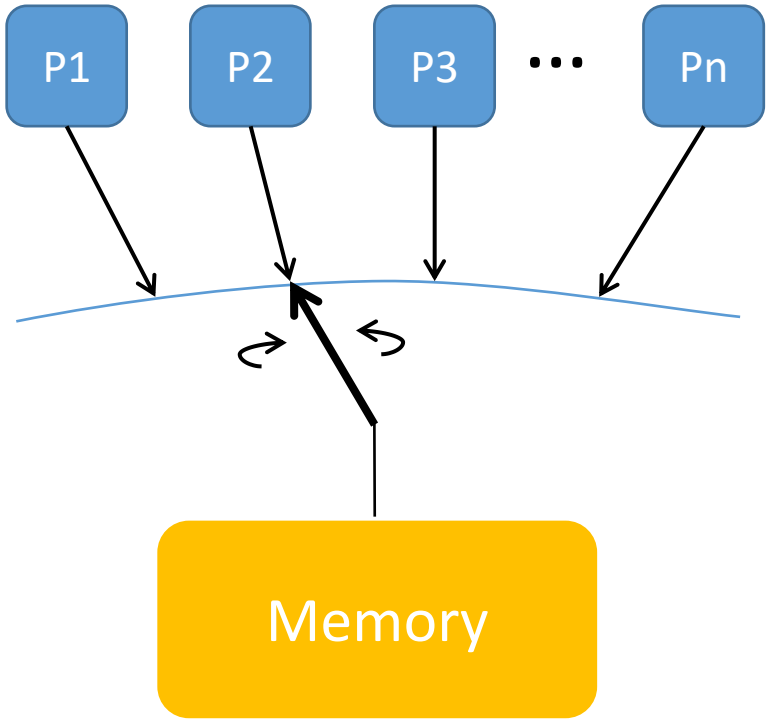

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- Memory operations occur:
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- How is this different from coherence?
- Why do modern CPUs not implement SC?
- Requirements: ***program order, write atomicity***

Sequential Consistency

- All operations are executed in *some* sequential order
- each process issues operations in program order
  - *Any* valid interleaving is allowed
  - All *agree* on the same interleaving
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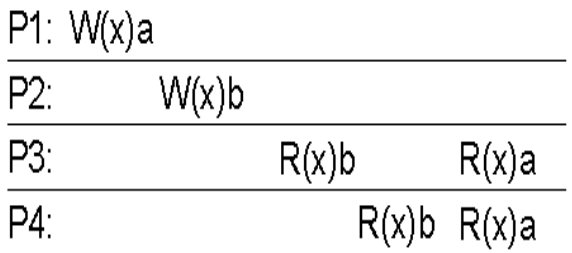

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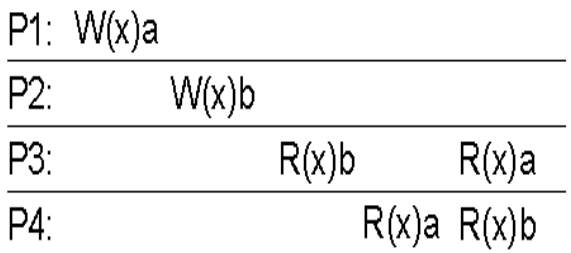

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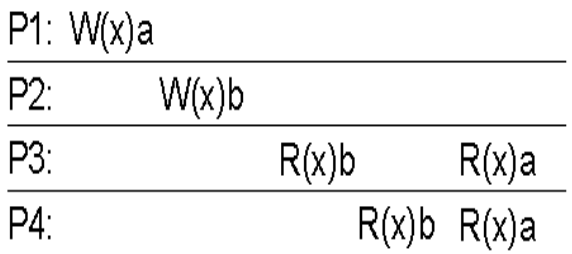

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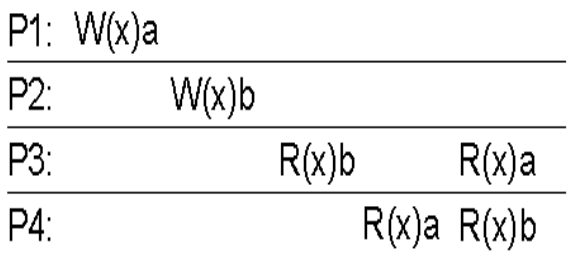

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Are either of these SC?

Sequential Consistency: Canonical Example

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Initially, Flag1 = Flag2 = 0
```

P1

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Flag1 = 1
if (Flag2 == 0)
  enter CS
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Can both P1 and P2 wind up in the critical section at the same time?

Do we need Sequential Consistency?

Initially, Flag1 = Flag2 = 0

P1	**P2**
Flag1 = 1	
	Flag2 = 1
	if (Flag1 == 0)
	shared_data++
if (Flag2 == 0)	
shared_data++	

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- P1 and P2 may not see each other's writes in the same order
- Implication: both in critical section, which is incorrect
- Why would this happen?

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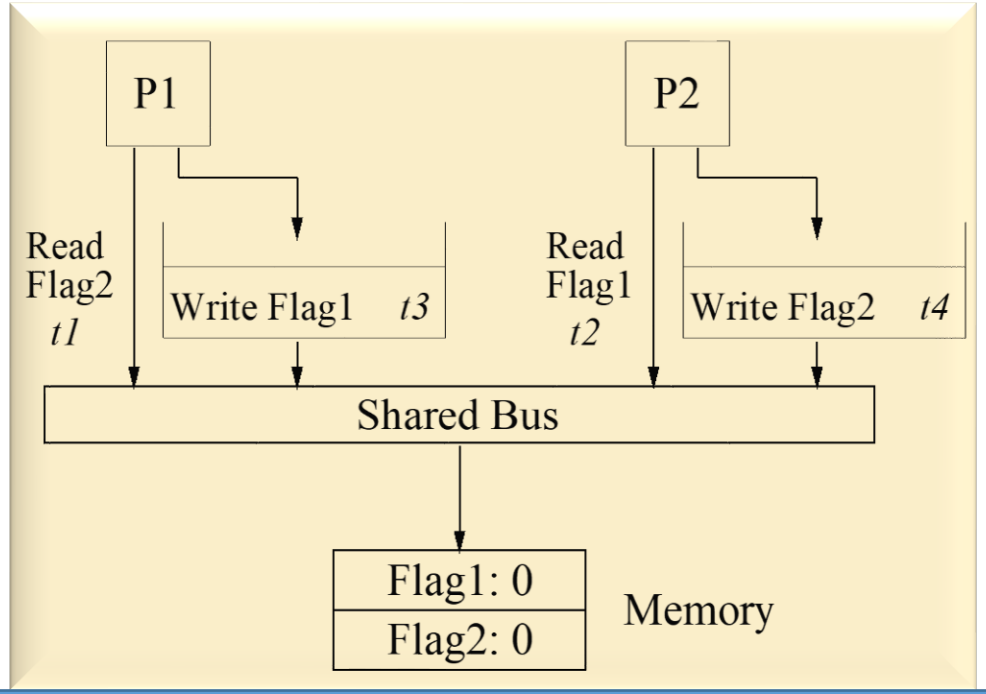

Write Buffers

- P_0 write → queue op in write buffer, proceed
- P_0 read → look in write buffer,
- P_(x != 0) read → old value: write buffer hasn't drained

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Disadvantages:

- Difficult to implement!
  - Coherence to (e.g.) write buffers is hard
- Sacrifices many potential optimizations
  - Hardware (cache) and software (compiler)
  - Major performance hit

Relaxed Consistency Models

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IBM 370 [14]	√					serialization instructions
TSO [20]	√				√	RMW
PC [13, 12]	√			√	√	RMW
PSO [20]	√	√			√	RMW, STBAR
WO [5]	√	√	√		√	synchronization
RCsc [13, 12]	√	√	√		√	release, acquire, nsync, RMW
RCpc [13, 12]	√	√	√	√	√	release, acquire, nsync, RMW
Alpha [19]	√	√	√		√	MB, WMB
RMO [21]	√	√	√		√	various MEMBAR's
PowerPC [17, 4]	√	√	√	√	√	SYNC

Relaxed Consis

```
static inline void arch_write_lock(arch_rwlock_t *rw) {
   asm volatile(LOCK_PREFIX WRITE_LOCK_SUB(%1) "(%0)\n\t"
        "jz 1f\n"
         "call __write_lock_failed\n\t"
        "1:\n"
        ::LOCK_PTR_REG (&rw->write), "i" (RW_LOCK_BIAS) : "memory"); }
```

x86

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```
static inline unsigned long
__arch_spin_trylock(arch_spinlock_t *lock)
{
  unsigned long tmp, token;
  token = LOCK_TOKEN;
  __asm__ __volatile__(
    "1: "  PPC_LWARX(%0,0,%2,1) "\n\
           cmpwi 0,%0,0\n\
           bne- 2f\n\
           stwcx. %1,0,%2\n\
           bne- 1b\n"
           PPC_ACQUIRE_BARRIER
    "2:“ : "=&r" (tmp)
         : "r" (token), "r" (&lock->slock)
         : "cr0", "memory");
    return tmp;
}
```

PowerPC

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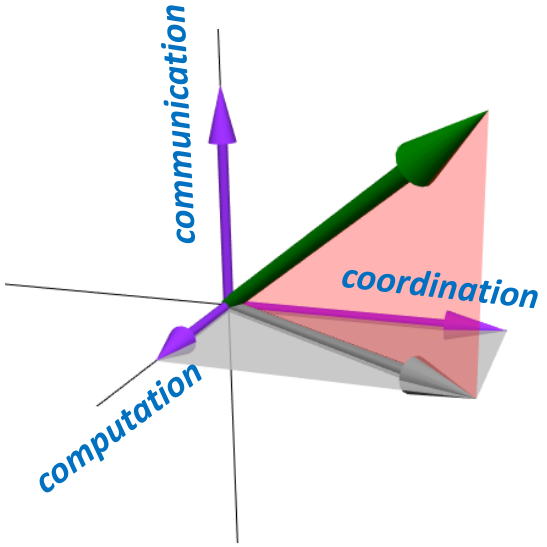

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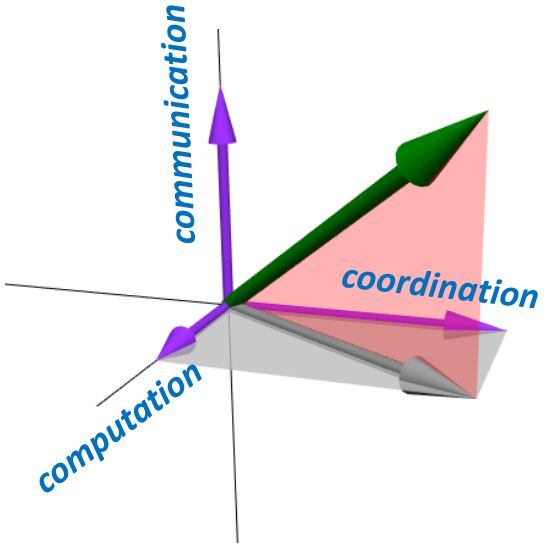

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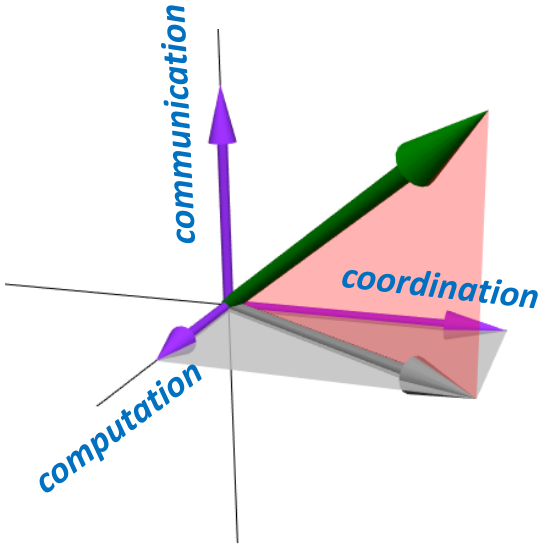
  - *Mostly about how to deal with shared state*



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Core issue: multiple updates

Canonical examples:

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   delete(file, old-dir)
   add(file, new-dir)
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Problems: crash in the middle / visibility of intermediate state

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No.
Not even if all messages get through!

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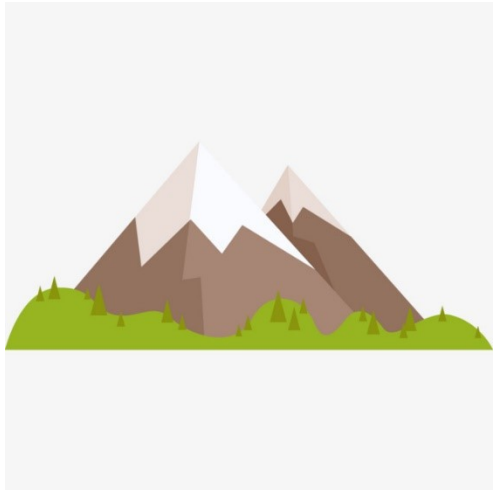

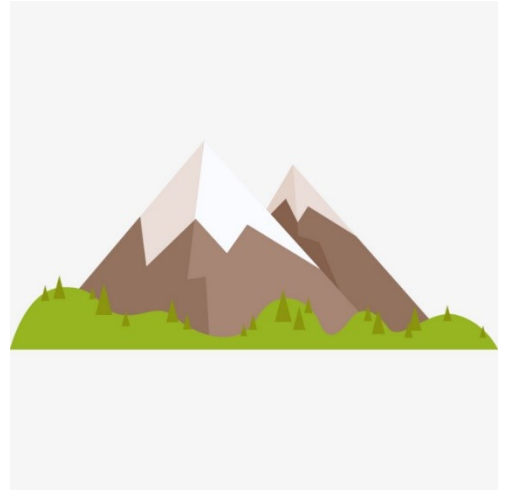

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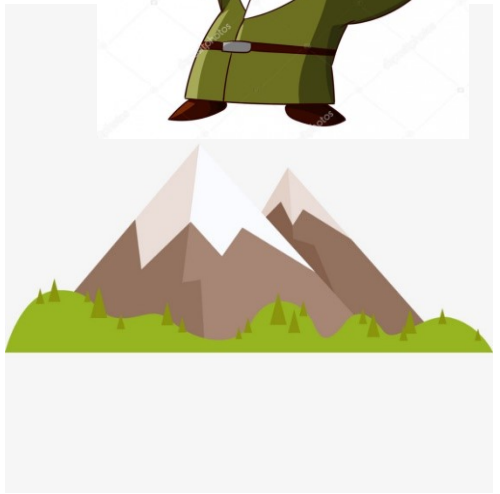

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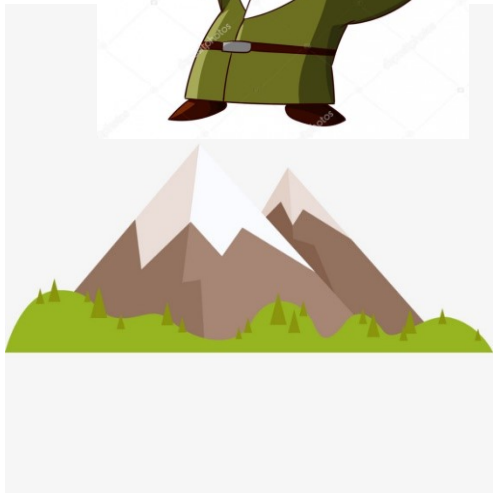

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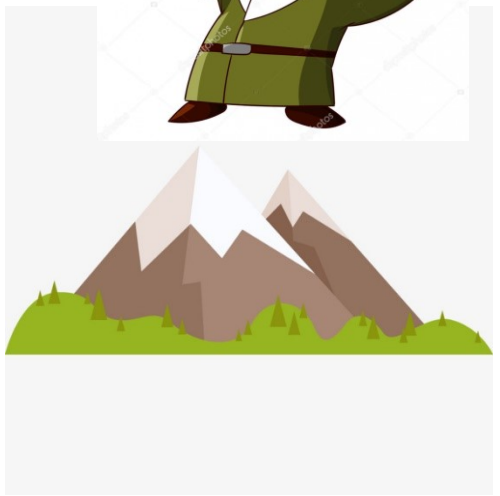
General A → General B: Check. Dawn it is.
General B → General A: Alright already—dawn.

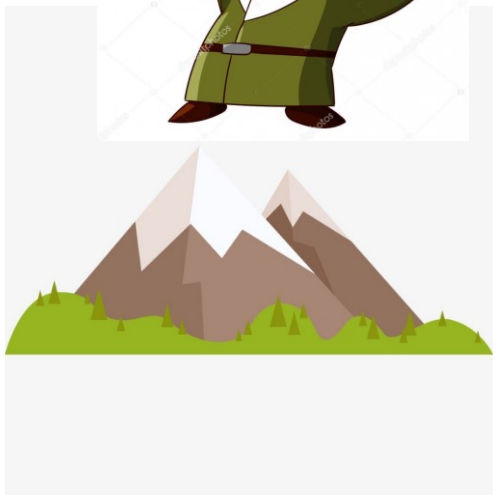


General's paradox

- Two generals on separate mountains
- Can only communicate via messengers
- Messengers can get lost or captured
- Need to coordinate attack
  - attack at same time good, different times bad!

- Even if all messages delivered, can't assume– maybe some message didn't get through.
- No solution: one of the few CS impossibility results.

General A → General B: let's attack at dawn
General B → General A: OK, dawn.
General A → General B: Check. Dawn it is.
General B → General A: Alright already—dawn.



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- Core idea: one entity has the power to say yes or no for all
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  - Distributed transactions
    - 2 phase commit
    - One machine has final say for all machines
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What is the role of synchronization here?

Transactional Programming Model

```
begin transaction;
    x = read(“x-values”, ....);
    y = read(“y-values”, ....);
    z = x+y;
    write(“z-values”, z, ....);
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What has changed from previous programming models?

ACID Semantics

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What are they?

- A
- C
- I
- D

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ACID Semantics

- Atomic – all updates happen or none do
- Consistent – system invariants maintained across updates
- Isolated – no visibility into partial updates
- Durable – once done, stays done
- Are subsets ever appropriate?
  - When would ACI be useful?
  - ACD?
  - Isolation only?

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  - Optimistic Concurrency Control
  - Journaling
  - 2,3-phase commit
  - Speculation-rollback
  - Single global lock
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Pros/Cons?

Two-phase locking

- Phase 1: only acquire locks in order
- Phase 2: unlock at commit
- avoids deadlock

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```
BEGIN_TXN() {
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  forall x in rwset
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A: grab locks
A: modify x, y,
A: unlock y, x
B: grab locks
B: update x, y
B: unlock y, x
B: COMMIT
A: CRASH

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unlock y, x
COMMIT_TXN();
```

B commits changes that depend on A's updates

A: grab locks
A: modify x, y,
A: unlock y, x
B: grab locks
B: update x, y
B: unlock y, x
B: COMMIT
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Pros/Cons?

What happens on failures?

Two-phase commit

- N participants agree or don’t (atomicity)
- Phase 1: everyone “prepares”
- Phase 2: Master decides and tells everyone to actually commit
- What if the master crashes in the middle?

2PC: Phase 1

1. Coordinator sends REQUEST to all participants
2. Participants receive request and
3. Execute locally
4. Write VOTE_COMMIT or VOTE_ABORT to local log
5. Send VOTE_COMMIT or VOTE_ABORT to coordinator

Example—move: C→S1: delete foo from /, C→S2: add foo to /

Failure case:
S1 writes rm /foo, VOTE_COMMIT to log
S1 sends VOTE_COMMIT
S2 decides permission problem
S2 writes/sends VOTE_ABORT

Success case:
S1 writes rm /foo, VOTE_COMMIT to log
S1 sends VOTE_COMMIT
S2 writes add foo to /
S2 writes/sends VOTE_COMMIT

2PC: Phase 2

- Case 1: receive VOTE_ABORT or timeout
  - Write GLOBAL_ABORT to log
  - send GLOBAL_ABORT to participants
- Case 2: receive VOTE_COMMIT from all
  - Write GLOBAL_COMMIT to log
  - send GLOBAL_COMMIT to participants
- Participants receive decision, write GLOBAL_* to log

2PC corner cases

Phase 1

1. Coordinator sends REQUEST to all participants
2. X Participants receive request and
3. Execute locally
4. Write VOTE_COMMIT or VOTE_ABORT to local log
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Phase 2

- Y Case 1: receive VOTE_ABORT or timeout
  - Write GLOBAL_ABORT to log
  - send GLOBAL_ABORT to participants
- Case 2: receive VOTE_COMMIT from all
  - W Write GLOBAL_COMMIT to log
  - send GLOBAL_COMMIT to participants
- Z Participants recv decision, write GLOBAL_* to log

- What if participant crashes at X?
- Coordinator crashes at Y?
- Participant crashes at Z?
- Coordinator crashes at W?

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- Coordinator crashes at W, never wakes up
- All nodes block forever!
- Can participants ask each other what happened?
- 2PC: always has risk of indefinite blocking
- Solution: (yes) 3 phase commit!
  - Reliable replacement of crashed “leader”
  - 2PC often good enough in practice

Questions?