Parallel Architectures

Chris Rossbach

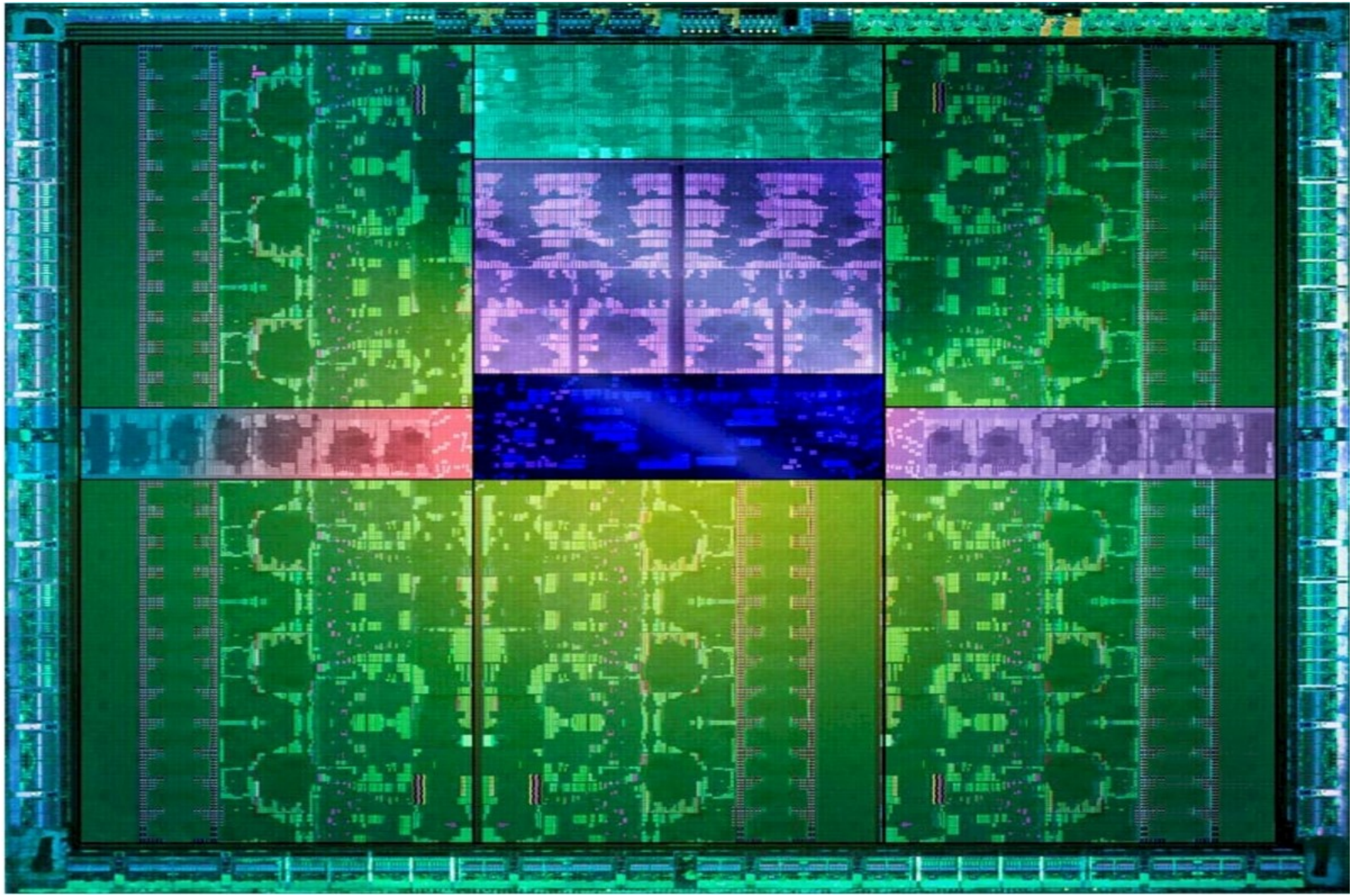
Outline for Today

- Questions?
- Administrivia

- Agenda
  - Parallel Architectures (GPU background)

Faux Quiz questions

- What is hardware multi-threading; what problem does it solve?
- What is the difference between a vector processor and a scalar?
- Implement a parallel scan or reduction
- How are GPU workloads different from GPGPU workloads?
- How does SIMD differ from SIMT?
- List and describe some pros and cons of vector/SIMD architectures.
- GPUs historically have elided cache coherence.Why? What impact does it have on the the programmer?
- List some ways that GPUs use concurrency but not necessarily parallelism.



A modern GPU: Volta V100

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  - Streaming Multiprocessor

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Also:
CU or *ACE*

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Roughly: all of pfxsum 1,000s X/sec

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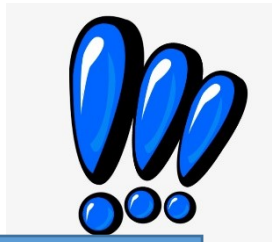

How do you program a machine like this? pthread_create()?

GPUs: Outline

- Background from many areas
  - Architecture
    - Vector processors
    - Hardware multi-threading
  - Graphics
    - Graphics pipeline
    - Graphics programming models
  - Algorithms
    - parallel architectures → parallel algorithms
- Programming GPUs
  - CUDA
  - Basics: getting something working
  - Advanced: making it perform

Architecture Review: Pipelines

Processor algorithm:

```
main() {
  while(true)
    do_next_instruction();
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}
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Architecture Review: Pipelines

Processor algorithm:

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main() {
  v
}

do_n
  inst
  ops
  exe
  access_memory(ops, regs);
  write_back(regs);
}
```

```
main() {
  pthread_create(do_instructions);
  pthread_create(do_decode);
  pthread_create(do_execute);
  …
  pthread_join(…);
  …
}
```

Architecture Review: Pipelines

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  …
  pthread_join(…);
  …
}
```

```
do_instructions() {
  while(true) {
    instruction = fetch();
    enqueue(DECODE, instruction);
}}
```

```
do_decode() {
  while(true) {
    instruction = dequeue();
    ops, regs = decode(instruction);
    enqueue(EX, instruction);
}}
```

```
do_execute() {
  while(true) {
    instruction = dequeue();
    execute_calc_addrs(ops, regs);
    enqueue(MEM, instruction);
}}
```

….

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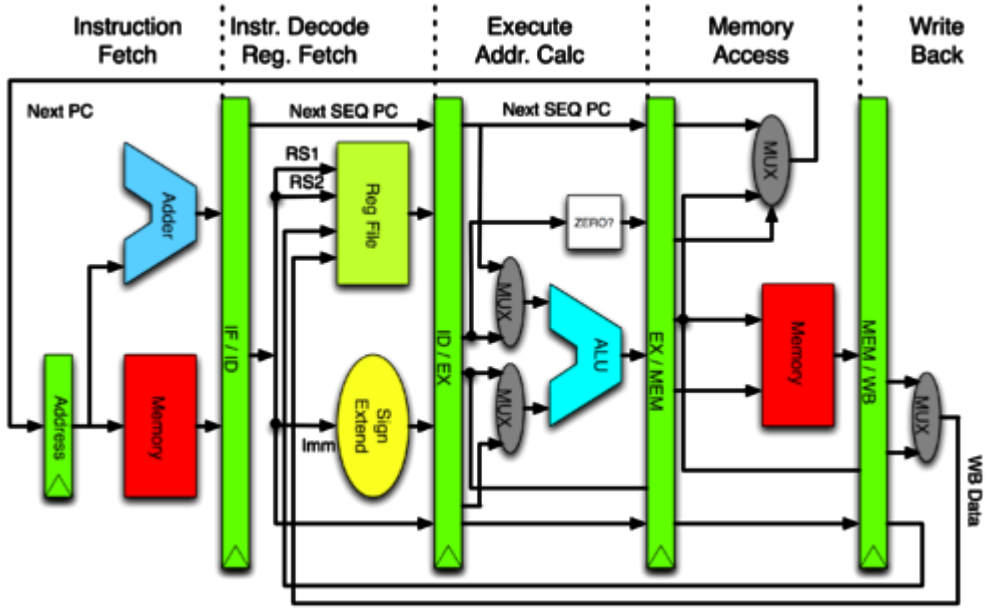


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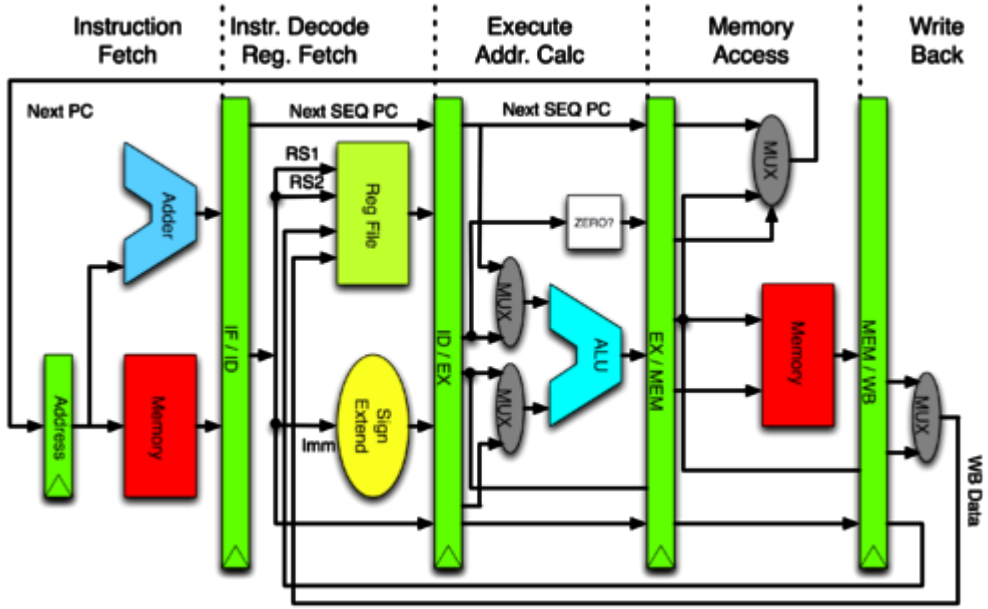


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3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

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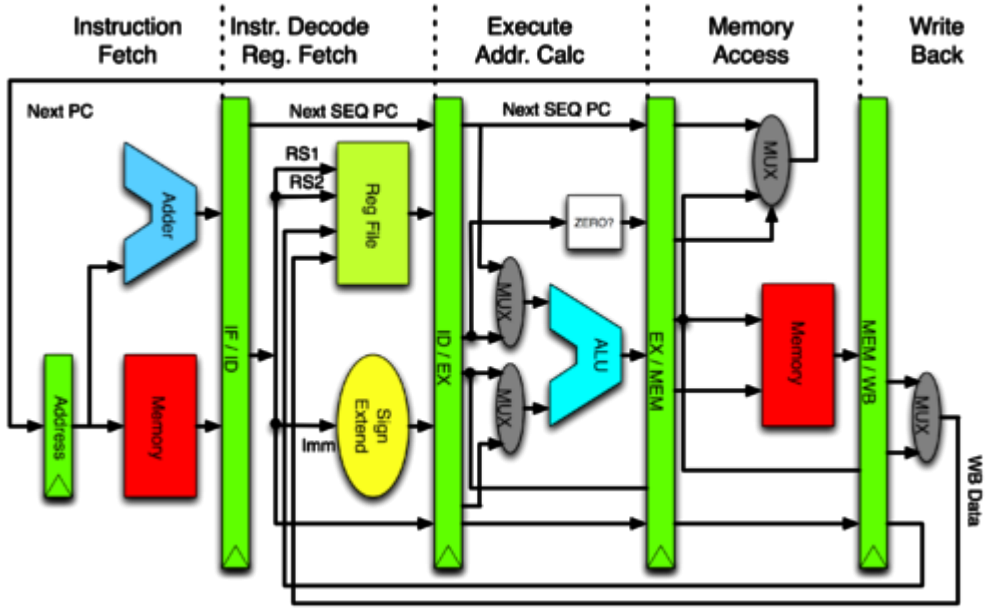


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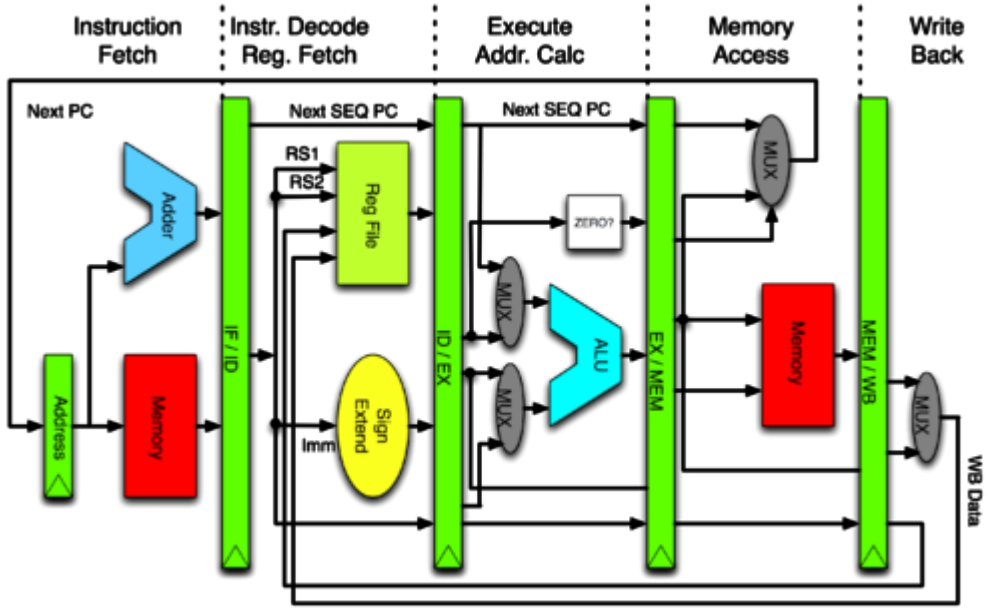


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Works well if pipeline is kept full
What kinds of things cause "bubbles"/stalls?

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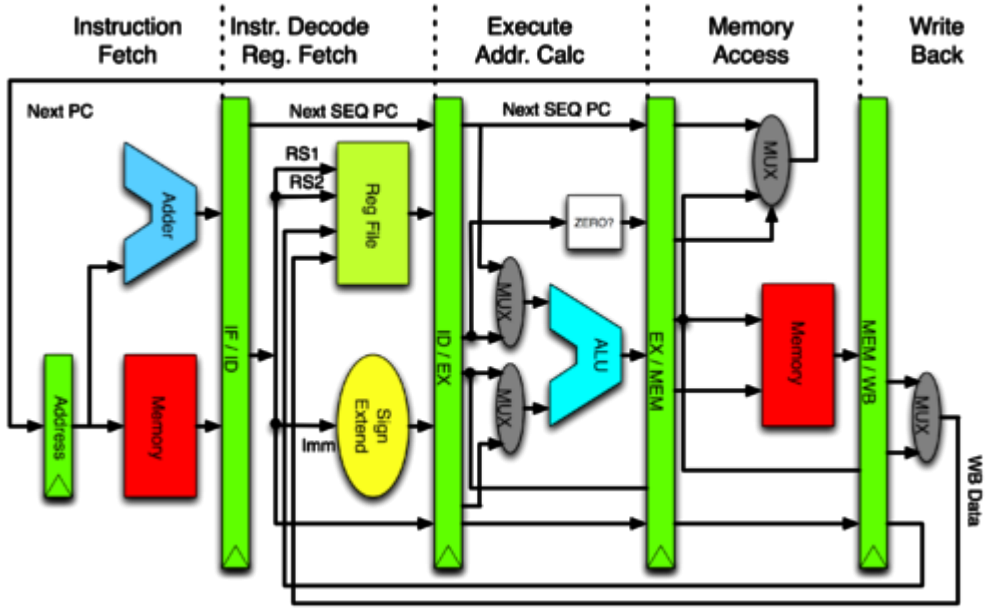


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How can we get *more* parallelism?

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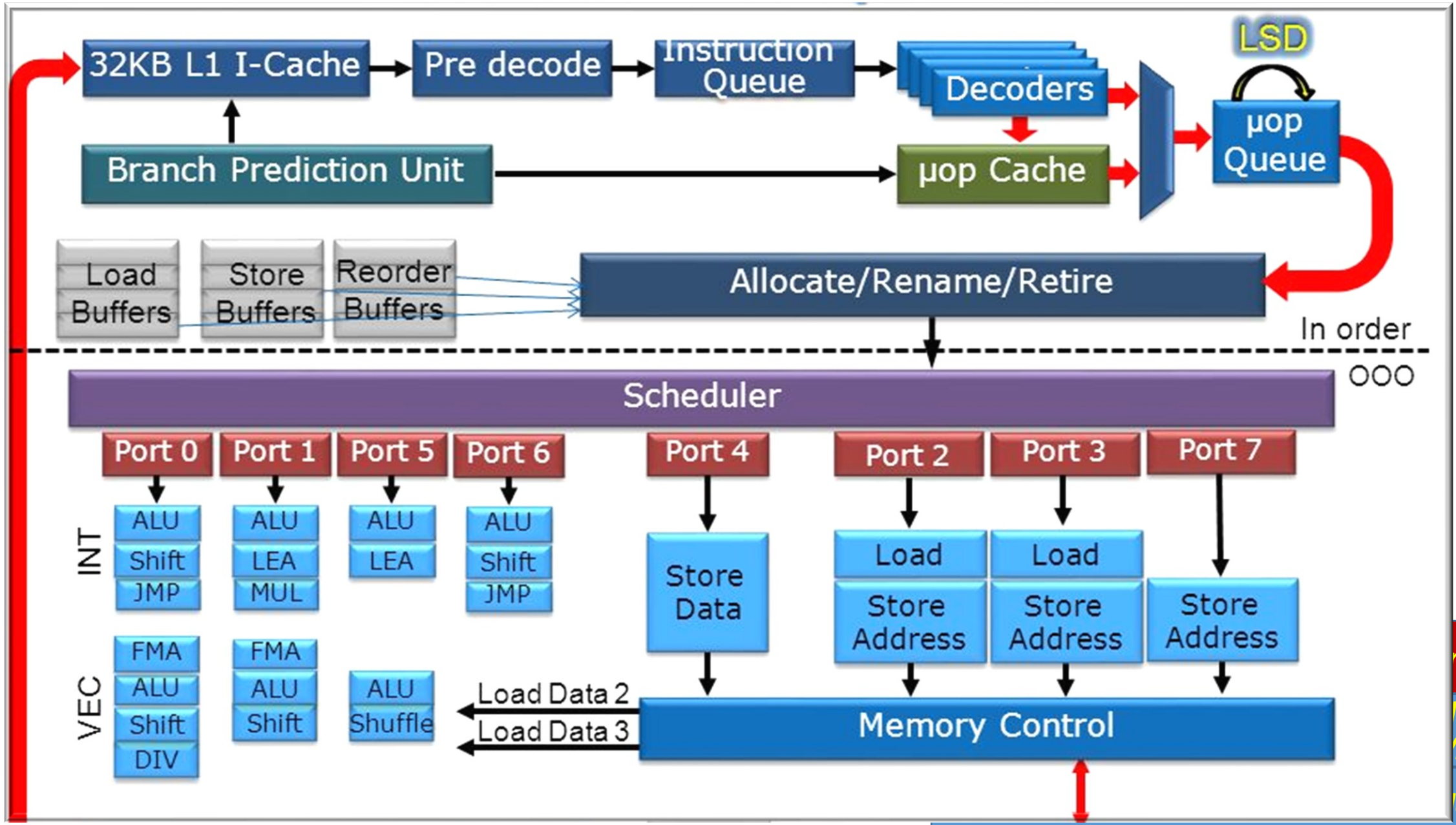
32KB L1 I-Cache
Pre decode
Instruction Queue
Decoders
LSD
µop Queue
Branch Prediction Unit
µop Cache
Load Buffers
Store Buffers
Reorder Buffers
Allocate/Rename/Retire
In order
OOO
Scheduler
Port 0
Port 1
Port 5
Port 6
Port 4
Port 2
Port 3
Port 7
INT
ALU
Shift
JMP
ALU
LEA
MUL
ALU
LEA
ALU
Shift
JMP
Store Data
Load
Store Address
Load
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VEC
FMA
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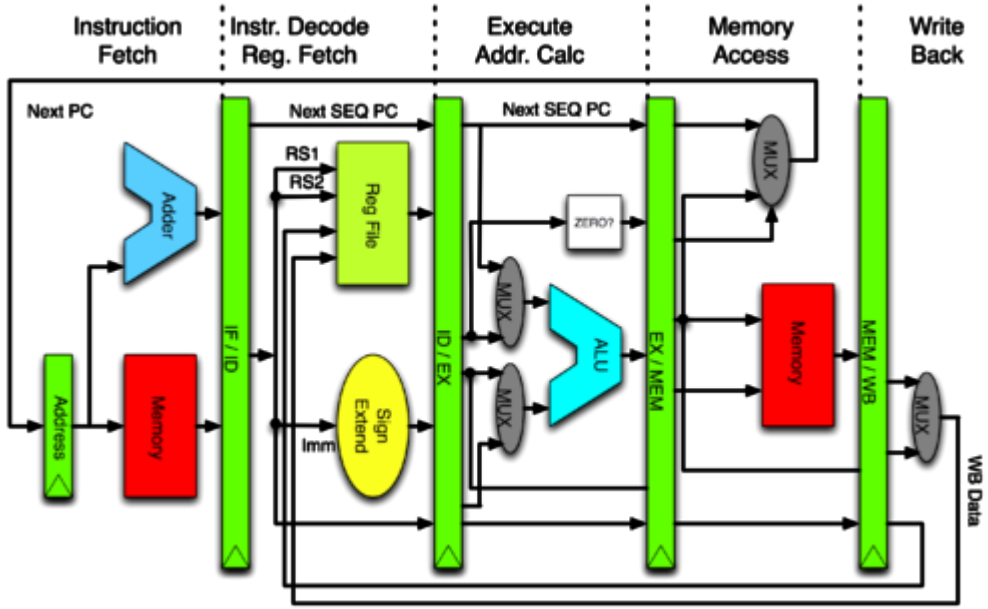


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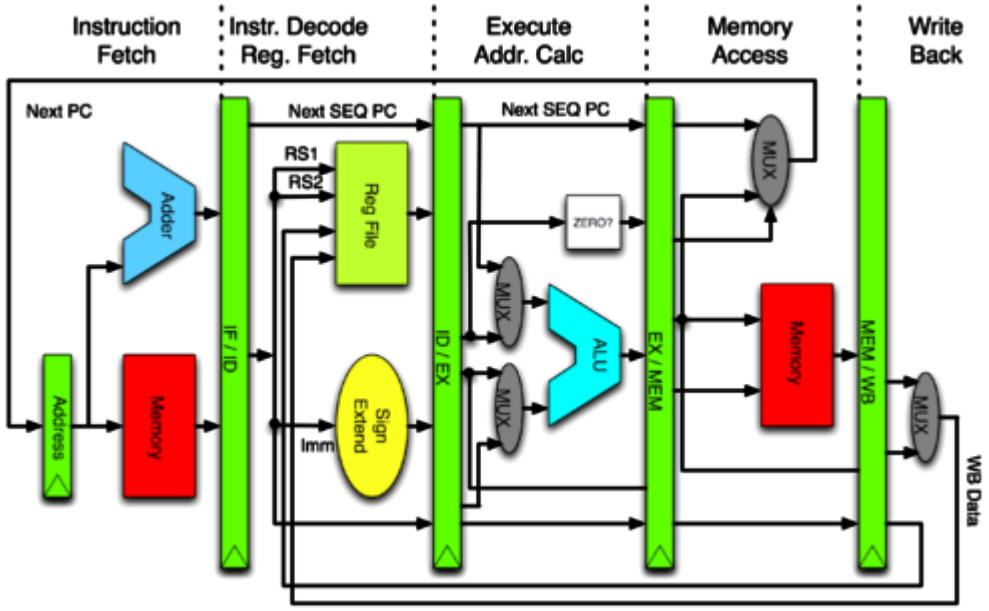

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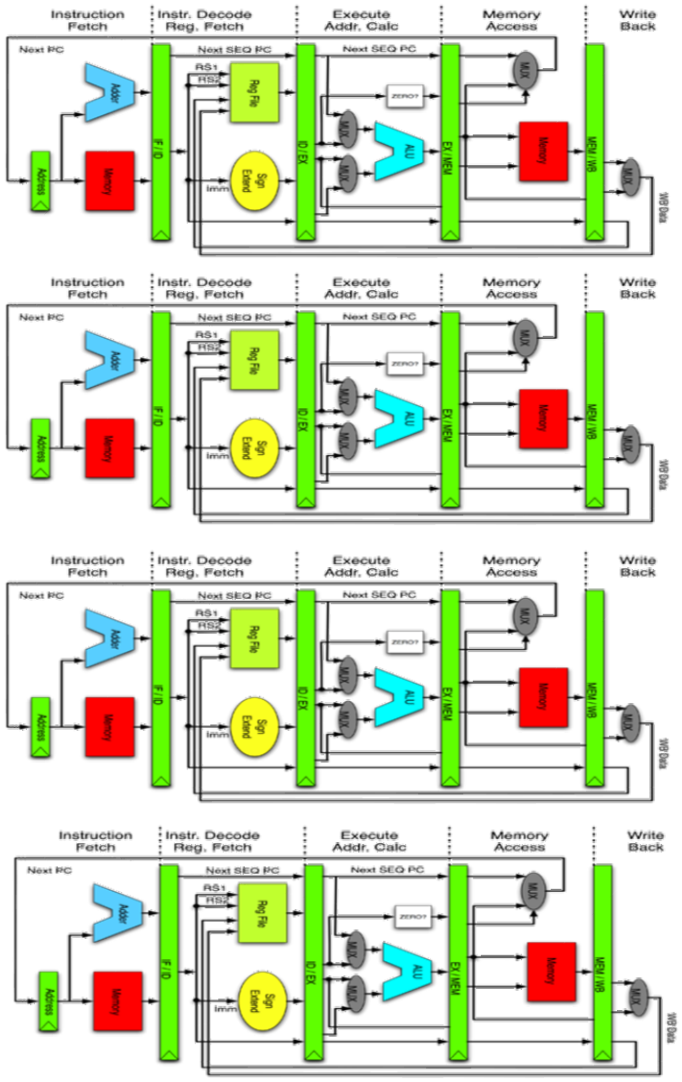

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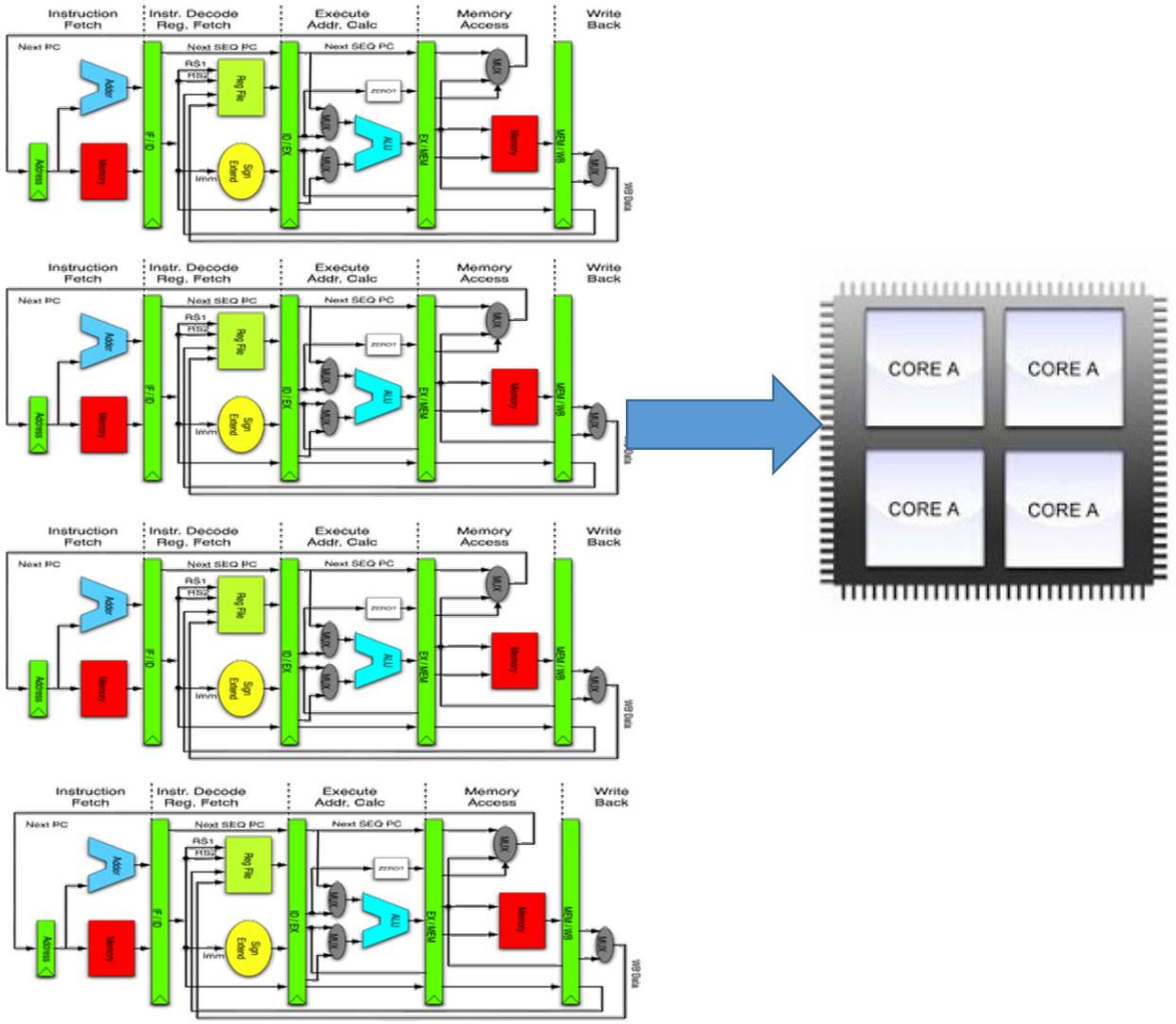

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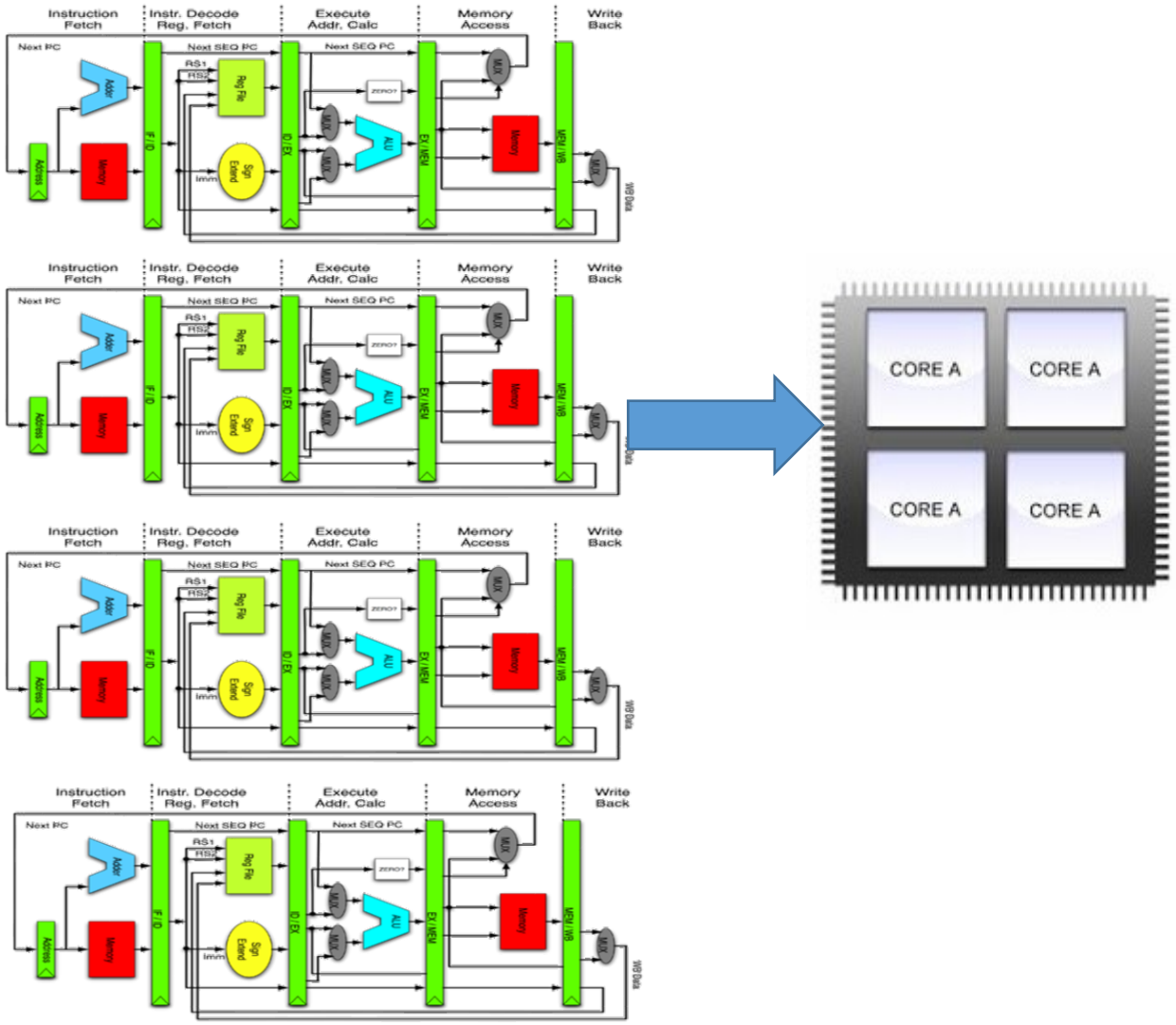


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    pthread_create(
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  }
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- ***Pros: Simple***
- ***Cons: programmer has to find the parallelism!***

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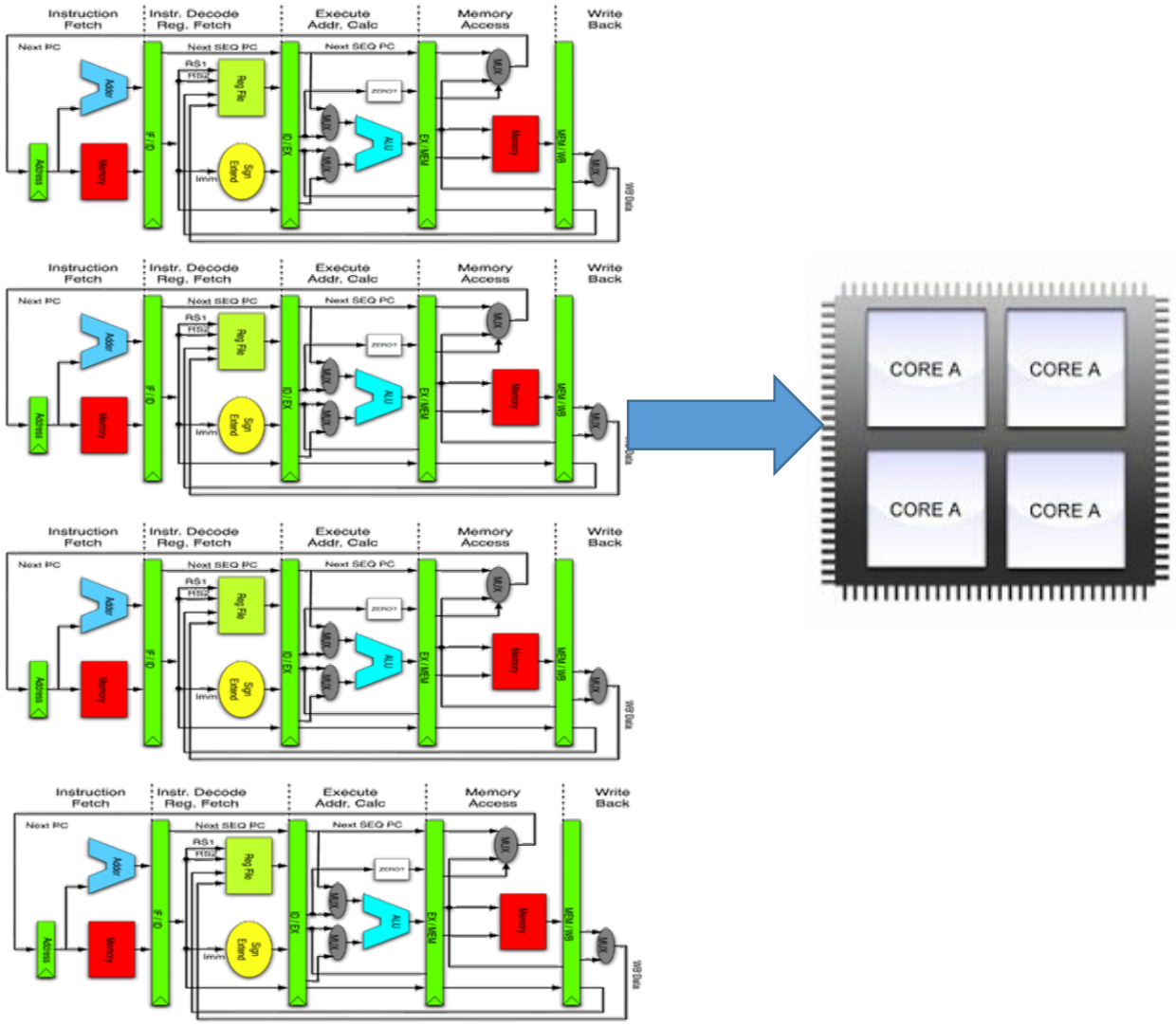


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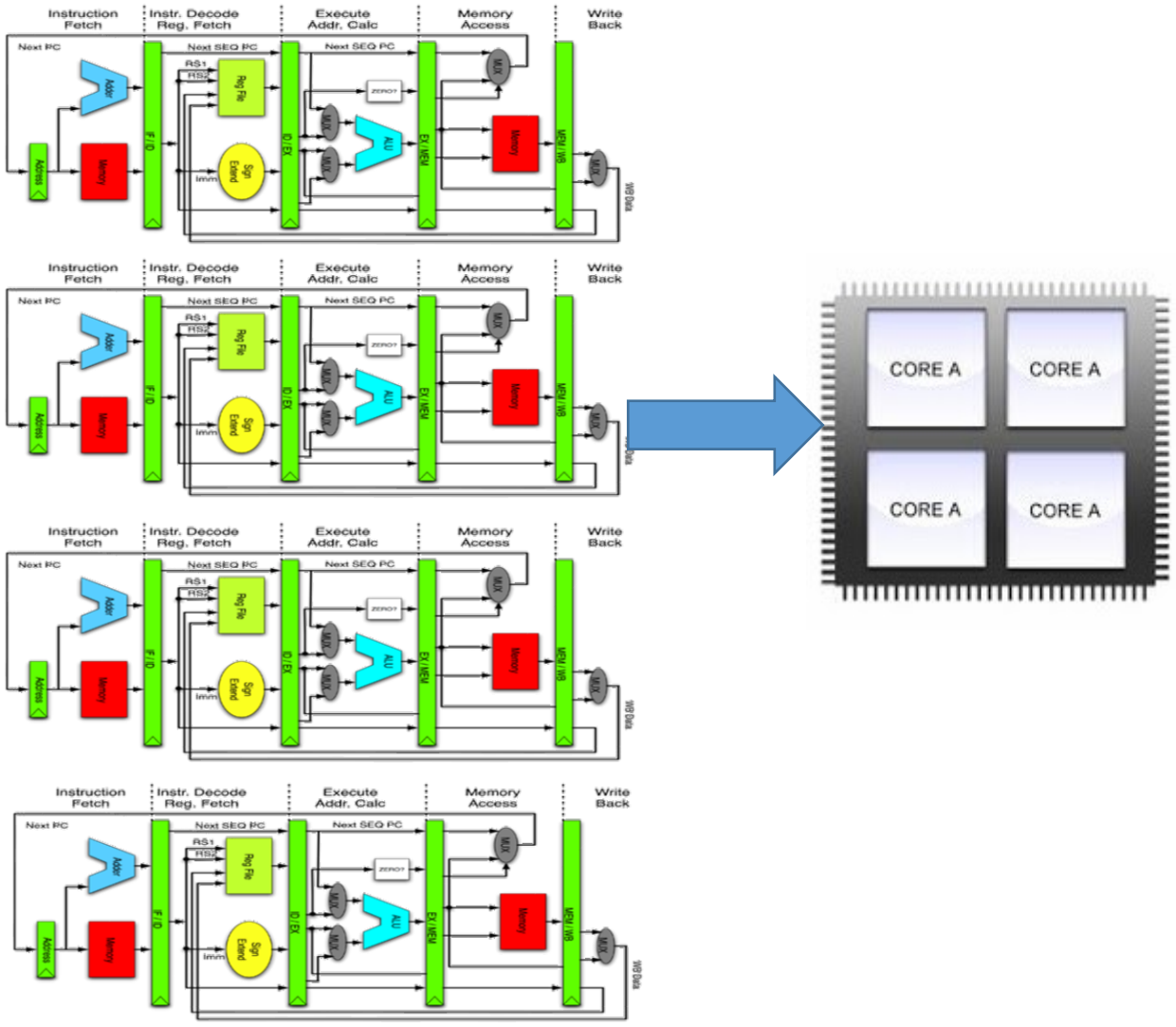


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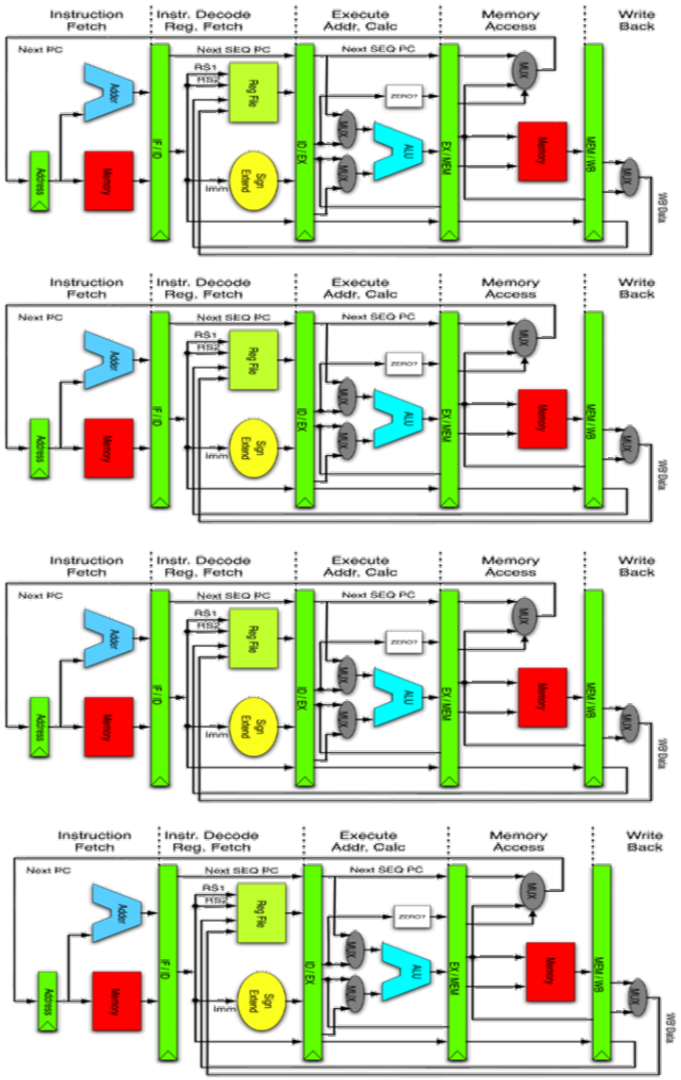
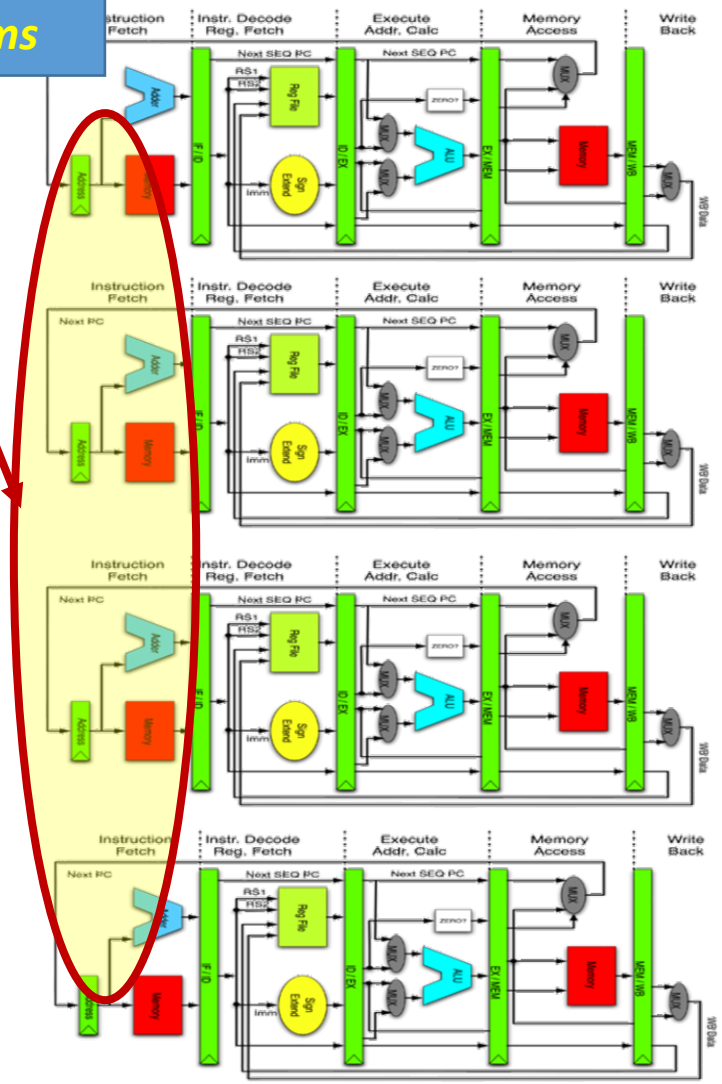
Other techniques extract parallelism here, try to let the machine find parallelism

Superscalar processors



Superscalar processors

Remove extra instruction streams



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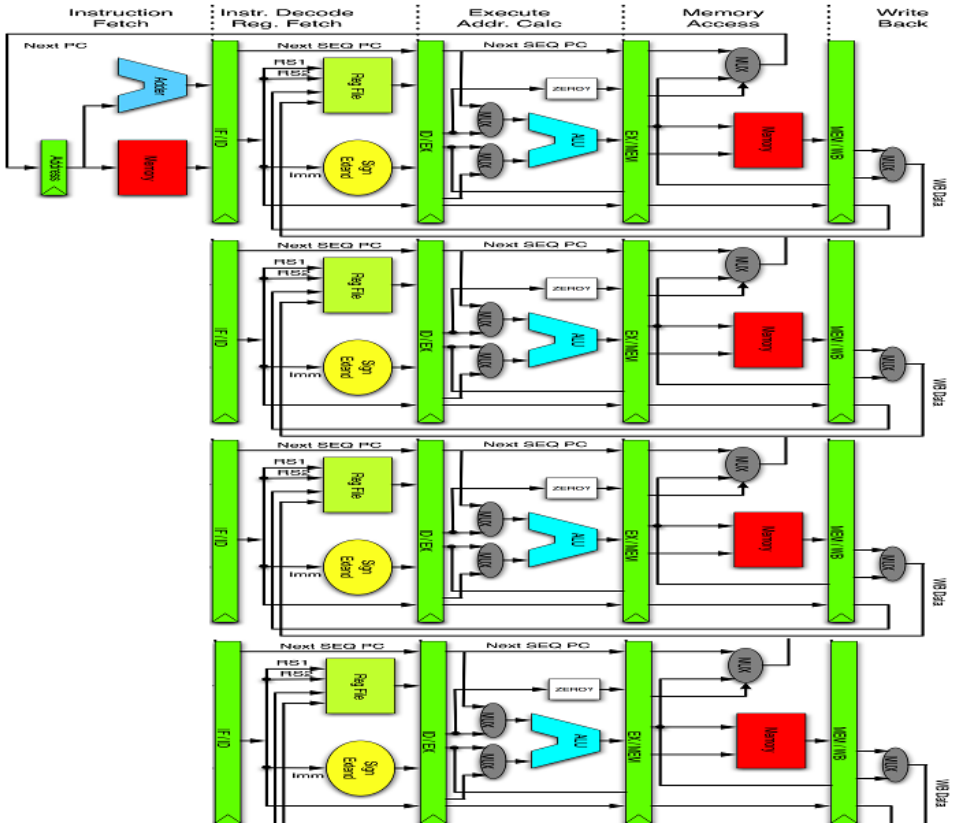

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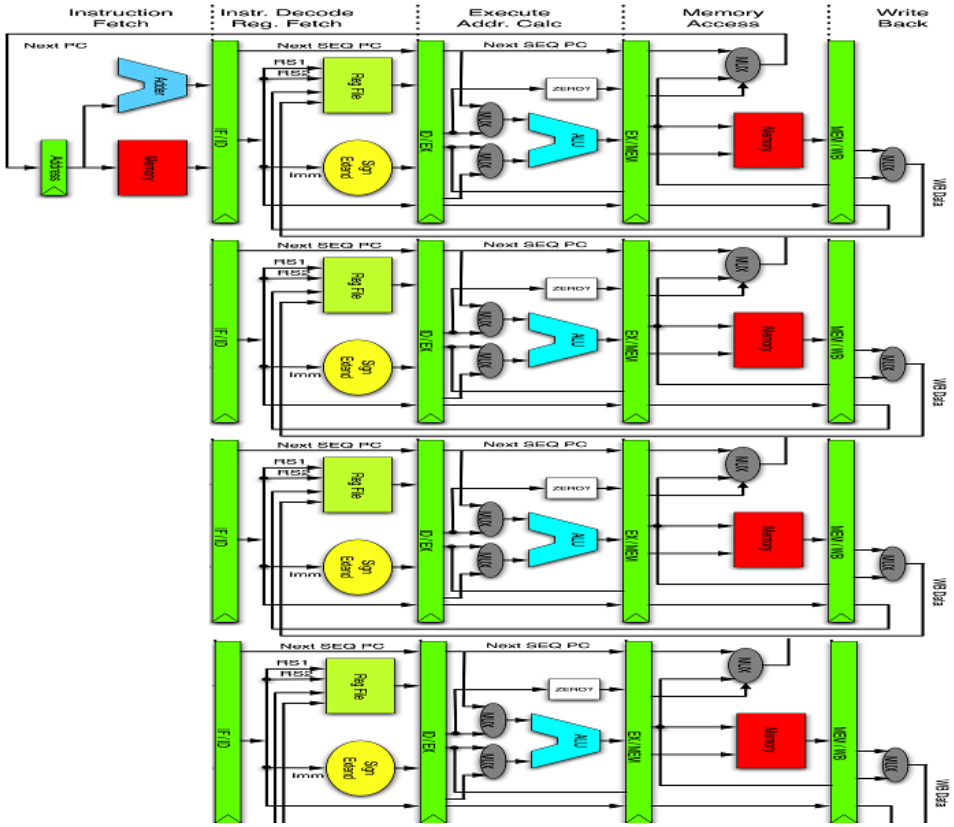


```
main() {
  for(i=0; i<CORES; i++)
    pthread_create(decode_exec);
    while(true) {
      instruction = fetch();
      enqueue(instruction);
    }
}

decode_exec() {
  instruction = dequeue();
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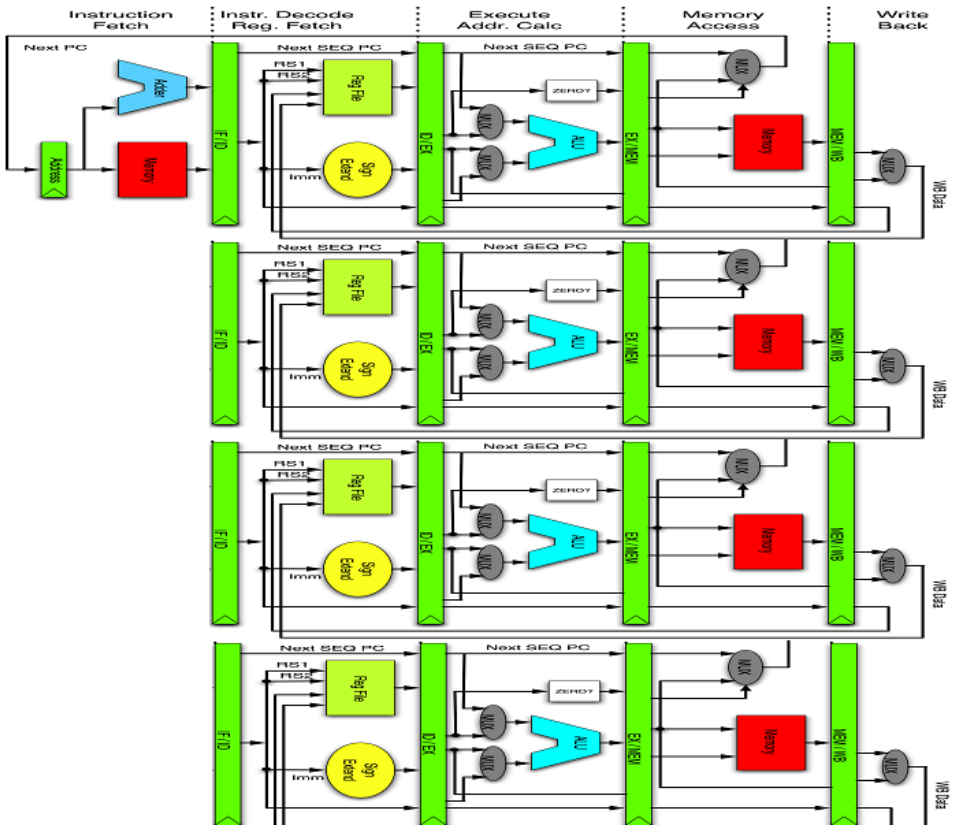


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Doesn't look that different does it? Why do it?

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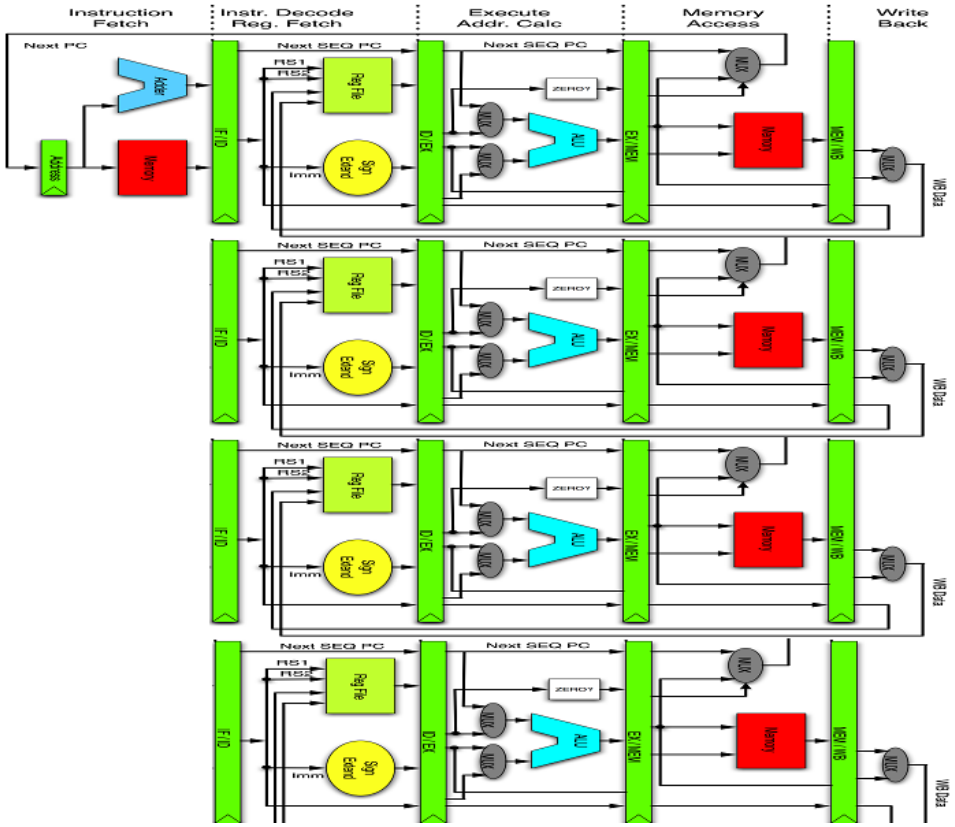


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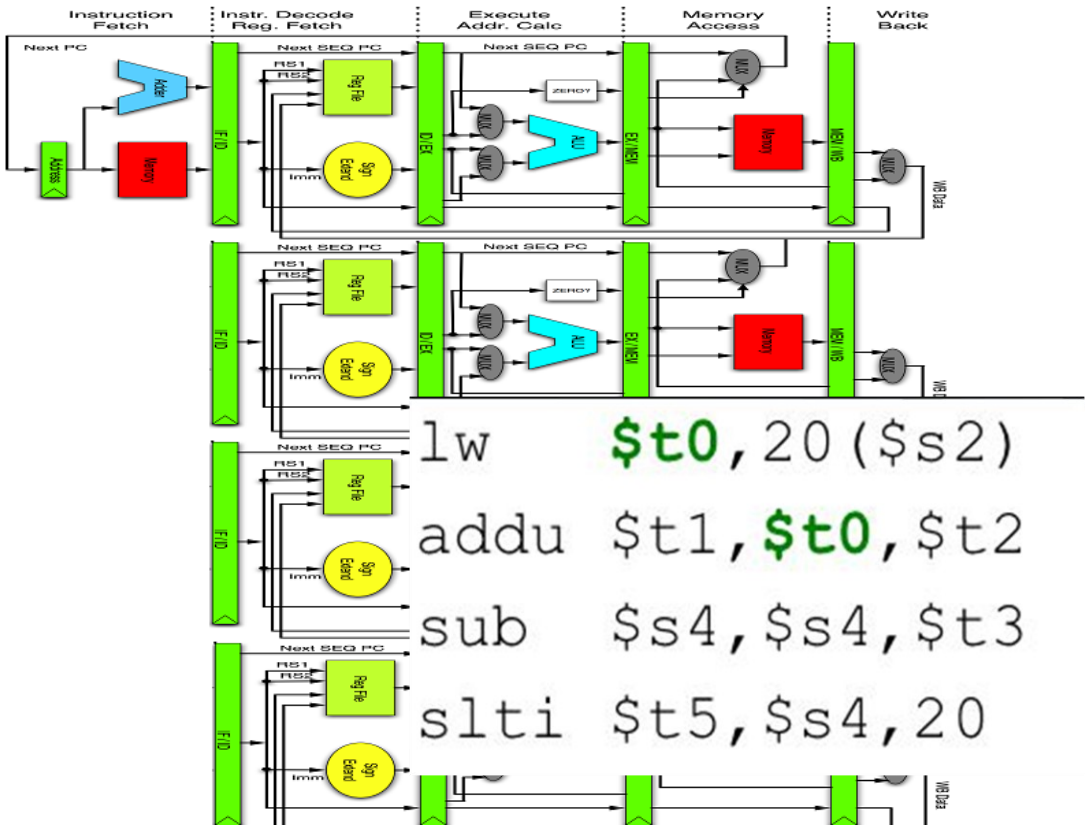
Enables independent instruction parallelism.

Superscalar processors

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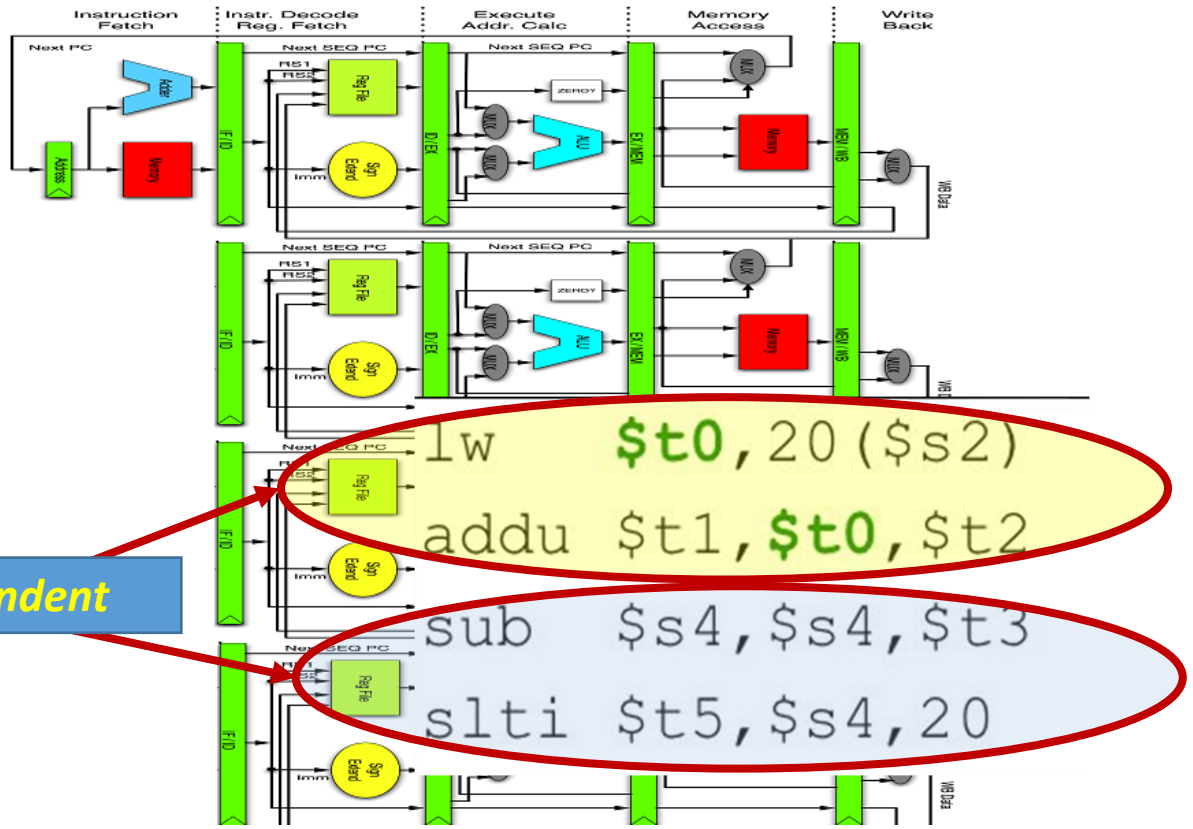

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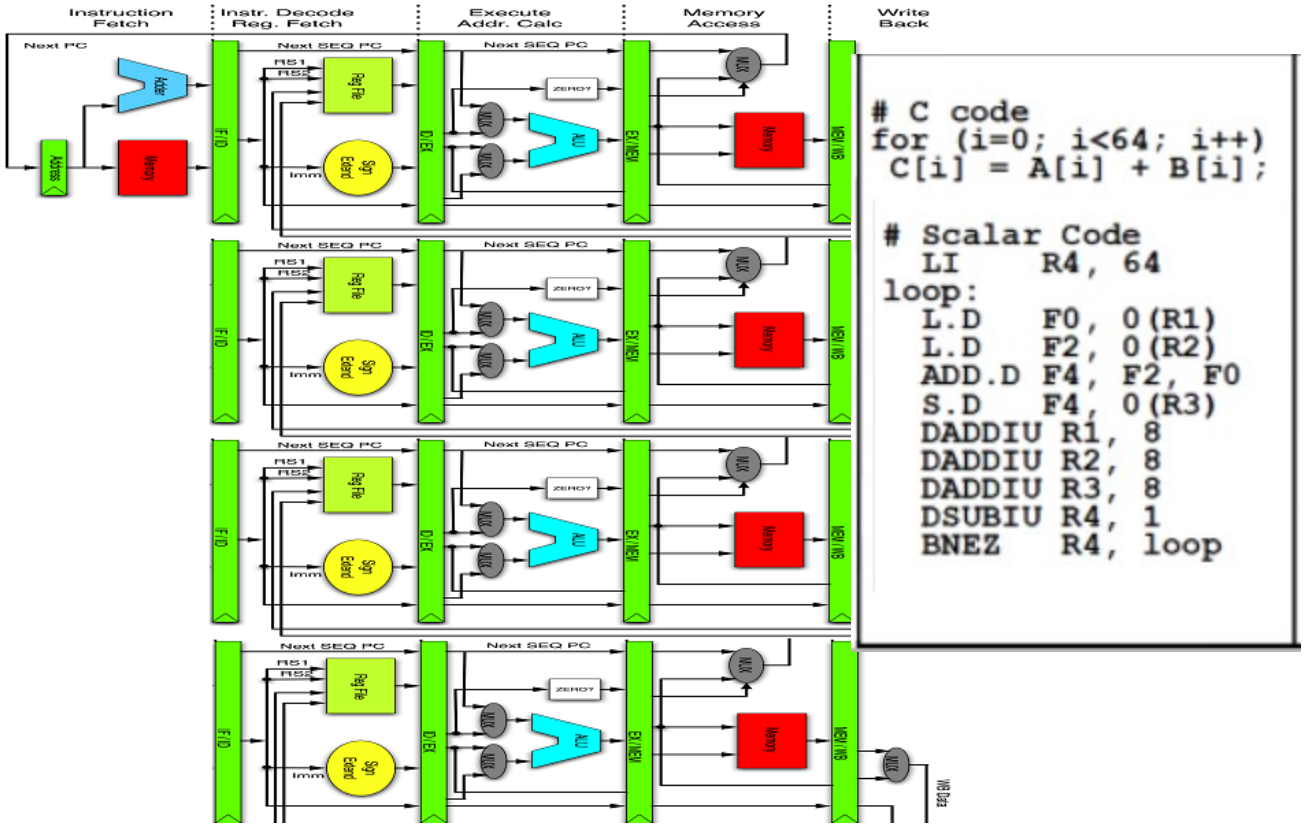
Vector/SIMD processors

```
# C code
for (i=0; i<64; i++)
 C[i] = A[i] + B[i];

# Scalar Code
   LI     R4, 64
loop:
   L.D    F0, 0(R1)
   L.D    F2, 0(R2)
   ADD.D  F4, F2, F0
   S.D    F4, 0(R3)
   DADDIU R1, 8
   DADDIU R2, 8
   DADDIU R3, 8
   DSUBIU R4, 1
   BNEZ   R4, loop
```

Vector/SIMD processors

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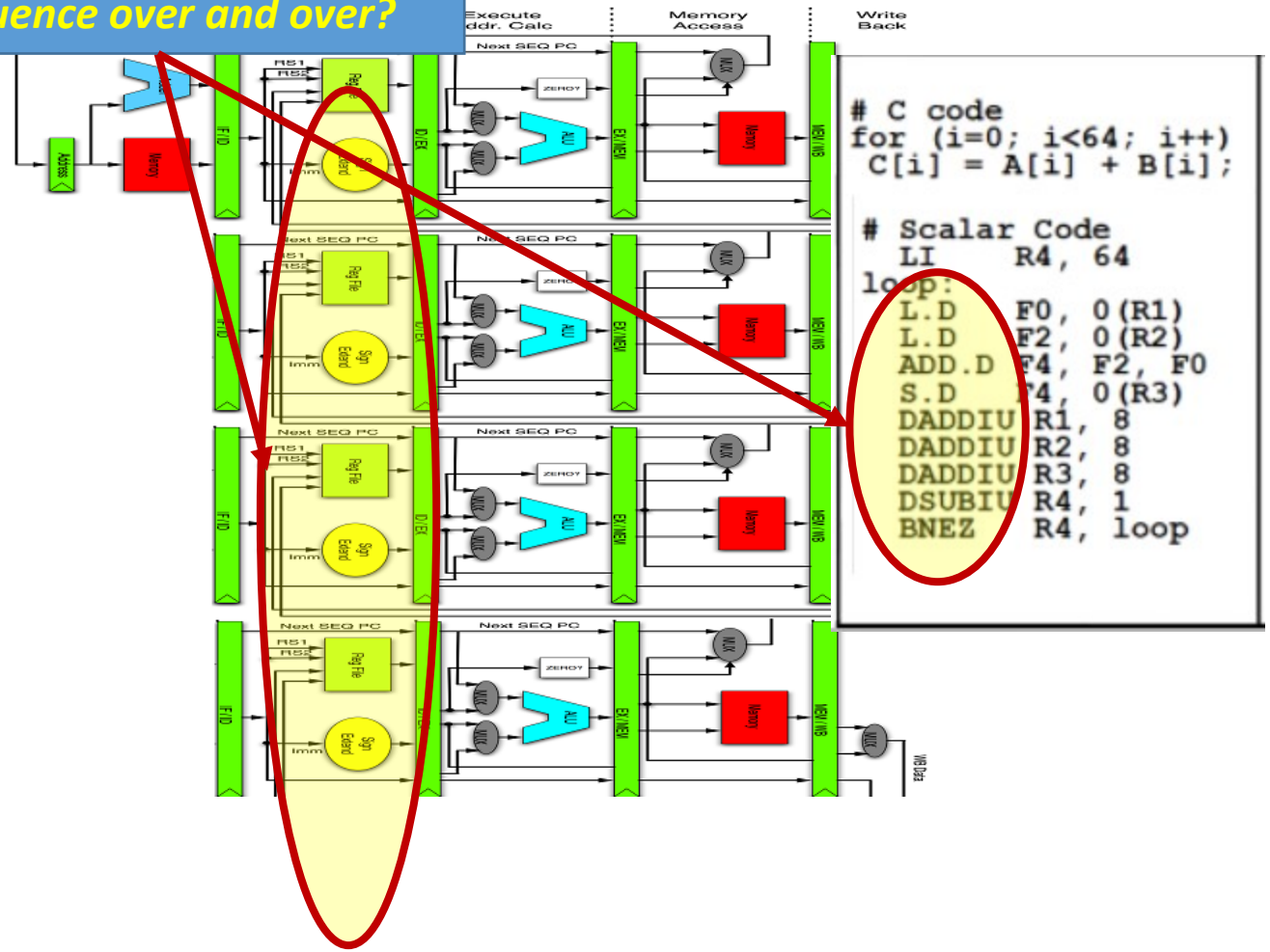
Vector/SIMD processors

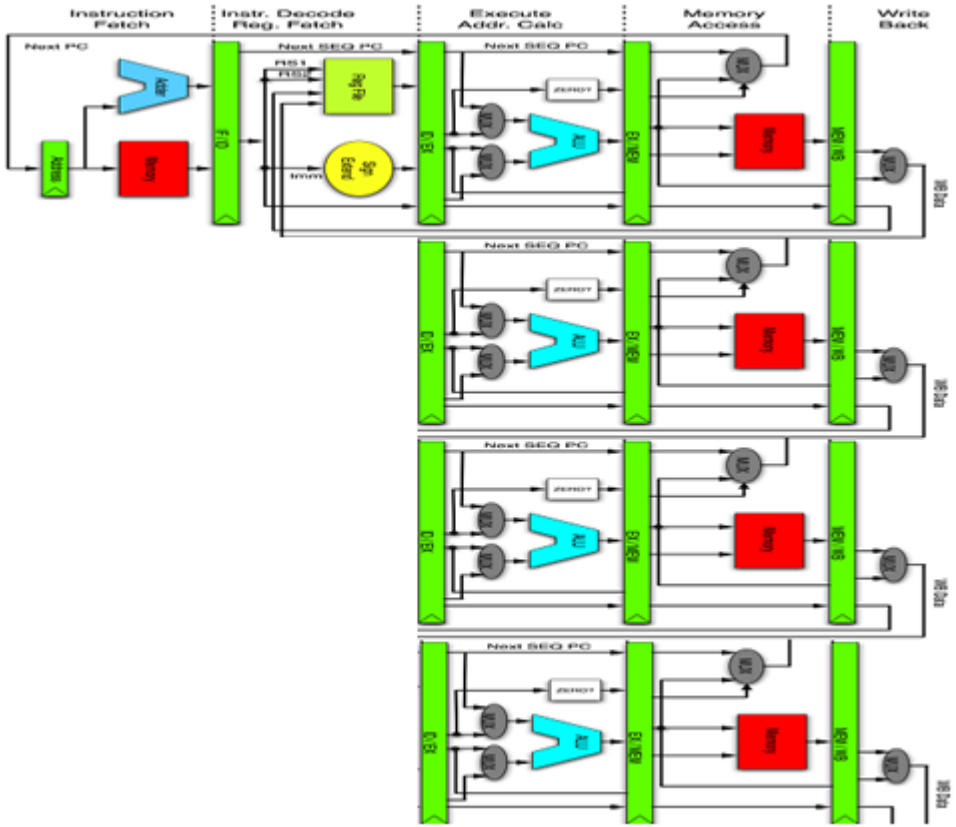
Why decode same instruction sequence over and over?



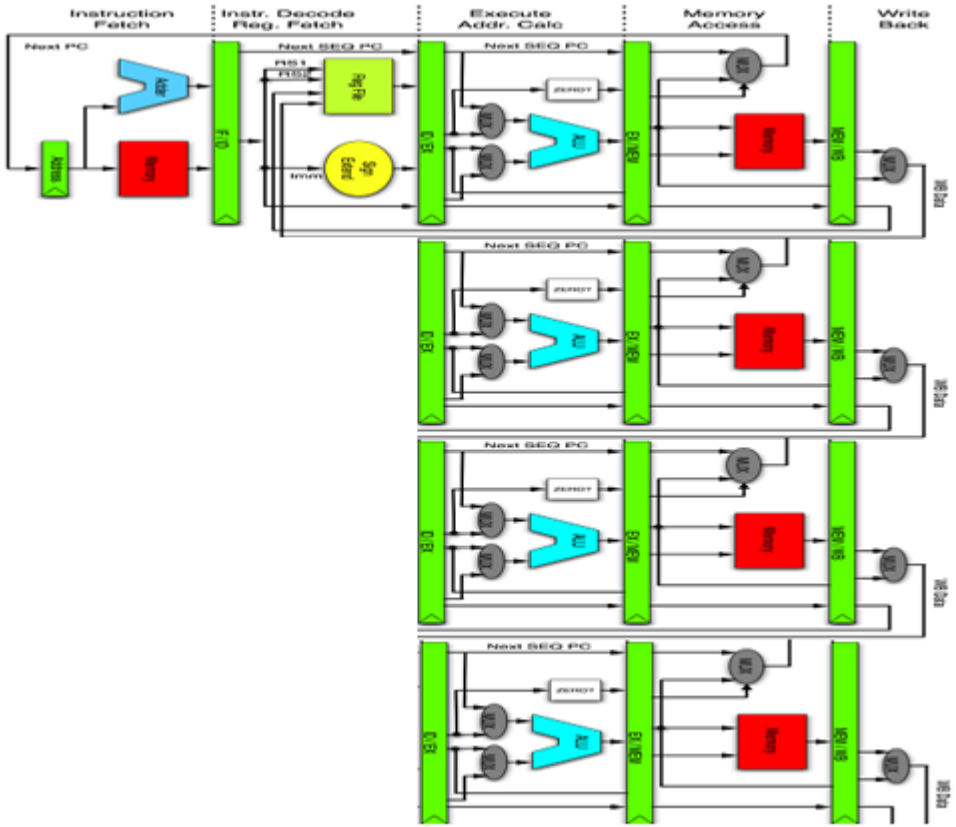

```
# C code
for (i=0; i<64; i++)
 C[i] = A[i] + B[i];

# Scalar Code
   LI     R4, 64
loop:
   L.D    F0, 0(R1)
   L.D    F2, 0(R2)
   ADD.D  F4, F2, F0
   S.D    F4, 0(R3)
   DADDIU R1, 8
   DADDIU R2, 8
   DADDIU R3, 8
   DSUBIU R4, 1
   BNEZ   R4, loop
```

Vector/SIMD processors



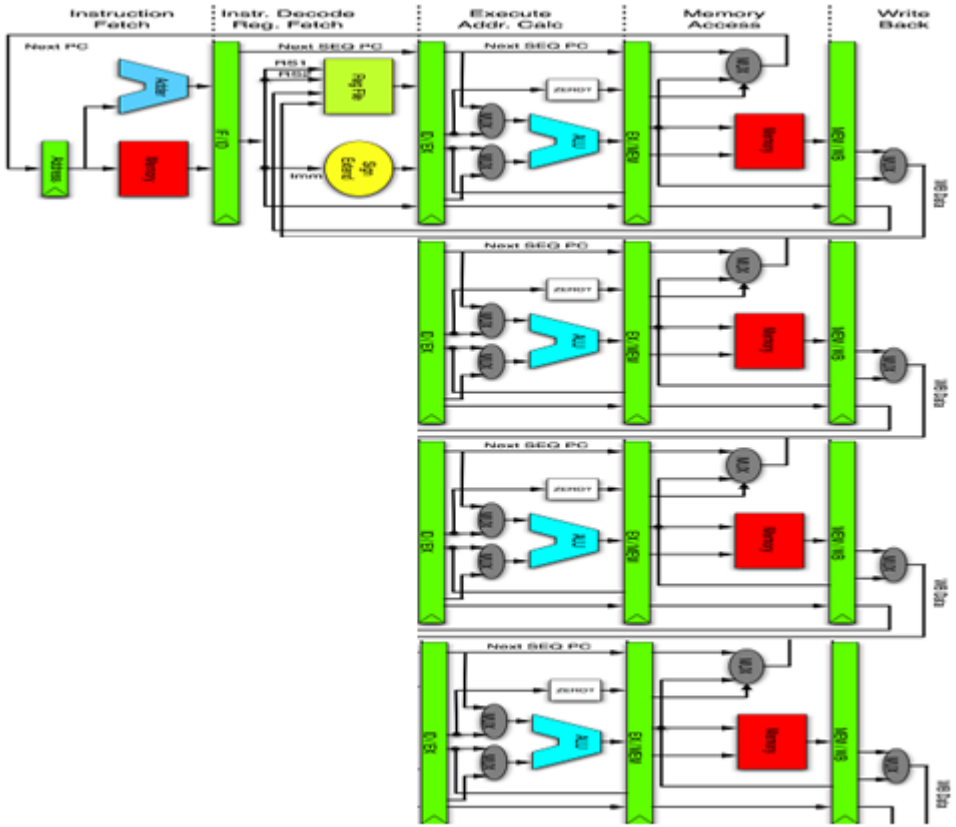
Vector/SIMD processors




```
main() {
  for(i=0; i<CORES; i++)
    pthread_create(exec);
    while(true) {
      ops, regs = fetch_decode();
      enqueue(ops, regs);
    }
}

exec() {
  ops, regs = dequeue();
  execute_calc_addrs(ops, regs);
  access_memory(ops, regs);
  write_back(regs);
}
```

Vector/SIMD processors

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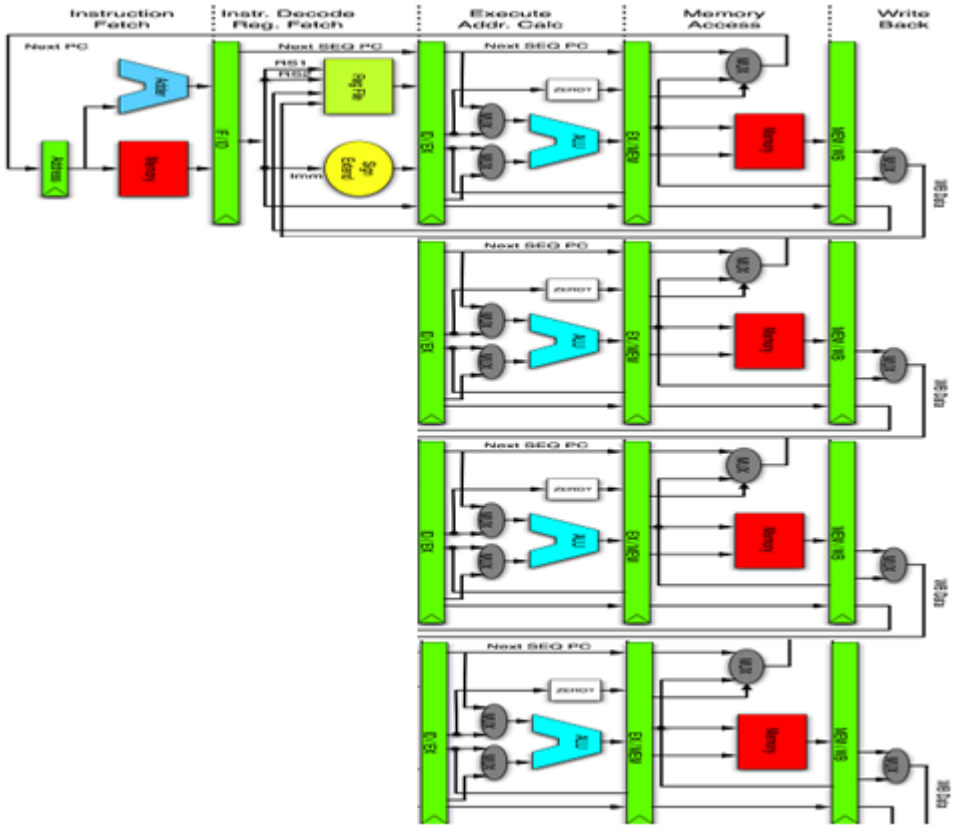
Single instruction stream, multiple computations

Vector/SIMD processors

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Single instruction stream, multiple computations

But now all my instructions need multiple operands!