Parallel Architectures Parallel Algorithms CUDA

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Outline for Today

- Questions?
- Administrivia
 - pedagogical-* machines should be available
- Agenda
 - Parallel Algorithms
 - CUDA

 Acknowledgements: http://developer.download.nvidia.com/compute/develo pertrainingmaterials/presentations/cuda_language/Intro duction_to_CUDA_C.pptx



Faux Quiz Questions

- What is a reduction? A prefix sum? Why are they hard to parallelize and what basic techniques can be used to parallelize them?
- Define flow dependence, output dependence, and anti-dependence: give an example of each. Why/how do compilers use them to detect loop-independent vs loop-carried dependences?
- What is the difference between a thread-block and a warp?
- How/Why must programmers copy data back and forth to a GPU?
- What is "shared memory" in CUDA? Describe a setting in which it might be useful.
- CUDA kernels have implicit barrier synchronization. Why is ____syncthreads() necessary in light of this fact?
- How might one implement locks on a GPU?
- What ordering guarantees does a GPU provide across different hardware threads' access to a single memory location? To two disjoint locations?
- When is it safe for one GPU thread to wait (e.g. by spinning) for another?

| <pre># C code for (i=0; i<64; i++) C[i] = A[i] + B[i];</pre> |
|--|
| <pre># Scalar Code LI R4, 64 loop: L.D F0, 0(R1) L.D F2, 0(R2) ADD.D F4, F2, F0 S.D F4, 0(R3) DADDIU R1, 8 DADDIU R1, 8 DADDIU R2, 8 DADDIU R3, 8 DSUBIU R4, 1 BNEZ R4, loop</pre> |









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|--|--|---|
|--|--|---|



Implementation:

- Instruction fetch control logic shared
- Same instruction stream executed on
- Multiple pipelines
- Multiple different operands in parallel

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What are the potential bottlenecks here? When can it improve throughput?



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Proved Pro



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Only helps if memory can keep the pipeline busy!



• Address memory bottleneck

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- Share exec unit across
 - Instruction streams
 - Switch on stalls

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- Three variants:
 - Coarse
 - Fine-grain
 - Simultaneous



Running example



- Colors \rightarrow pipeline full
- White \rightarrow stall

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Why Vector and Multithreading Background?

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GPU:

- A very wide vector machine
- Massively multi-threaded to hide memory latency
- Originally designed for graphics pipelines...

- 3D world model(objects, materials)
 - Geometry modeled w triangle meshes, surface normals
 - GPUs subdivide triangles into "fragments" (rasterization)
 - Materials modeled with "textures"
 - Texture coordinates, sampling "map" textures → geometry

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display(visible_fragments(frags));



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GeForce 6 series

Dandelion
Late Modernity: unified shaders



Mapping to Graphics pipeline no longer apparent Processing elements no longer specialized to a particular role Model supports *real* control flow, larger instr count

Mostly Modern: Pascal



Definitely Modern: Turing





Cross-generational GPU observations

GPUs designed for parallelism in graphics pipeline:

- Data
 - Per-vertex
 - Per-fragment
 - Per-pixel
- Task
- Vertex processing
- Fragment processing
- Rasterization
- Hidden-surface elimination
- MLP
- HW multi-threading for hiding memory latency

- Simple cores
- Single instruction stream
 - Vector instructions (SIMD) OR
 - Implicit HW-managed sharing (SIMT)
- Hide memory latency with HW multi-threading

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Even as GPU architectures become more general, certain assumptions persist:
1. Data parallelism is *trivially* exposed
2. All problems look like painting a box with colored dots

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2. All problems look like painting a box with colored dots

But what if my problem isn't painting a box?!!?! OR

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Programming Model

- GPUs are I/O devices, managed by user-code
- "kernels" == "shader programs"
- 1000s of HW-scheduled threads per kernel
- Threads grouped into independent blocks.
 - Threads in a block can synchronize (barrier)
 - This is the *only* synchronization
- "Grid" == "launch" == "invocation" of a kernel
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Parallel Algorithms

- Sequential algorithms often do not permit easy parallelization
 - Does not mean there work has no parallelism
 - A different approach can yield parallelism
 - but often changes the algorithm
 - Parallelizing != just adding locks to a sequential algorithm
- Parallel Patterns
 - Map
 - Scatter, Gather
 - Reduction
 - Scan
 - Search, Sort

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If you can express your algorithm using these patterns, an apparently fundamentally sequential algorithm can be made parallel

Map

- Inputs
 - Array A
 - Function f(x)
- map(A, f) \rightarrow apply f(x) on all elements in A
- Parallelism trivially exposed
 - f(x) can be applied in parallel to all elements, in principle

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for(i=0; i<numPoints; i++) {
 labels[i] = findNearestCenter(points[i]);</pre>



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Why is this useful on a box-drawing machine?



Scatter





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 - Associative operator op
 - Ordered set s = [a, b, c, ... z]
- Reduce(op, s) returns a op b op c ... op z

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Scan (prefix sum)

- Input
 - Associative operator op
 - Ordered set s = [a, b, c, ... z]
 - Identity I
- scan(op, s) = [I, a, (a op b), (a op b op c) ...]
- Scan is the workhorse of parallel algorithms:
 - Sort, histograms, sparse matrix, string compare, ...



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- Lambda function maps elements \rightarrow key

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foreach(T elem in ints)
{
 key = KeyLambda(elem);
 group = GetGroup(key);
 group.Add(elem);

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GroupBy using parallel primitives $\zeta \zeta \zeta \zeta \zeta \zeta \zeta$
















