Magnetoelectronic Structures for Non-Volatile Microprocessors

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I. Introduction

One limitation of conventional integrated circuits is their vulnerability to state loss when power is removed from the system. This vulnerability is due to the fact that these circuits use the charge on a variety of capacitative structures to hold state information. Without a power supply, leakage currents quickly drain off the charge stored on these capacitors, destroying the state of an ongoing computation.

Magnetoelectronic devices, which integrate ferromagnetic materials with conventional semiconductor structures, offer the potential to overcome this limitation by using the magnetization state of a ferromagnetic element to store state information. Since ferromagnetic materials retain their magnetization state until a magnetic field of sufficient intensity to re-magnetize the material is applied, they can provide high-performance, non-volatile storage. In this abstract, we describe one such device, the hybrid Hall effect (HHE) device, which can be used to implement a wide range of logic gates that retain their state indefinitely when power is removed and can be integrated into CMOS fabrication processes. We then briefly outline some ideas for ways in which these devices could be used to build power-failure tolerant microprocessors.

II. The Hybrid Hall Effect Device

Figure 1 shows an atomic force micrograph of a hybrid Hall effect device that was fabricated at the Naval Research Laboratory. The device consists of a 2.2 μ by 0.5 μ ferromagnetic bar, which is fabricated on top of a semiconductor mesa. The state of the device can be written by flowing current through a write wire (not shown in the figure) which passes over the ferromagnetic bar. If the current in the write wire is sufficiently large, the magnetic field it induces will magnetize the ferromagnetic bar in either the left or right direction, depending on the direction of current flow in the write wire.

To read the state of the device, a bias current is applied along the bias line shown in the figure. The interaction of this bias current and the magnetic field generated by the ferromagnetic element creates a Hall voltage perpendicular to the current, which can be sensed on the output line of the device. In our previous work [1] we have developed a wide range of HHE-based logic gates that retain their output values indefinitely even in the absence of a power supply.

Prototype HHE devices have been operated at 2GHz clock rates, and require 5mA of input current to change the magnetization state of their ferromagnetic element. Given access to state-of-the-art fabrication processes, HHE devices are expected to scale at least as well as CMOS transistors, with significant decreases in input current as they shrink.

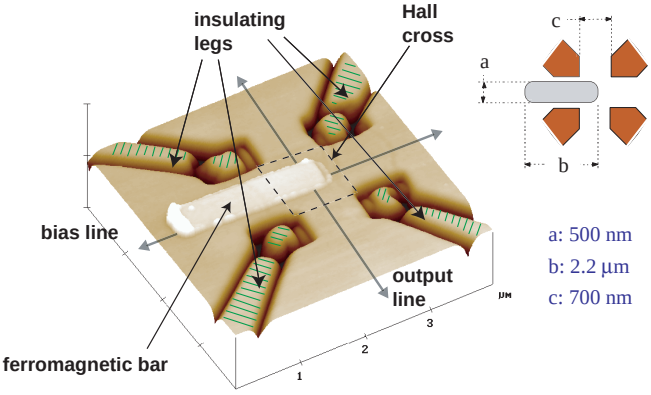

Fig. 1. Hybrid Hall Effect Device

III. Application to Non-Volatile Processors

While HHE devices are some of the fastest known non-volatile circuit elements, their long cycle times and high power requirements compared to CMOS latches make it impractical to construct entire computing systems out of them. Instead, our architectural studies focus on identifying ways in which small numbers of HHE gates can be used to capture the critical state of a computation to allow recovery from power failures.

One example of such a structure is a magnetoelectronic "shadow" register file, which would hold a copy of the processor's register state, along with the address of the last instruction whose result had been copied into the register file. Blocks of instruction results would be copied into the shadow register file in program order, effectively checkpointing the program's progress, and allowing trade-offs between checkpoint frequency and the amount of power consumed writing state into the magnetoelectronic devices. In the presentation, we will present details of the design of the shadow register file, along with proposals for structures to protect the contents of caches during power failures.

In addition, we are exploring the use of the same structures that prevent state loss on power failure to recover from soft errors. Magnetoelectronic devices are significantly less vulnerable to radiation-induced upsets than CMOS structures, so a processor that incorporated HHE devices to allow recovery from power failures could also roll-back to its magnetically stored state if a soft error was detected.

References

[1] S. P. Ferrera and N. P. Carter, "Reconfigurable circuits using hybrid hall effect devices," in *Proceedings of the 13th International Conference on Field Programmable Logic*, 2003.